High Mobility Nanocrystalline Silicon Transistors on Clear Plastic Substrates

Alex Z. Kattamis, Russell J. Holmes, I-Chun Cheng, Ke Long, James C. Sturm, Stephen R. Forrest, and Sigurd Wagner

***Abstract*—We demonstrate nanocrystalline silicon (nc-Si) top-gate thin-film transistors (TFTs) on optically clear, flexible plastic foil substrates. The silicon layers were deposited by plasma-enhanced chemical vapor deposition at a substrate temperature of 150 °C. The n-channel nc-Si TFTs have saturation electron mobilities of 18 $cm^2V^{-1}s^{-1}$ and transconductances of 0.22 $\mu S\mu m^{-1}$. With a channel width to length ratio of 2, these TFTs deliver up to 0.1 mA to bottom emitting electrophosphorescent organic light-emitting devices (OLEDs) which were fabricated on a separate glass substrate. These results suggest that high-current, small-area OLED driver TFTs can be made by a low-temperature process, compatible with flexible clear plastic substrates.**

***Index Terms*—Clear plastic (CP) foil, electrophosphorescence, flexible substrate, nanocrystalline silicon (nc-Si), organic light emitting device (OLED), thin-film transistor (TFT).**

I. Introduction

THIN-FILM transistors (TFTs) based on nanocrystalline silicon (nc-Si) are candidates for active-matrix backplanes on clear, flexible plastic substrates. Nanocrystalline-Si TFTs qualify for CMOS [1] with electron mobilities up to 150 $cm^2V^{-1}s^{-1}$ [2], [3] and hole mobilities up to 1 $cm^2V^{-1}s^{-1}$ [4], [5]. Such nc-Si TFTs have been fabricated on glass [6], [7] and on DuPont Kapton E plastic foil [8]. Kapton E limits light transmission in the blue and therefore cannot be used with bottom emitting organic light emitting devices (OLEDs). Since nc-Si TFTs are fabricated by plasma-enhanced chemical vapor deposition at substrate temperatures from 150 °C to 300 °C, they have the potential to serve as a high-transconductance alternative to amorphous Si (a-Si) TFTs, particularly on plastic substrates requiring low process temperatures. Top gate nc-Si TFTs, however, are hampered by charge trapping in the SiO_2 gate insulator, leading to electrical instabilities and high threshold voltages (V_T) [4]. However, their ON currents in saturation are fairly stable making them suitable for driving OLEDs.

The objective of this work was to determine whether nc-Si TFTs with small channel width to length (W/L) ratios can serve as OLED drivers. Therefore, we fabricated nc-Si TFTs with $W/L = 90/45$ μm on clear plastic substrates to drive electrophosphorescent OLEDs separately deposited on glass [9]. Due to their high mobilities, the TFTs can be integrated with bottom emitting OLEDs into display driver pixels, where the circuit covers less than 15% of the total emission aperture.

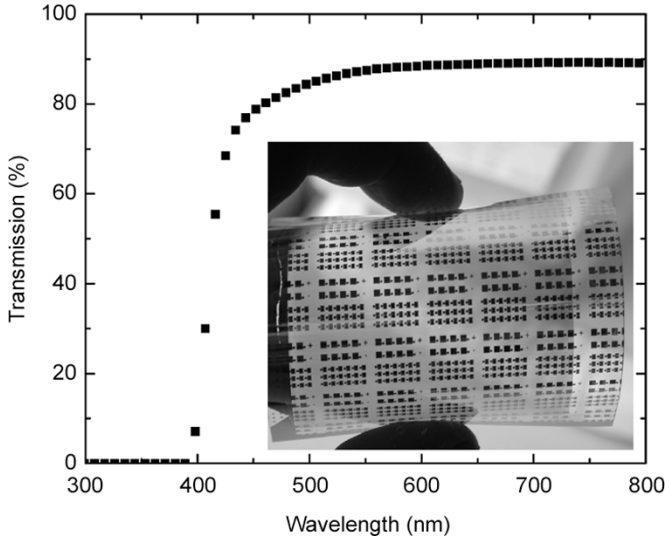

Fig. 1. Optical transmission spectrum of a 50-μm thick CP substrate. The optical transmittance of the uncoated substrate is >80% over the visible spectrum. Inset: nc-Si TFT array on a clear plastic substrate.

II. Experimental Procedures

We used a 50-μm-thick clear plastic (CP) substrate with a glass transition temperature of 325 °C. The n-channel nc-Si TFTs were configured in a staggered top gate, bottom source/drain (S/D) geometry [4]. Fig. 1 shows >80% transmission for the CP substrate over the entire visible spectrum as measured using a spectrophotometer. The inset shows a 6 × 6 cm^2 array of nc-Si TFTs. Except for the clear band along its right edge, the substrate is covered by SiN_x passivation, which gives it a yellow tint. Alloying the SiN_x with oxygen to form SiON will lead to an improved transparency [10]. The Si layers used for the TFT channel were deposited at 150 °C, and the thermally evaporated contact metals were deposited at room temperature. The Cr layers were etched using CR-7S [11], and a mixture of water, phosphoric, acetic, and nitric acids in the ratio 16:2:1:1 $H_3PO_4 : H_2O : HNO_3 : CH_3CO_2H$ was used to etch Al. The SiO_2 gate insulator was etched using 1:10 HF: H_2O, and the Si and SiN_x layers by a 4:1 $CF_4 : O_2$ plasma.

Manuscript received September 12, 2005; revised October 18, 2005. This work was supported in part by the New Jersey Commission on Science and Technology and the Universal Display Corporation, and in part by a Princeton Program in Plasma Science and Technology Graduate Fellowship. The review of this letter was arranged by Editor J. Sin.

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Digital Object Identifier 10.1109/LED.2005.861256

The plasma frequency for reactive-ion etching (RIE) and deposition was 13.56 MHz at a power density of 100 mW/cm^2 and a pressure of 500 mtorr, except where otherwise noted.

Passivation layers of 200-nm-thick SiN_x were first deposited on both faces of the CP using a gas composition of 40:10:1 H_2 : NH_3 : SiH_4 at 110 mW/cm^2. Next, 20-nm-thick a-Si:H followed by 40-nm-thick nominally undoped nc-Si were deposited as a channel seed layer [8]. The a-Si:H was deposited at 110 mW/cm^2 using 1:1 H_2 : SiH_4. The SiH_4 : H_2 ratio was increased to 50:1 for the nc-Si deposition at 80 MHz and dichlorosilane (DCS) was added at 0.5% of the total gas flow to electrically compensate the nc-Si [12]. After thermal evaporation of the 30-nm-thick Al and 10-nm-thick Cr bottom S and D contacts, the films were etched to the CP surface forming 100×100 μm^2 SiN_x islands. The 50-nm-thick n$^+$ nc-Si S/D layer was then deposited from 120:1:1 H_2 : SiH_4 : PH_3 at 80 MHz. The *S* and *D* regions were patterned by RIE to expose the seed layer. Next, a 50-nm-thick nc-Si channel was deposited onto the exposed seed layer from a 15:3:1 H_2 : SiH_4 :DCS source gas mixture at 80 MHz. This was immediately followed by deposition of a 300-nm-thick SiO_2 gate dielectric deposition using 350:2:1 He: N_2O : SiH_4 at 2 torr and 110 mW/cm^2. After the *S* and *D* contact holes were etched, a 50-nm-thick Al layer was deposited by thermal evaporation. Finally, the top Al layer was patterned, defining the gate, *S* and *D* regions.

Electrophosphorescent OLEDs were separately grown on glass substrates pre-coated with a 150-nm-thick layer of indium tin oxide (ITO), degreased with solvents, and cleaned by exposure to UV-ozone following previous reports [13]. The entire device was deposited by thermal evaporation in a vacuum system with a base pressure of 10^{-7} torr. The OLED consists of a 30-nm-thick 4–4′-bis[N-(1 -naphthyl-)N-phenyl-amino] biphenyl (NPD) hole transport layer deposited on the ITO anode. Next, the green phosphorescent material, fac tris(2-phenylpyridine) iridium (Ir (ppy)_3) was doped at 8 wt.% into an N,N′-dicarbazolyl-4-4′-biphenyl (CBP) host forming the 30-nm-thick emissive layer. Finally, a 40-nm-thick electron transport layer consisting of 2,9–dimethyl–4,7–diphenyl–1,10–phenanthroline (bathocuproine, BCP) was deposited and used to confine holes and excitons within the emissive layer of the device. Cathodes consisting of a 0.5-nm-thick layer of LiF followed by a 50-nm-thick layer of Al were patterned by deposition through a shadow mask affixed in a N_2 ambient and with an array of 1-mm diameter openings. The OLEDs exhibit quantum and power efficiencies of (7.0 ± 0.7)% and (20.5 ± 2.1)lm/W, as is typical for Ir(ppy)$_3$/CBP-based devices [13].

III. TFT and TFT/OLED Circuit Results

The characteristics of the TFTs and the OLEDs were measured using an HP4155 parameter analyzer and a calibrated photodiode [14]. The TFTs had $V_T = 13 \pm 0.5$ V, a current ON/OFF ratio of $I_{\rm ON}/I_{\rm OFF} > 10^8$, a subthreshold slope of $S = 1 \pm 0.1$ V/dec, and a transconductance of $g_{\rm msat} = 0.22 \pm 0.03\,\mu S \mu{\rm m}^{-1}$, from which we extract linear and saturation electron mobilities of $\mu_{\rm lin} = 16 \pm 2$ cm^{2}V^{-1}s^{-1}, and $\mu_{\rm sat} = 18 \pm 2$ cm^{2}V^{-1}s^{-1}, respectively. The large V_T is due to charge trapping in the SiO_2, [4] and research is underway to develop a more stable low temperature ($\sim$ 150 °C) SiO_2 dielectric. The nc-Si TFTs exhibit similar V_T, but slightly lower mobilities, than previous results for similar devices deposited on glass and Kapton E [4], [8]. To prevent cracking during substrate flexion, the S/D metal and n$^+$ nc-Si were thinner than in those previous devices, causing increased contact resistance and the observed decrease in mobility.

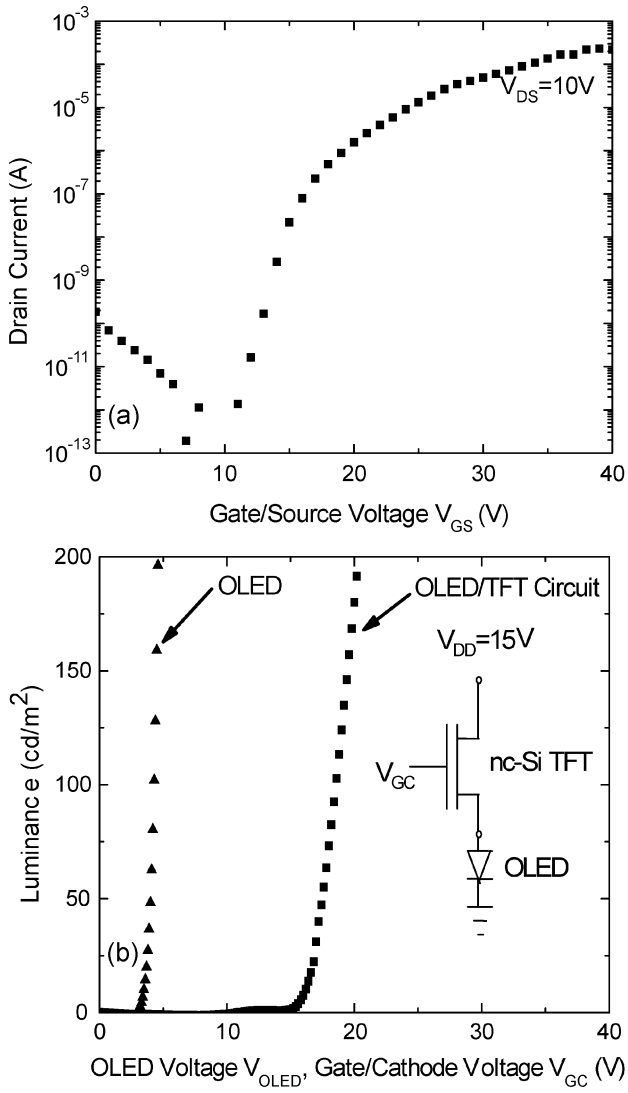

Fig. 2. (a) Drain current versus gate to source voltage characteristic of a nc-Si TFT for $V_{\rm DS} = 10$ V. (b) Luminance versus voltage characteristics for the electrophosphorescent, green-emitting OLED and the TFT/OLED circuit. The gate to OLED cathode voltage, $V_{\rm GC}$, was swept from 0 to 25 V at a drain supply voltage of $V_{\rm DD} = 15$ V. Inset: TFT/OLED circuit schematic.

Fig. 2(a) shows the transfer characteristics for the nc-Si TFT at a S/D voltage of $V_{\rm DS} = 10$ V. After separate evaluation of both the TFT and OLED, the OLED cathode was grounded, while the anode was connected to the TFT source. The TFT drain was biased at a power supply voltage of $V_{\rm DD} = 15$ V [see inset, Fig. 2(b)]. Fig. 2(b) shows the luminance versus voltage across the OLED ($V_{\rm OLED}$) and the gate-to-cathode voltage ($V_{\rm GC}$) characteristics for the TFT/OLED circuit. As noted previously, *W/L*= 2 was used to drive the 1-mm diameter OLED, which is $\sim$30 times the $\sim$ 100×300 μm^2 area of a typical

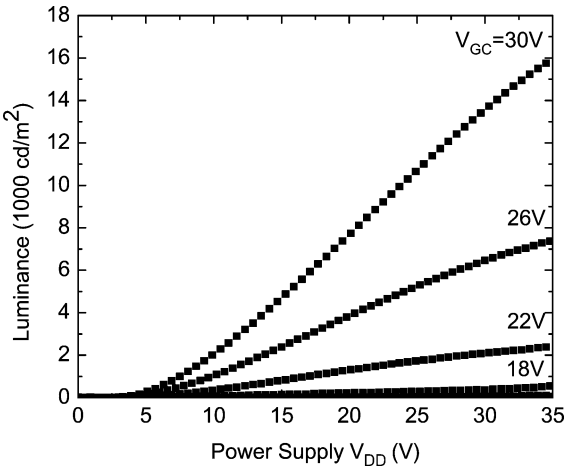

Fig. 3. Luminance versus supply voltage ($V_{\rm DD}$) and gate-to-cathode voltage ($V_{\rm GC}$) for the TFT/OLED circuit in Fig. 2(b).

subpixel [15]. Nevertheless, the TFT supplied sufficient current to obtain a peak luminance of 16 000 cd/m^2 at $V_{\rm GC} = 30$ V and $V_{\rm DD} = 35$ V, as shown in Fig. 3.

For bottom emitting displays, a small footprint pixel circuit is crucial. Previously, it has been shown that a five-TFT a-Si pixel circuit [16] with $W/L = 50$ driver TFTs can serve as stable OLED drivers. With a gate length of 10 μm and 5 μm allocated for gate, S and D overlaps, the area of each TFT needed in such a circuit is approximately 10×30 μm. Using standard interconnect widths of 10 μm and a spacing of 10 μm between devices allows for a total pixel area of ~ 4000 μm^2, without including the storage capacitor. This footprint leaves a light emitting aperture of $>85\%$ in a 100×300 μm pixel.

IV. Conclusion

Nanocrystalline silicon TFTs have been fabricated on a CP foil substrate. These devices function as high current drive transistors for electrophosphorescent OLEDs. Due to the high electron mobilities characteristic of nc-Si, the TFT area can be made sufficiently small to allow for 100×300 μm pixels with an 85% emitting aperture. This letter illustrates the potential of nc-Si TFTs as pixel drivers in flexible, bottom emitting OLED displays.

Acknowledgment

The authors would like to thank The DuPont Company for supplying substrates.

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