

# Stability of Amorphous-Silicon TFTs Deposited on Clear Plastic Substrates at 250 °C to 280 °C

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**Abstract**—Amorphous-silicon (a-Si) thin-film transistors (TFTs) were fabricated on a free-standing new clear plastic substrate with high glass transition temperature ( $T_g$ ) of  $> 315$  °C and low coefficient of thermal expansion of  $< 10$  ppm/°C. Maximum process temperatures on the substrates were 250 °C and 280 °C, close to the temperatures used in industrial a-Si TFT production on glass substrates. The first TFTs made at 280 °C have dc characteristics comparable to TFTs made on glass. The stability of the 250 °C TFTs on clear plastic is approaching that of TFTs made on glass at 300 °C–350 °C. TFT characteristics and stability depend only on process temperature and not on substrate type.

**Index Terms**—Amorphous-silicon (a-Si), device stability, flexible, plastic substrate, thin-film transistor (TFT).

## I. INTRODUCTION

AMORPHOUS-SILICON (a-Si) thin-film transistors (TFTs) on plastic substrates are attractive for backplanes of flexible active-matrix displays. The plastic substrate must be optically clear for active-matrix liquid-crystal displays (AMLCDs) or the conventional bottom-emitting active matrix organic light-emitting displays (AMOLEDs) that require the light to pass through the substrate. The a-Si TFT fabrication process is restricted to temperatures below 140 °C, since most clear plastics have glass transition temperatures ( $T_g$ ) of 120 °C or less and high coefficients of thermal expansion (CTE) [1], [2]. TFTs deposited at temperatures below 140 °C have lower electron mobility, higher off-current and higher gate leakage current than those deposited at higher temperatures. They also exhibit more carrier trapping in the gate nitride and therefore are less stable, which is critical for AMOLEDs that require stable dc drive current [2], [3]. Therefore, it is desirable to keep the TFT process in the optimum temperature range of 300 °C–350 °C, which is that in larger scale industrial use for a-Si TFTs on glass [4]. For easy industrial adoption, a plastic substrate should be a drop-in substitute for glass substrates with as little adjustment of TFT processing as possible. Therefore, a clear plastic substrate is needed that enables a-Si backplane fabrication near 300 °C.

The polyimide Kapton (DuPont) is a typical high-temperature plastic. It has a  $T_g$  of  $\sim 350$  °C and allows the fabrication of TFTs with excellent performance at process temperatures of 150 °C–250 °C [5], [6]. However, Kapton is not optically clear,

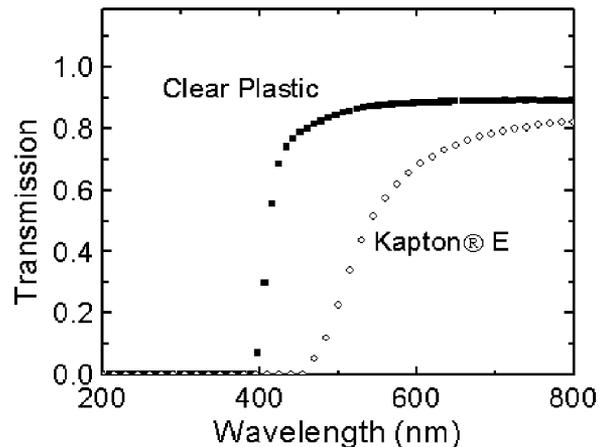


Fig. 1. Optical transmission spectra of 50  $\mu\text{m}$ -thick Kapton 200E and the 75  $\mu\text{m}$ -thick clear plastic.

as is evident from its orange-brown color and the optical transmission spectrum of Fig. 1 for a 50- $\mu\text{m}$  thick Kapton 200E substrate, which cuts off at about 500 nm. In this letter, we present 1) the first a-Si TFTs with excellent performance processed at temperatures up to 280 °C on clear plastic substrates and 2) demonstrate that they are more stable than TFTs processed at 150 °C.

## II. TFT FABRICATION

After the addition of a silicon nitride ( $\text{SiN}_x$ ) buffer layer on each side of the substrate, the process was similar to that used for our standard inverted-staggered a-Si TFTs on glass [5]. The buffer layers planarize the substrate, passivate it against process chemicals, and help the device layers adhere to the plastic substrate. The typical buffer layer thickness was 200 nm. In contrast to mounting the plastic substrates on rigid carriers [6], we kept our substrates freestanding and maintained the back surface optically clean and clear. The critical element of our work is a proprietary clear plastic substrate with  $T_g > 315$  °C and a  $\text{CTE} < 10$  ppm/°C, which is transparent to 400 nm as shown in Fig. 1 (bare substrate). The substrate thickness was  $\sim 75$   $\mu\text{m}$  and the substrate size in our work is 3 in  $\times$  3 in square. The maximum TFT process temperature was reached during the deposition of the  $\text{SiN}_x$  for the buffer layer and the gate dielectric. We fabricated the TFTs at the maximum process temperatures of 250 °C and 280 °C.

## III. RESULTS AND DISCUSSION

Fig. 2(a) shows transfer characteristics of TFTs fabricated at 280 °C, those made at 250 °C were similar. Threshold voltages  $V_T$  ranged from 2.5 to 4.5 V, the ON/OFF ratio is  $\sim 10^6$

Manuscript received October 7, 2005; revised November 22, 2005. The review of this letter was arranged by J. Sin.

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Digital Object Identifier 10.1109/LED.2005.863147

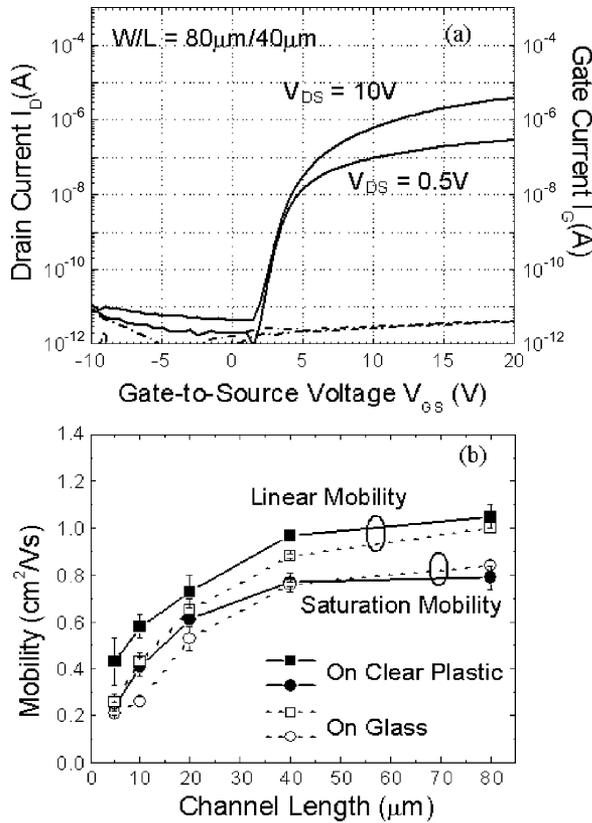


Fig. 2. (a) Transfer characteristics of a TFT ( $W/L = 80/40 \mu\text{m}$ ) made on free-standing clear plastic substrate at  $280^\circ\text{C}$ . (b) Linear (squares) and saturation (circles) mobilities, not corrected for contact resistance, versus channel length for a-Si TFTs fabricated at  $250^\circ\text{C}$  on clear plastic (closed symbols) and on glass (open symbols).  $W = 80 \mu\text{m}$ .

for gate voltages at 20 and 0 V, and the subthreshold slope is 400 mV/dec. At a channel length  $L = 40 \mu\text{m}$ , the linear and saturation mobilities were  $1.0 \text{ cm}^2/\text{Vs}$  and  $0.8 \text{ cm}^2/\text{V} \cdot \text{s}$ , respectively (average of 10 devices). The source-gate leakage current is smaller than the sensitivity of 4 pA of our parameter analyzer. Control TFTs processed identically on glass substrates (without nitride buffer) at  $250^\circ\text{C}$  had linear and saturation mobilities which were both somewhat lower (10% at  $L = 40 \mu\text{m}$  and 30% at  $L = 10 \mu\text{m}$ ) than those on clear plastic [Fig. 2(b)]. The reason for the superior mobilities of the TFTs on the clear plastic substrates is not known. Because the mobilities are not corrected for contact resistance, they appear to decrease at short channel lengths. Other dc TFT characteristics were similar for glass and plastic substrates. These results clearly show that TFTs with excellent performance can be fabricated at high temperatures on free-standing flexible clear plastic substrates.

TFT stability is a key issue for active matrix displays. Threshold voltage of a-Si TFTs changes with the application of the gate bias voltage, because of carrier trapping in the silicon nitride gate insulator and creation of new dangling bonds in the a-Si channel [7], [8]. We performed gate voltage stress tests on the  $250^\circ\text{C}$  TFTs with drain and source grounded. For comparison, control devices made at  $150^\circ\text{C}$  on clear plastic and at  $150^\circ\text{C}$  and  $250^\circ\text{C}$  on glass were also tested. The result of a stress test for a TFT made on clear plastic at  $150^\circ\text{C}$  is shown in Fig. 3. With the same stress condition, the threshold

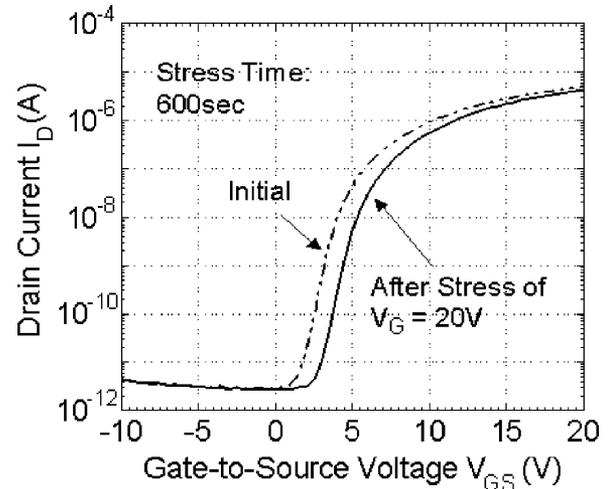


Fig. 3. Transfer characteristics of a-Si TFT made at  $150^\circ\text{C}$  on clear plastic before (dotted line) and after (solid line) gate bias stressing at 20 V for 600 s at room temperature.

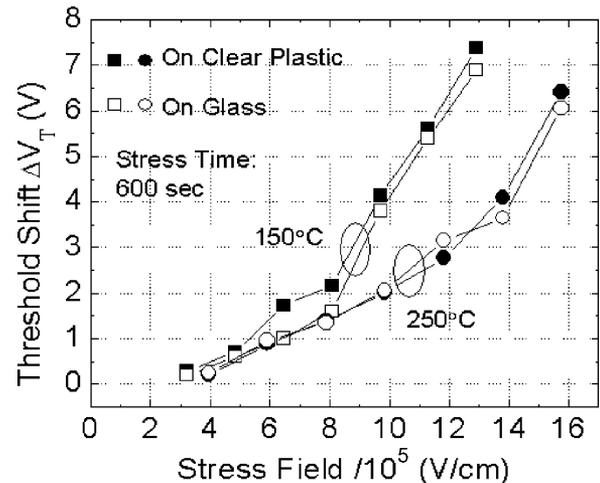


Fig. 4. TFT threshold voltage shift after gate stressing at room temperature for 600 s, as a function of gate stress field, for clear plastic (closed symbols) and glass (open symbols) substrates. Circles are for  $250^\circ\text{C}$  process, squares are for  $150^\circ\text{C}$  process.

voltage shift  $\Delta V_T$  is smaller in TFTs made at  $250^\circ\text{C}$  than those made at  $150^\circ\text{C}$ . That the TFT stability is a function only of process temperature and not of substrate type is clearly evident from Fig. 4. The stressing does not substantially alter the mobility, off current and ON/OFF ratio of the TFTs.

Separately, TFTs made on clear plastic substrates at  $150^\circ\text{C}$  and  $250^\circ\text{C}$  were stressed for up to 24 h at the same gate bias electric field of  $10^6 \text{ V/cm}$ . The nearly uniform lateral shift of the  $\Delta V_T$  data of Fig. 5 shows that the lifetime in  $250^\circ\text{C}$  devices is a factor of about five longer than in  $150^\circ\text{C}$  devices.

We now compare our stability results to literature data for a-Si TFTs processed at higher temperatures on glass ( $300^\circ\text{C}$ – $360^\circ\text{C}$ ). Fig. 6 shows the threshold voltage shift after 600 sec of stress as a function of stress field for our  $150^\circ\text{C}$  and  $250^\circ\text{C}$  TFTs on clear plastic, for TFTs on Kapton 200E polyimide from our lab made at  $150^\circ\text{C}$  [9], and TFTs made at temperatures of  $300$ – $360^\circ\text{C}$  on glass [8], [10], [11]. All data closely follow straight lines on a log-log plot, with slopes of  $\sim 2$

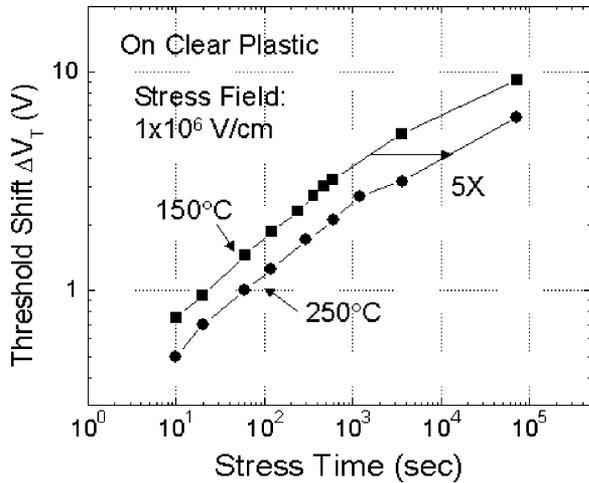


Fig. 5. TFT threshold voltage shift versus stress time at constant gate bias for TFTs made at 150 °C and 250 °C on clear plastic.

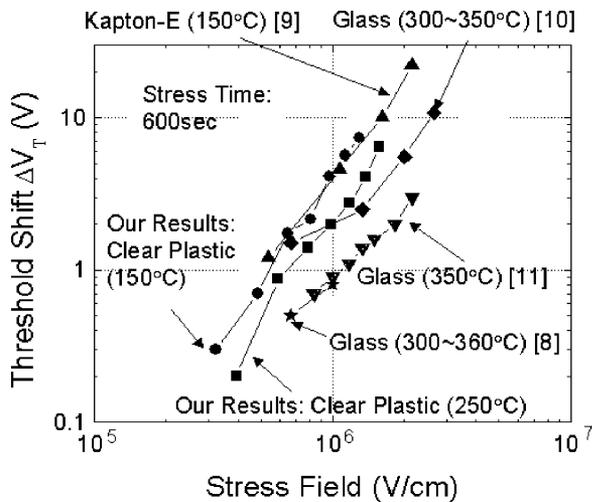


Fig. 6. TFT threshold voltage shift as a function of gate electric field, held constant for 600 s. Various substrates and process temperatures are labeled.

[7], [8]. TFTs made on Kapton E at 150 °C in our laboratory [9] about five years ago give results almost identical to our 150 °C TFTs on clear plastic, suggesting a stable fabrication process. The 250 °C devices on clear plastic are superior to the 150 °C devices as discussed above. It is evident that  $\Delta V_T$  is reduced when the process temperature increased. The 250 °C results on plastic begin to approach the 300 °C–350 °C results on glass. Further improvement is expected for TFTs fabricated on clear plastic at 300 °C.

#### IV. CONCLUSION

a-Si TFTs have been made on clear plastic substrates that allow high process temperatures of up to 280 °C. The TFTs have dc characteristics similar to those of industry-standard a-Si TFTs fabricated on glass in the 300 °C range. The stability under gate bias stress of the TFTs on clear plastic is approaching that of standard TFTs on glass. These results represent an important step toward a generic TFT backplane on a flexible and optically clear substrate.

#### ACKNOWLEDGMENT

The authors gratefully acknowledge the DuPont Company and NJCST for supporting this research and DuPont Company for providing the substrates.

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