Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates

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Abstract — Mechanical stress in hydrogenated amorphous-silicon (a-Si:H) thin-film transistors (TFTs) is becoming an important design parameter, especially when the TFTs are made on compliant substrates. Excessive stress always has been avoided to prevent film fracture and peeling. Now, attention is turning to the effects of stress on the TFT backplane dimensions and hence on the overlay alignment. The goal is to keep the size of the circuit-on-substrate composite structure the same at successive critical photolithographic steps. This is done most easily by keeping the structure flat. We show that a compensating stress can be dialed into the silicon nitride (SiN_x) gate dielectric to also keep the substrate size constant. Varying the stress in the SiN_x gate dielectric did not significantly change the as-fabricated TFT characteristics.

Keywords — *Thin-film transistor, amorphous silicon, silicon nitride, plastic substrate, overlay registration, stress control, deposition power.*

1 Introduction

Organic polymer foils are major substrate candidates for flexible electronics. They offer the advantages of light weight, transparency, flexibility, even deformability, and possibly low cost. However, organic polymers typically have high coefficients of thermal expansion, low elastic moduli, and low dimensional stability compared to conventional glass substrates. These characteristics bring with them challenges in overlay registration during device fabrication.

Bonding the compliant polymer substrate to a rigid carrier throughout the processing can improve the dimensional stability. The adhesive must provide sufficiently strong bonding between the substrate and the carrier, resist the process chemicals, degas little and release few contaminants, and be easily removed at the end of the process. However, thermoplastic adhesives impose a ceiling on the process temperature that is necessarily lower than the highest working temperature of the substrate. This requirement makes the process window narrow and therefore may degrade device performance. In the research described here, we worked with nearly free-standing substrates. The substrates were only temporarily held loosely in a frame for deposition and were flattened for photolithography. The experimental results obtained by this handling technique will be particularly useful to future roll-to-roll processing.

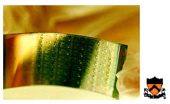
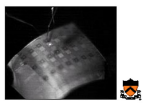
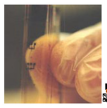
2 Mechanical behavior of film-on-substrate structures

When a device film is deposited on a substrate, the mismatch strain, ε_M, between the film and the substrate can cause deformation of the film-on-substrate structure. The response of the structure to mismatch strain depends highly on the elastic modulus, Y, and the thickness, d, of the film and of the substrate. With few exceptions[1] the substrate is much thicker than the circuit films, so that $d_s >> d_f$, where d_s and d_f are the substrate and film thicknesses. Table 1 lists examples of device films on flexible substrates that represent the four different combinations of Y. Based on relative mechanical strength, *i.e.,* the product $Y{\cdot}d$, three different regimes are encountered. When $Y_s \cdot d_s >> Y_f \cdot d_f$, the substrate dominates and the film must comply with it. The resulting radius of curvature, R, is large (*i.e.,* small curvature $K \equiv 1/R$) and is described by the Stoney equation[6]:

$$R = \frac{Y_s^* d_s^2}{6\varepsilon_M Y_f^* d_f}, \qquad (1)$$

where Y_s^* and Y_f^* are the biaxial elastic moduli of substrate and film. When the film faces outward (convex), the sign of the radius of curvature R is defined as negative because then the film is in compression. R is positive when the film

TABLE 1 — The four combinations of stiff or compliant device films and flexible substrates. Illustrations clockwise from upper left: M. Wu *et al.*,[2] C. C. Wu *et al.*,[3] Klauk *et al.*,[4] Gleskova.[5]

$Y_s \cdot d_s$ versus $Y_f \cdot d_f$		thin film (small d_f)	
		stiff (large Y_f)	compliant (small Y_f)
thick substrate (large d_s)	stiff (large Y_s)	poly-Si TFT / steel substrate  $Y_s \cdot d_s >> Y_f \cdot d_f$	OLED / steel substrate  $Y_s \cdot d_s >> Y_f \cdot d_f$
	compliant (small Y_s)	a-Si TFT / polymer substrate  $Y_s \cdot d_s \approx Y_f \cdot d_f$	OTFT / polymer substrate  $Y_s \cdot d_s >> Y_f \cdot d_f$

Received 02/04/05; accepted 02/15/05.

The authors are with Princeton University, Department of Electrical Engineering and PRISM, Princeton, NJ 08544; telephone 609/258-5902, fax -1840, e-mail: iccheng@princeton.edu.

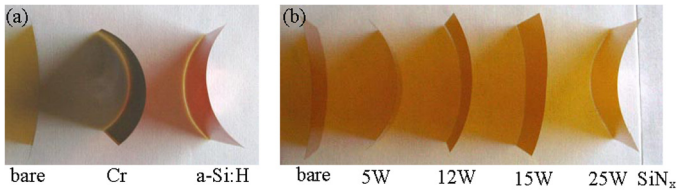


FIGURE 1 — Curvature induced by stress in films of (a) Cr and a-Si:H and (b) SiN_x deposited over a range of RF power, all on 50-µm-thick Kapton® 200E polyimide substrates. All films are on the side of the substrate that faces left. The 300–500-nm thick SiN_x and the 250-nm-thick a-Si:H films were deposited at 150°C, and the 80-nm-thick Cr was deposited by thermal evaporation without control of substrate temperature. The built-in stress of Cr is tensile and that of a-Si:H is compressive. The built-in stress in SiN_x can be adjusted by deposition power. The bare substrate has the radius of curvature R_0.

faces inward (concave) because the film is in tension. When $Y_s \cdot d_s << Y_f \cdot d_f$, the film dominates. This situation is encountered in elastic electronic surfaces[7] but not in displays. In this paper, we focus on the third and most-complicated regime where substrate and film have comparable strengths, *i.e.*, $Y_s \cdot d_s \approx Y_f \cdot d_f$. A commonly seen example is a thin inorganic device multilayer with a typical Y_f of ~200 GPa, deposited on a relatively thick organic polymer substrate with a typical Y_s of <5 GPa. Because of their comparable mechanical strengths, the film and substrate affect each other's strain, and can induce large and variable curvature $1/R$. The relationship between the curvature and the mismatch strain can be approximated by[8–12]

$$\frac{1}{R} = \frac{6\varepsilon_M(1+\nu)\overline{Y}_f\overline{Y}_s d_f d_s(d_f+d_s)}{(\overline{Y}_s d_s^2 - \overline{Y}_f d_f^2)^2 + 4\overline{Y}_f\overline{Y}_s d_f d_s(d_f+d_s)^2}. \quad (2)$$

Here $\overline{Y}_f$ and $\overline{Y}_s$ are the plane strain elastic moduli of the film and substrate and ν is the average value of Poisson's ratio of the film, ν_f, and the substrate, ν_s. If the substrate is initially curved with radius R_0, the curvature $1/R$ of Eq. (2) must be replaced by the effective curvature, $1/R - 1/R_0$. A sheet of polymer foil cut from a roll is usually curved.

3 Sources of mismatch strain

The total mismatch strain ε_M is composed mainly of (a) built-in strain, ε_0, (b) thermal mismatch strain, ε_{th}, and (c) moisture mismatch strain, ε_{ch}. These strain components add as described by the following equation:

$$\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch}. \quad (3)$$

The built-in strain ε_0 is produced by built-in stress, which arises from atoms deposited in out-of-equilibrium positions. It is a function of the material system and deposition conditions. For instance, the built-in strain tends to be tensile in Cr and compressive in a-Si, while it can vary from tensile to compressive in SiN_x when the deposition power increases,[13] as shown in Fig. 1.

The thermal mismatch strain, ε_{th}, is introduced by the coefficient of thermal expansion (CTE) mismatch between the film and the substrate. During a-Si:H TFT fabrication,

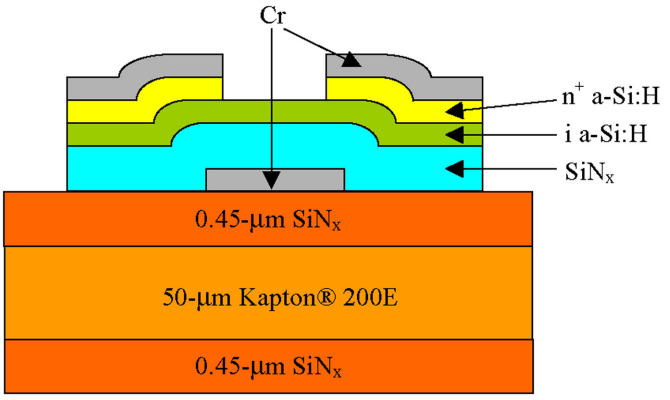


FIGURE 2 — Schematic cross section of a back-channel etched a-Si:H TFT on a passivated polyimide substrate.

most films are deposited at elevated temperature. The thermal mismatch strain produced by cooling down to room temperature is given by

$$\varepsilon_{th} = (\alpha_f - \alpha_s) \times (T_{dep} - T_{room}). \quad (4)$$

Typical inorganic semiconductor films have α_f ranging from 1 to 5 ppm/°C, and organic polymer substrates have α_s of 10–50 ppm/°C. This makes the thermal stress measured at room temperature in the device film always compressive.

We observe a moisture mismatch strain ε_{ch} in samples that had been dried completely by a vacuum bake before film deposition and were brought into the moist air after deposition. It is described by

$$\varepsilon_{ch} = -(\beta_f - \beta_s) \times \%RH, \quad (5)$$

where the β denotes the coefficient of humidity expansion (CHE) and *%RH* is the percent of relative humidity. In a structure of inorganic-film on organic-polymer substrate, ε_{ch} must be taken into consideration because the typical organic-polymer substrate has a β_s of a few ppm/*%RH*, while β_f of inorganic films is just about zero. In practice, the mismatch strain caused by moisture can be kept small by depositing inorganic barrier films on both faces of the organic polymer substrate as shown in Fig. 2. One function of these barrier films is to dramatically slow down moisture uptake by the polymer substrate.

Once the substrate material and process temperature have been selected, there is little opportunity for further control of thermal and humidity expansion. Therefore, we focused on controlling the built-in stress by adjusting deposition conditions. To do so, we first evaluated the built-in strain in structures of simple 300-nm-thick SiN_x films grown by plasma-enhanced chemical vapor deposition over a range of radio-frequency deposition power on one side of 50-µm-thick DuPont™ Kapton® 200E polyimide substrates. Because the built-in stress depends on the deposition power, various curvatures resulted, as shown in Fig. 3(a). From measurements of the effective radius of curvature, the total mismatch strain ε_M is obtained from Eq. (2). Then we calculated the components of ε_M and extracted ε_0, using Eqs.

(3)–(5) together with the material properties of Table 2. All contributions to Eq. (3) are plotted in Fig. 3(b). The built-in strain changes from tensile to compressive as the deposition power increases. The crossover deposition power for the transition in this particular case lies around 17 W (75 mW/cm^2).

4 Consequences of mismatch strain

Typical brittle inorganic films can be strained more in compression than in tension. For instance, a-Si:H films can be strained from ~–2% to ~+0.5%.[14] In tension, the films fail by crack propagation from pre-existing defects. In compression, a-Si:H fails by delamination coupled with buckling and fracture; to suppress this failure mode the film must be made to adhere well.[12] The film may crack during or after deposition. The main stress component during deposition is built-in stress. Whether or not the film cracks after deposition is determined by the total mismatch strain. To ensure crack-free devices, it is important to keep the built-in stress as well as the total mismatch stress below a critical value throughout the entire process.[12]

As long as the mismatch strain is kept below this critical value, the film will be crack-free, but the stress caused by mismatch strain still can make the sample curve. Varying curvature corresponds to varying size of the flattened sample. Thus, variation of the stress-induced curvature throughout the device process causes misalignment in overlay registration. Even though the stress-induced *curvature* can always be balanced to zero by applying a compensating layer on the backside of the substrate, this procedure changes the *size* of the sample. Hence, to ensure the dimensional stability of the work piece, the mismatch strain between the film stack and the substrate must be kept at a constant value for all photolithographic steps. This constant value is ensured when one specific value of the curvature 1/*R* of the free-standing work piece is maintained through all photolithographic steps. The most simple approach is to maintain this curvature at zero by keeping the structure flat.

TABLE 2 — Material properties used for the calculation of the built-in stress in SiN_x films on Kapton® E foil substrates.

	Kapton® E	SiN_x deposited at 150°C
Young's modulus	Y_s = 5.3 GPa	Y_f = 210 GPa
Poisson's ratio	ν_s = 0.32	ν_f = 0.25
Biaxial stress modulus $Y^* = \frac{Y}{1-\nu}$	Y_s^* = 7.8 GPa	Y_f^* = 280 GPa
Plane strain modulus $\bar{Y} = \frac{Y}{1-\nu^2}$	$\bar{Y}_s$ = 5.9 GPa	$\bar{Y}_f$ = 224 GPa
Coefficient of thermal expansion	α_s = 16 ppm/K	α_f = 2.7 ppm/K
Coefficient of humidity expansion	β_s = 8 ppm/%RH	β_f = 0 ppm/%RH
Initial radius of curvature of substrate	R_0 = 14.3 cm	

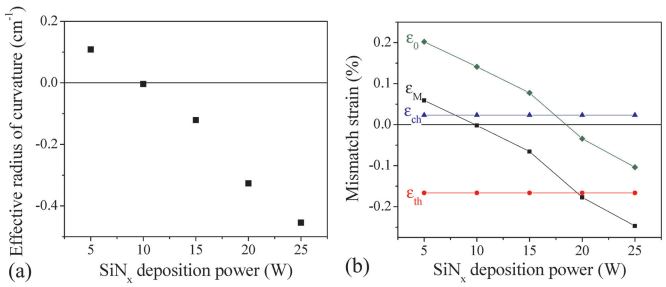


FIGURE 3 — (a) Effective radius of curvature caused by 300-nm PECVD SiN_x deposited at 150°C over a range of deposition power on 50-µm-thick Kapton® 200E polyimide substrates. The curvature was measured at room temperature and 29% relative humidity. The effective radius is the difference between the final sample curvature 1/*R* and the initial curvature of the bare substrate 1/R_0. (b) Components of the mismatch strain in the SiN_x films; ε_M denotes the total mismatch strain extracted from 1/*R*; calculated values of the thermal ε_{th} and humidity ε_{ch} mismatch strains are subtracted from it to arrive at the built-in strain ε_0. The horizontal line denotes zero strain. The film is in tension at positive strain and in compression at negative strain.

5 Experiments

We used a-Si:H TFTs on polyimide-foil substrates for demonstrating the control of overlay registration by adjusting the built-in stress in the SiN_x gate dielectric. The TFTs were fabricated in a non-self-aligned back-channel-etched geometry. We began by passivating the 50-µm-thick polyimide substrate on both sides with ~0.45-µm-thick PECVD SiN_x at 150°C. The SiN_x coat has several functions: it (i) provides reliable adhesion to the subsequent device layers, (ii) seals the substrate against process chemicals and against degassing of the substrate itself, (iii) serves as a barrier layer for the moisture to avoid dimensional change of the organic substrate due to uptake of moisture, and (iv) balances the stress-induced curvature of the sample through part of the process. Following substrate passivation, the TFT fabrication process was carried out on what was the concave side of the bare polyimide cut from the roll (Fig. 1). The device cross section is shown in Fig. 2. An ~80-nm-thick Cr film was sputtered at room temperature and wet etched to form the first device pattern, the bottom gate electrode. Next, a silicon stack, composed of (i) ~300-nm SiN_x gate dielectric, (ii) ~200-nm i a-Si:H channel layer, and (iii) ~50-nm n^+ a-Si:H source/drain layer, was deposited by PECVD, followed by ~80-nm-thick thermally evaporated Cr for the source/drain metal contact. The silicon stack was deposited from a gas mixtures of SiH_4 + NH_3 + H_2, SiH_4 + H_2, and SiH_4 + PH_3 for SiN_x, i a-Si:H, and n^+ a-Si:H, respectively, at a pressure of 500 mTorr (67 Pa) and a substrate temperature of 150°C. The thermal evaporation of Cr heated the substrate up to ~100°C, in the absence of temperature control. The source/drain pattern was then created by wet etching the Cr, followed by dry etching the n^+ a-Si:H in a gas mixture of CF_4 and O_2. In the final two steps, we dry etched

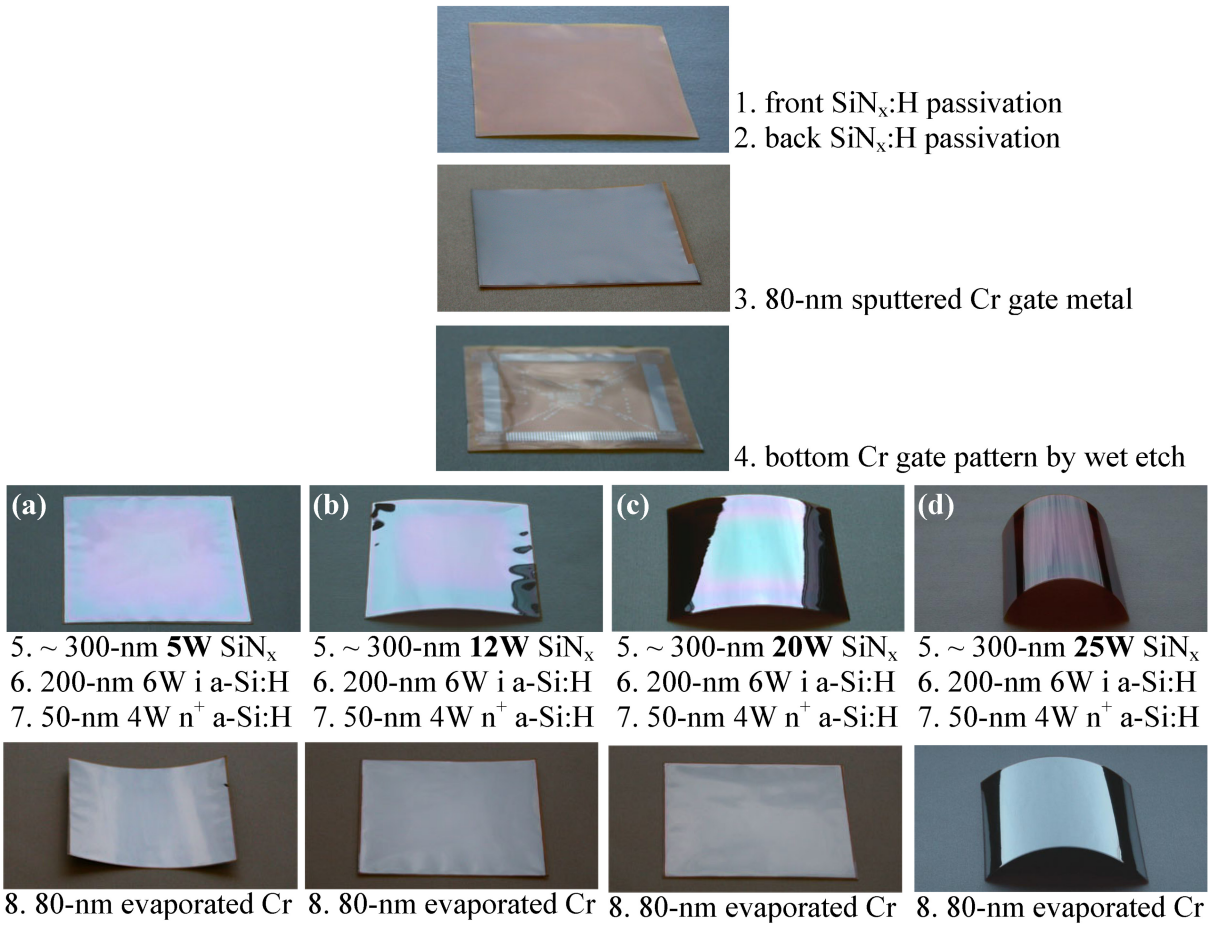


FIGURE 4 — Sample curvature variation in a-Si:H TFT fabrication between substrate passivation and evaporation of the top Cr source/drain contact metal. In all four samples all process steps are the same, except for the deposition power of the gate SiN_x, which was varied from 5 to 25 W.

the i a-Si:H to define the transistor island, and opened the window through the gate SiN_x to access the bottom-gate contact pad. The highest process temperature was 150°C, which is a compromise between obtaining satisfactory device performance while avoiding excessive CTE mismatch stress between the device films and the polyimide substrate. As described earlier, the samples were carried as nearly free-standing foils through most of the process steps; during film deposition and photolithography they were temporarily held flat.

We monitored the degree of misalignment between the first and second photolithography levels, *i.e.*, the bottom gate and the source/drain. Their alignment is crucial to setting source/gate and gate/drain overlaps. Between the two photolithographic steps falls the deposition of the silicon stack, composed of (i) SiN_x gate dielectric, (ii) i a-Si:H channel, (iii) n^+ a-Si:H source/drain, and (iv) Cr source/drain contact. To quantify the stress compensation, we kept all these layers the same, except for intentionally varying the built-in stress in the gate SiN_x from tensile to compressive. This we did by tuning the deposition power from low to high, 5, 12, 20, 25 W (22, 53, 89, 111 mW/cm^2), which results in an effective stress in the film stack ranging from highly tensile to highly compressive.

6 Results and discussion

The sample curvatures throughout the TFT process are illustrated in Fig. 4. To make the passivated substrate slightly convex prior to TFT fabrication, as shown in the top frame of Fig. 4, we grow intentionally slightly unsymmetric SiN_x passivation coats. Then the bottom Cr is sputtered on, which makes the sample flat for the first photolithography step. Etching the continuous Cr film into the small gate features releases the stress partially and the sample curves slightly. Next, the TFT stack is deposited, followed by thermal evaporation of Cr for the source/drain contacts. While the samples are pronouncedly convex or concave with 5- and 25-W SiN_x gate nitrides, they turn out nearly flat at 12 and 20 W. This indicates that the stresses within the device layers nearly compensate each other with the 12- and 20-W SiN_x. Because these 12- and 20-W samples are (nearly) flat after step 8 just as they were after step 3, they have (nearly) the same sizes after steps 3 and 8, and thus meet the requirement for accurate mask-overlay registration.

Figure 5 shows the corresponding mask overlays. At both the gate and source/drain levels, we aligned to a mark at the center of the substrate, and measured the misalignment of four marks, each lying on a corner of a 52 × 52 mm

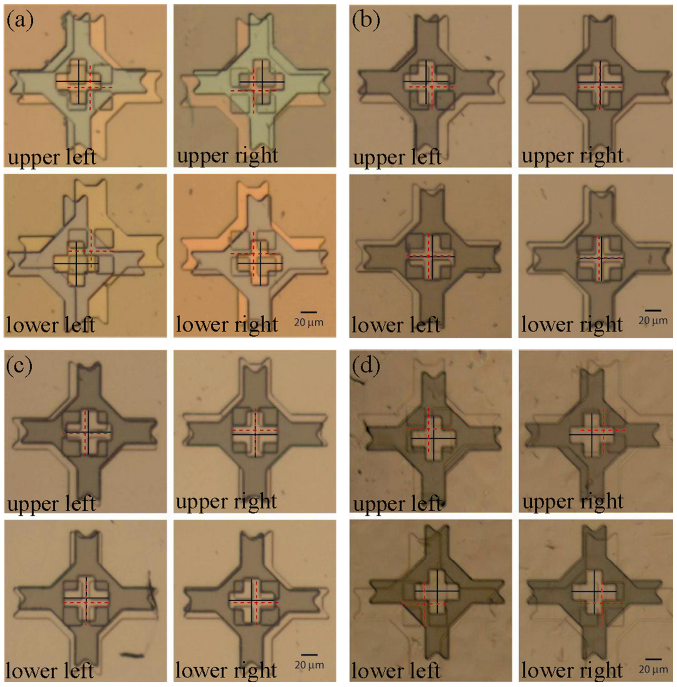


FIGURE 5 — Overlay misalignment between the first, bottom-gate, and second, source/drain, photolithography levels in the back-channel etched a-Si TFT process with (a) 5 W, (b) 12 W, (c) 20 W, and (d) 25 W gate SiN_x. The frames lie 52 mm apart near the corners of the 70-mm square substrate. The dashed red crosses mark the center at the gate level and the solid black crosses at the source/drain level. The sample is seen to shrink substantially with 5-W SiN_x, slightly with 12-W SiN_x, expand somewhat with 20-W SiN_x, and substantially with 25-W SiN_x. Note the correspondence with the curvatures after step 8 of Fig. 4.

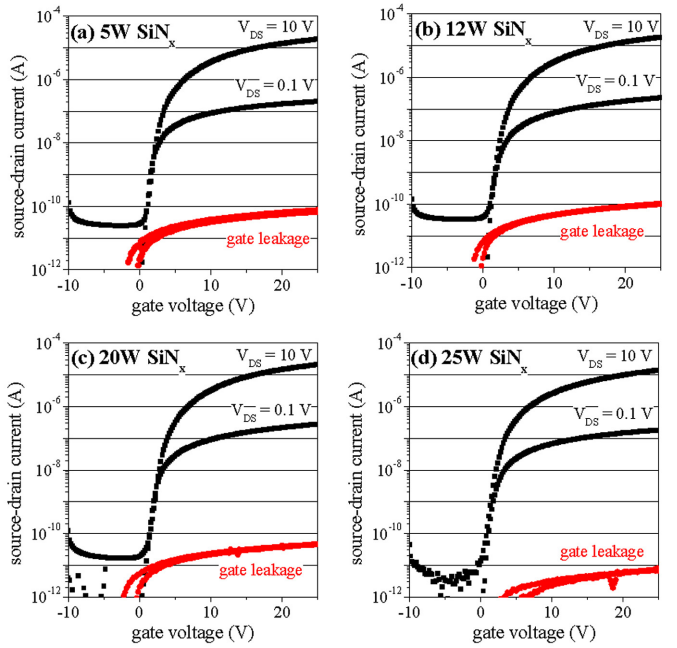


FIGURE 6 — Transfer characteristics of TFTs with 300-nm-thick (a) 5-W, (b) 12-W, (c) 20-W, and (d) 25-W gate SiN_x. The TFT gates are 80 μm wide and 10 μm long. The OFF and gate leakage currents are instrument-limited shunt values. No significant change is observed with SiN_x deposition power. The slight drop of the ON current with 25-W gate SiN_x may result from a reduction of the tensile strain in the TFT.

square (the overall substrate size is 70 × 70 mm). The dashed red crosses mark the center at the first photolithography level, for the gate, and the solid black crosses at the second photolithography level, for source/drain. The sample is seen to greatly shrink with a 5-W gate SiN_x, shrink slightly at 12 W, expand slightly at 20 W, and expand substantially at 25 W.

The TFT transfer characteristics of Fig. 6 show that varying the deposition power has a negligible effect on the electrical performance of as-fabricated TFTs. The slight drop of the ON current in the TFT with the 25-W gate SiN_x may result from the mobility reduction caused by the reduction of tensile strain in the TFT.[15] If, after accelerated stress tests or extended operation, the TFT performance likewise is found not to differ from that of standard TFTs, adjusting the built-in stress in the gate SiN_x may become a useful technique for improving the mask-overlay registration. This method would be valuable in the fabrication of a-Si:H TFT circuits on free-standing organic-polymer-foil substrates.

7 Summary

Careful management of the dimensions of the work piece is essential to fabricating a-Si:H TFTs on substrate foils of compliant organic polymers. Mismatch strain between the films and substrate can cause mismatch-stress-induced device fracture, and/or curvature that varies throughout the process. Because varying curvature corresponds to varying size of the flattened work piece, the curvature at the photolithographic steps must be made identical, and preferably zero. The size or curvature at specific process steps can be made identical by adjusting the built-in stress in a device layer. One example is the adjustment of stress in the SiN_x gate dielectric by variation of the rf deposition power. This variation has no significant influence on the electrical performance of as-fabricated a-Si:H TFTs. If no deviation from standard TFT performance is detected after long-term operation, stress control in a device layer could become a practical technique for improving overlay registration.

Acknowledgments

We would like to thank Prof. Zhigang Suo and Teng Li of Harvard University for their help with thin-film mechanics, Dr. Helena Gleskova for valuable discussions, and the New Jersey Commission for Science and Technology and DuPont Company for support.

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