Ultrathin Strained-SOI by Stress Balance on Compliant Substrates and FET Performance

Haizhou Yin, *Member, IEEE*, Karl D. Hobart, *Member, IEEE*, Rebecca L. Peterson, *Student Member, IEEE*, F. J. Kub, and James C. Sturm, *Fellow, IEEE*

***Abstract*—Ultrathin, strained-silicon-on-insulator (s-SOI) structures without a residual silicon-germanium (SiGe) underlayer have been fabricated using stress balance of bi-layer structures on compliant borophosphorosilicate glass (BPSG). The bi-layer structure consisted of SiGe and silicon films, which were initially pseudomorphically grown on a silicon substrate and then transferred onto BPSG by a wafer bonding and SmartCut[1] process. The viscous flow of the BPSG during a high-temperature anneal then allowed the SiGe/Si bi-layer to laterally coherently expand to reach stress balance, creating tensile strain in the silicon film. No dislocations are required for the process, making it a promising approach for achieving high-quality strained-silicon for device applications. To prevent the diffusion of boron and phosphorus into the silicon from the BPSG, a thin nitride film was inserted between the bi-layer and BPSG to act as a diffusion barrier, so that a lightly doped, sub-10-nm s-SOI layer (0.73% strain) was demonstrated. N-channel MOSFETs fabricated in a 25-nm silicon layer with 0.6% strain showed a mobility enhancement of 50%.**

***Index Terms*—Compliant substrate, SiGe, silicon-on-insulator (SOI), strained-Si.**

I. Introduction

THE enhancement of electron mobility has been well established in tensile-strained[2] silicon, drawing much attention for its application in high-performance CMOS [1]. Ultrathin silicon-on-insulator (SOI) has long been known for its superior properties over bulk silicon for MOSFETs, such as reduced FET parasitic capacitance, lower leakage current, and reduced short-channel effects (SCEs) [2]. In addition, ultrathin SOI structures also allow the fabrication of multigate devices [3]. Therefore, the combination of strained-silicon and SOI offers a promising opportunity for device performance improvement.

Manuscript received December 8, 2004; revised May 16, 2005. This work was supported by the Defense Advanced Research Projects Agency (DARPA) under Grant N66001-00-10-8957 and the Army Research Office (ARO) under Grant DAAG55-98-1-0270. The review of this paper was arranged by Editor T. Skotnicki.

H. Yin is with the Princeton Institute for the Science and Technology of Materials and the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA, and also with IBM, Hopewell Junction, NY USA.

K. D. Hobart and F. J. Kub are with the Naval Research Laboratory, Washington, DC 20375 USA.

R. L. Peterson and J. C. Sturm are with the Princeton Institute for the Science and Technology of Materials and the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA.

Digital Object Identifier 10.1109/TED.2005.856185

[1]SmartCut is a trademark of SOITEC.

[2]Strain is commonly expressed as a dimensionless number: the fractional change in the length of a solid in a given direction. This is also expressed in terms of a percentage—e.g. an absolute strain level of 0.1 (fractional length expansion) is the same as a strain of 10%.

There have been numerous efforts to date towards achieving strained ultrathin SOI. The first type of approach involves the formation of relaxed $Si_{1-x}Ge_x$ on insulator (SGOI) followed by epitaxial Si regrowth [4], [5]. However, the thickness of the combined layers usually exceeds 100 nm, which is too thick to suppress SCE. Furthermore, the presence of SiGe can cause process technology problems, such as the diffusion of germanium to the gate oxide interface, difficulty in forming low-resistance silicides and altered dopant diffusion compared to that in silicon [6]. Therefore, a strained-silicon-on-insulator (s-SOI) structure without SiGe is very attractive. The usual approach to such SiGe-free layers involves transferring strained-silicon grown on relaxed, compositionally graded SiGe buffers directly onto silicon dioxide, followed by the removal of the transferred SiGe buffer [7]–[10]. In all of these approaches, the quality of the strained-silicon depends on the quality of the original relaxed SiGe buffer layers, which is limited in practice by a threading defect density of $\sim 10^5$ cm^{-2} [11]. Furthermore, these relaxed buffer layers in practice require thick epitaxial graded layers and chemical–mechanical polishing (CMP) steps to overcome roughening [12].

In this paper, a novel approach based on stress balance on compliant, insulating borophosphorosilicate glass (BPSG) was used to achieve ultrathin s-SOI without the presence of SiGe in the final structure [13]. No dislocations or lattice-mismatched epitaxial growth are required in the process, so that in principle this method should be capable of extremely low defect density. It also involves the growth of only very thin (tens of nanometers) epitaxial layers, which should minimize the cost of the epitaxial processes. The final strained SOI thickness ranged from 10 to 30 nm, which enabled the fabrication of fully depleted strained-Si n-channel MOSFETs. The work is based on our previous studies of the strain relaxation of SiGe and SiGe/Si structures on BPSG [14]–[17], which demonstrated how the lateral expansion of strained layer islands transferred to BPSG could be used to relieve the strain in those layers, and how stresses are balanced in multilayer structures on the BPSG. This paper reports details of device fabrication and characterization beyond the previous paper [13]. The earlier paper presented only device results using a very thick deposited gate oxide ($\sim$300 nm). In this paper, the gate oxide thickness is scaled down by more than one order of magnitude. This paper shows more complete device analysis: subthreshold slope, control of back gate, etc.

II. Fabrication and Structure Characterization

A. Fabrication of SiGe/Si Bilayers on BPSG

The first part of the strained-silicon on BPSG process was the creation of strained-$Si_{0.7}Ge_{0.3}$/unstrained Si bilayers on

0018-9383/$20.00 © 2005 IEEE

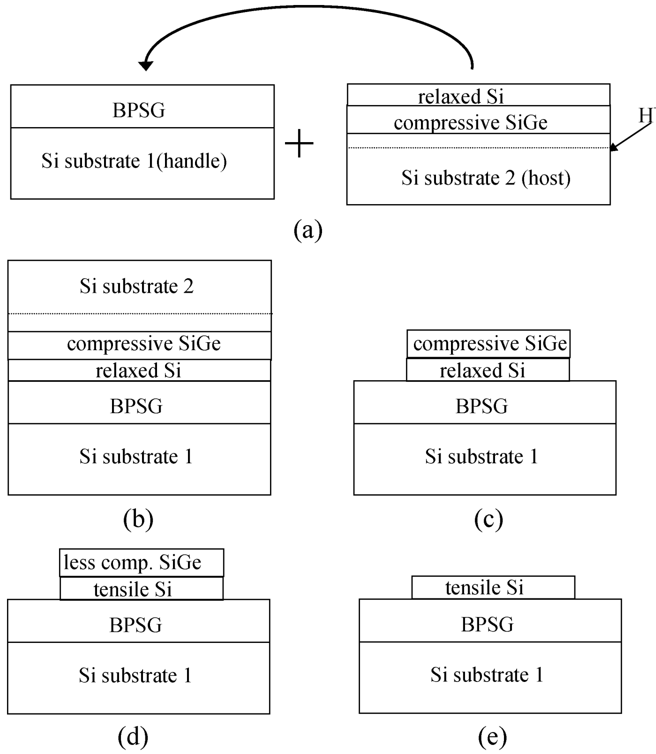


Fig. 1. Process flow of fabricating strained-silicon on BPSG. (a) Handle wafer is coated with BPSG, deposited by CVD, and the sacrificial host wafer has epitaxial Si/SiGe layers grown by CVD and is implanted with hydrogen ions. (b) SiGe/Si layers are transferred onto BPSG by wafer-bonding, cleaving at the H-implant depth, and selective etching to remove residual silicon. (c) SiGe/Si layers are patterned into islands to allow lateral expansion. (d) During high-temperature annealing, the SiGe/Si layers expand coherently, with the SiGe becoming less compressively strained and the silicon becomes tensilely strained. (e) Top SiGe layer is selectively removed by wet etching.

BPSG using a sacrificial "host" wafer and a "handle" wafer. The basic fabrication process is based on that of [17], which created relaxed SiGe layers on BPSG (without strained-silicon). In this paper, a 30-nm commensurately strained-$Si_{0.7}Ge_{0.3}$ layer and a 25-nm silicon epitaxial layer were grown on the surface of the sacrificial host Si(100) wafer [Fig. 1(a)]. The handle silicon wafer was coated with 200-nm BPSG (4.4% B and 4.1% P by weight) by chemical vapor deposition (CVD) [Fig. 1(a)]. The boron and phosphorus content in the BPSG were chosen to minimize its viscosity at elevated temperature [18]. The host wafer was implanted with H_2^+ (180 keV and dose of 4.5×10^{16} cm^{-2}). Both wafers were cleaned using a carbon dioxide "snow jet" to remove dust and ultra-violet ozone to remove organic residue. The wafers were then treated in $NH_4OH{:}H_2O_2 : H_2O : (1:1:4)$ and $HCl{:}H_2O_2 : H_2O : (1:1:4)$ to create hydrophilic surface and bonded at room temperature. The bonded wafers were annealed at 250 °C for four hours to enhance bond strength and then at 550 °C in nitrogen to separate the top layer from the host substrate at the depth of the hydrogen implant (800 nm) [Fig. 1(b)]. The remaining structure of Si/SiGe/Si/BPSG on silicon was dipped into an aqueous KOH solution (10% by weight) at 80 °C to selectively remove the approximately 800-nm silicon remaining on top of the SiGe after the splitting process. In one case, prior to layer transfer, a 5-nm Si_3N_4 layer was deposited on top of the silicon film on the sacrificial wafer at 725 °C using low-pressure CVD (LP-CVD) before bonding. The continuous SiGe/Si film was patterned into square islands of various edge sizes (from 10 to 200 μm) by reactive ion etching (RIE) in a SF_6/O_2 mixture [Fig. 1(c)]. The islands are critical to prevent buckling of the thin films during subsequent annealing to soften the BPSG and allow lateral expansion of the islands [15], [16].

The strain in SiGe and Si films was locally measured with an accuracy of $+/-0.07\%$ by micro-Raman spectroscopy, using an Ar^+ laser (514.5 nm) focused to a spot of 3 μm [15]. Atomic force microscopy (AFM) was utilized to determine the surface roughness of samples. The thickness of the thin SiGe and Si films on BPSG was measured using spectroscopic reflectometry, which had a repeatability of $\sim$1 nm.

B. Stress Balance and Strain in the Silicon

The SiGe/Si square islands on BPSG after layer transfer and the island patterning retained their original strain levels (biaxial-compressive strain in the SiGe film and zero strain in the Si film). This is because at temperatures below 600 °C, the BPSG does not flow, and thus provides a constraining force to support the compressive strain in the SiGe film [Fig. 1(c)]. During high temperature anneals (usually around 800 °C in our work) the BPSG was becomes soft or viscous and can flow. This removes the constraining force of the BPSG, effectively leading to a free-standing SiGe/Si bilayer. The compressive stress in the SiGe film then drives the film to expand laterally [Fig. 1(d)]. The lateral expansion occurs first at the edges of the island and then propagates from the edge to reach the center [15].

If there were no Si in the island structure, the SiGe would laterally expand to relieve all strain in the layer [17]. Earlier work on SiGe/Si bi-layer structures on BPSG (with the Si under the SiGe) has shown that the two layers remain coherent during the relaxation, i.e., there is no slippage between the Si and SiGe or formation of misfit dislocations between them [14]. The bottom silicon film expanded along with the SiGe film, leading to tension in the silicon layer in this case. The coherent interface by definition implies an identical strain change $(\Delta\varepsilon)$ in the silicon and SiGe films

$$\Delta\varepsilon_{\mathrm{SiGe}} = \Delta\varepsilon_{\mathrm{Si}}. \tag{1}$$

The lateral expansion process will stop when the compressive stress in the SiGe film is balanced by the tensile stress in the Si film (i.e., a stress balance condition)

$$\sigma_{\mathrm{SiGe}} h_{\mathrm{SiGe}} + \sigma_{\mathrm{Si}} h_{\mathrm{Si}} = 0 \tag{2}$$

where σ represents film stress under equal biaxial stresses $(\sigma_{11} = \sigma_{22} = \sigma)$ and h refers to film thickness. By combining (1) and (2), along with the initial strain of zero in the Si film, one can express the final tensile strain in the silicon film $(\varepsilon_{\mathrm{Si,final}})$ upon stress balance to be related to the initial SiGe strain (ε_0)

$$\varepsilon_{\mathrm{Si,final}} = -\varepsilon_0 \frac{(1-\nu_{\mathrm{Si}})E_{\mathrm{SiGe}}h_{\mathrm{SiGe}}}{(1-\nu_{\mathrm{Si}})E_{\mathrm{SiGe}}h_{\mathrm{SiGe}} + (1-\nu_{\mathrm{SiGe}})E_{\mathrm{Si}}h_{\mathrm{Si}}} \tag{3}$$

where E and ν refer to the films' Young's Modulus and Possion's ratio, respectively. The magnitude of the tensile strain created in the silicon film depends on the original strain in the

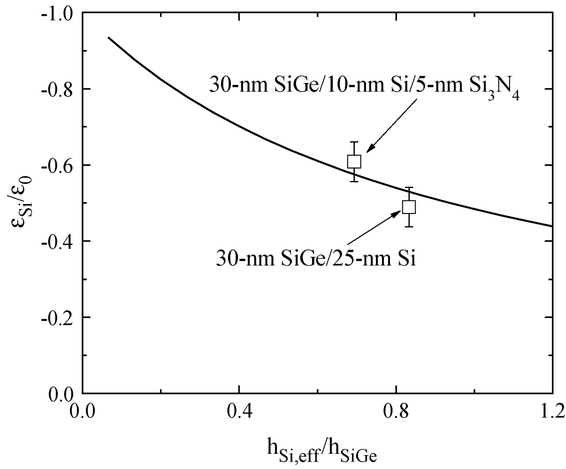


Fig. 2. Ratio of the final strain in the silicon after stress balance to that in the initial SiGe layer as a function of the ratio of the effective silicon thickness to that of the SiGe layer. Data points for 30-nm SiGe/25-nm Si and 30-nm SiGe/10-nm Si/5-nm Si_3N_4 are also given. Young's moduli of 13.0×10^{10} and $12.2 \times 10^{10} N/m^2$ for Si and $Si_{0.7}Ge_{0.3}$ were assumed, respectively. The solid line is from (3).

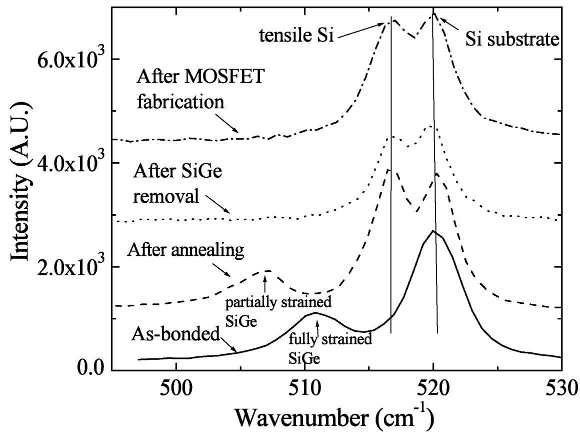


Fig. 3. Raman spectra measured at the center of a 90×90 μm^2 island at various stages of processing. The annealing reduced the compressive strain in the SiGe and added tension in the Si. The absence of a SiGe Raman peak after the SiGe etch confirms the complete removal of the SiGe. The FET process does not alter the strain in the silicon.

SiGe and thicknesses of the SiGe and silicon films. A thick SiGe film compared to the silicon layer and one with high strain (i.e., high germanium content) leads to a large tensile strain in the silicon film (Fig. 2). However, the thickness and germanium content one can use in the SiGe film are limited by the equilibrium critical thickness from its original growth on silicon [19], beyond which the strain in the SiGe film may be released by dislocations. While the 30-nm $Si_{0.7}Ge_{0.3}$ film used here below the metastable critical thickness [20], it is above the equilibrium critical thickness (8 nm). Therefore, achieving the maximum strain in the silicon requires the silicon be kept well under 30 nm.

Raman spectra collected after the layer transfer (solid line) and after stress balance (dashed line) at the center of a 90-micrometer island annealed at 800 °C are plotted in Fig. 3. The remaining silicon substrate was removed after layer transfer. It has no interference on the Raman measurement. After the layer transfer, the silicon film remained unstrained and its Raman peak overlaid with that of the silicon substrate. When stress balance was

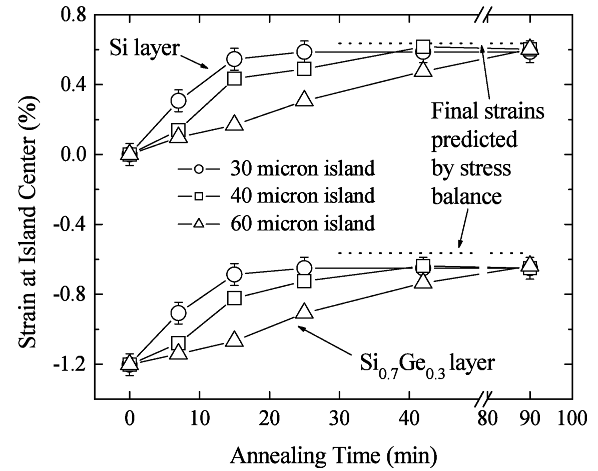


Fig. 4. Biaxial strain (from micro-Raman spectroscopy) of 30-nm $Si_{0.7}Ge_{0.3}$ and 25-nm Si films at the center of square islands as a function of annealing time at 800 °C, showing the evolution of strain in the silicon and SiGe films. Dashed lines are calculations of the final stress balance condition.

reached, the Raman peak from the 25-nm silicon film shifted to a smaller wavenumber, indicating a tensile strain. At the same time, the Raman peak from the SiGe film also moved to a smaller wavenumber due to a reduction in the compressive strain.

The generation of tensile strain in the silicon film as Si/SiGe island expands at 800 °C is shown in Fig. 4. The edge sizes of the SiGe/Si square islands range from 30 to 60 μm. All of the strain data were collected at center of the islands by Raman scattering. Also shown in Fig. 4 (as dotted lines) are the final strain values predicted based on the stress balance, which are indeed in good agreement with the final measured strain levels. The dotted lines are equivalent to the strain ratio of 0.52 (magnitude of final silicon strain to initial SiGe strain) shown on Fig. 2. As the compressive strain in the SiGe film decreased from 1.2% to 0.6%, the tensile strain in the silicon film increased from zero to about 0.6% at the same rate. Further, as expected, the relaxation of large islands is slower than that of small islands (Fig. 4), but 90 min at 800 °C was sufficient to reach the final stress balance condition for all island sizes.

Once the silicon film was strained, the top SiGe film had served its purpose, and then was removed to produce strained SOI layer without SiGe [Fig. 1(e)]. Because the silicon film (25 nm) was thin compared to the SiGe (30 nm), a selective SiGe etch was used to remove the top SiGe film. A solution consisting of $HF(6\%)$: $H_2O_2(30\%)$: $CH_3COOH(99.8\%)$:(1:2:3), chosen for its good selectivity (>30) and fast SiGe etch rate, was used at room temperature. The solution is known to vary over time [21], so its etch properties were measured as a function of storage time (Fig. 5). The SiGe etch rate nearly doubled after three weeks, but the selectivity did not degrade and remained better than 30. Also no dependence of the etch rate on strain was observed for SiGe. With the good etch selectivity, the over-etch of the Si during the SiGe removal process was kept under 1 nm. The disappearance of the SiGe Raman peak after the SiGe etch indicates that all SiGe was removed (Fig. 3). The strained Si film was very smooth after the SiGe etch with a RMS roughness of only 0.18 nm across an area of 10 μm × 10 μm. The measured RMS roughness on a bare silicon wafer is smaller than 0.10 nm. There was no evidence

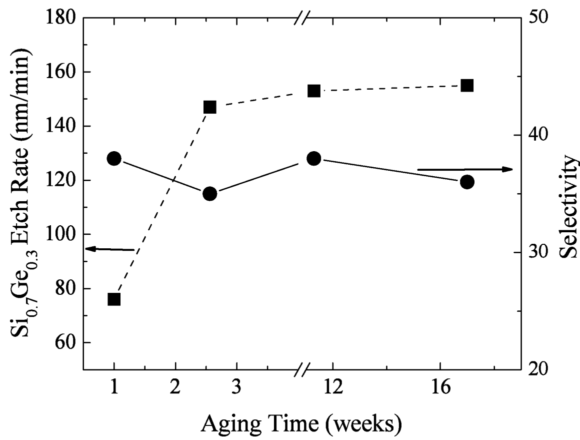


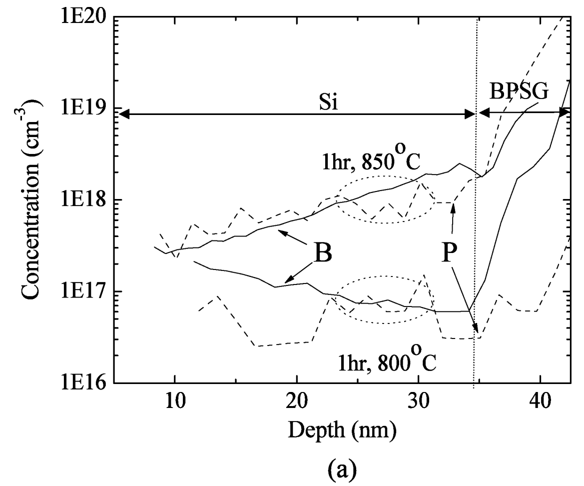
Fig. 5. Effect of aging on the SiGe etch rate and the selectivity relative to silicon of a buffered $HF : H_2O_2 : CH_3COOH$ etch. The etch rate stabilizes after two weeks.

of "crosshatching", as sometimes seen in conventional relaxed SiGe/strained Si films with misfit dislocations, or any other defects over an area of 11 μm × 11 μm. The crosshatching should not be expected. The elastic expansion allows the strain in SiGe to be released without misfit dislocations. The defect density in the 25-nm silicon layer was not directly measured. By defect etching (0.3 mol of CrO_3 : 49% HF at a 5:4 volume ratio) we measured no defects in relaxed $Si_{0.7}Ge_{0.3}$ 30 μm × 30 μm islands (without a silicon layer), to give an upper limit to defect density of $\sim 10^5$ cm^{-2}. In contrast, defect etching of 90-nm $Si_{0.7}Ge_{0.3}$ grown directly on Si(100) (over critical thickness) shows enormous density of defects ($\gg 10^8$ cm^{-2}) after similar etching, confirming the etch could delineate defects.

In principle, one might also expect the bilayer structures to curl during annealing, with the edges going down and the island center up due to the compressive strain in the top SiGe and tensile strain in the lower silicon layer. This effect was not observed, however, perhaps because this involves flow of BPSG at the island scale and thus requires much longer annealing time.

C. Suppression of Dopant Diffusion From BPSG

Our work requires a (800–850 °C) high-temperature anneal to soften the BPSG to allow its viscous flow. The BPSG viscosity can be reduced by a factor of five when annealing temperature is elevated from 800 °C to 850 °C [15], which effectively speeds up the island relaxation (to create strain in the silicon) by a factor of five, allowing strain generation in large islands (200 μm) within a reasonable time frame (<5 hrs) (a lower viscosity indicates films can more easily flow). However, the anneals could result in the diffusion of boron and phosphorus from BPSG into the silicon film. Fig. 6(a) shows the doping profile, measured using Secondary Ion Mass Spectroscopy (SIMS), in a thin silicon layer on BPSG after 1 h annealing at 800 °C and 850 °C, respectively. Little diffusion was seen after an 800 °C anneal. The cause of the rise of boron signal near the top surface after 800 °C annealing is not known. It may be from surface contamination due to poor cleaning before annealing or from the original epitaxial growth. The 850 °C anneal caused considerable boron and phosphorus diffusion into the silicon film, with doping levels $\sim 10^{18}$ cm^{-3} in the silicon. Because silicon nitride layers are known dopant barriers [22], a thin (~5 nm) silicon nitride layer was deposited on top of a 10-nm



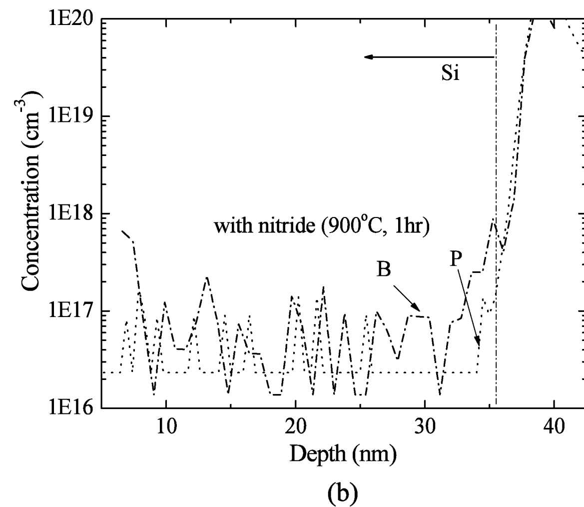


Fig. 6. Doping concentration vs depth in the Si film on BPSG after annealing. The vertical line denotes the Si/BPSG interface. (a) Samples without a nitride layer annealed for 1 h at 800 °C or 850 °C and (b) sample with a 5-nm nitride layer between the BPSG and silicon to block dopant diffusion, annealed at 900 °C for 1 h.

Si/30-nm $Si_{0.7}Ge_{0.3}$ structure using LP-CVD at 725 °C prior to the layer transfer. The tri-layer structure (Si_3N_4/Si/SiGe) was then transferred onto BPSG, sandwiching the nitride layer between the BPSG and SiGe/Si. The structure was annealed at 900 °C for 1 h to test the barrier against dopant diffusion. The boron and phosphorus levels in the silicon layer were now below the SIMS detection limit (5×10^{16} cm^{-3}) [Fig. 6(b)], indicating the effectiveness of the thin barrier.

Since the silicon nitride film is elastic, the SiGe layer would stretch the nitride layer along with the Si layer, potentially generating a smaller strain level than the nitride-free structure. In the stress balance relationship, the silicon nitride contributes thus to an effectively thicker silicon layer. This is why the silicon nitride layer was kept so thin. In this case, the silicon thickness in (3) should be replaced by an effective silicon thickness $h_{Si,eff}$

$$h_{Si,eff} = h_{Si} + \frac{E_{Si_3N_4}(1-\nu_{Si})}{E_{Si}(1-\nu_{Si_3N_4})} h_{Si_3N_4} \tag{4}$$

To investigate this effect, the tri-layer structure was patterned into islands and then annealed to reach stress balance. Fig. 7 shows the Raman spectra taken before and after annealing.

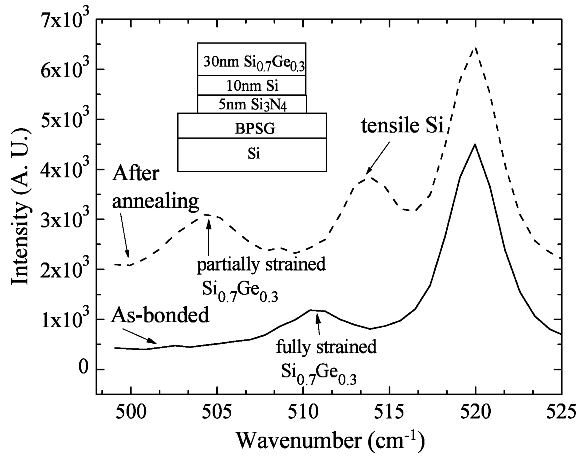


Fig. 7. Raman spectra measured at the center of a 30 μm × 30 μm island (30 nm-SiGe/10 nm-Si/5-nm-Si_3N_4/1 μm-BPSG) after annealing at 800 °C for 30 min. The Si layer was still stretched by compressive SiGe even when the Si_3N_4 layer was present.

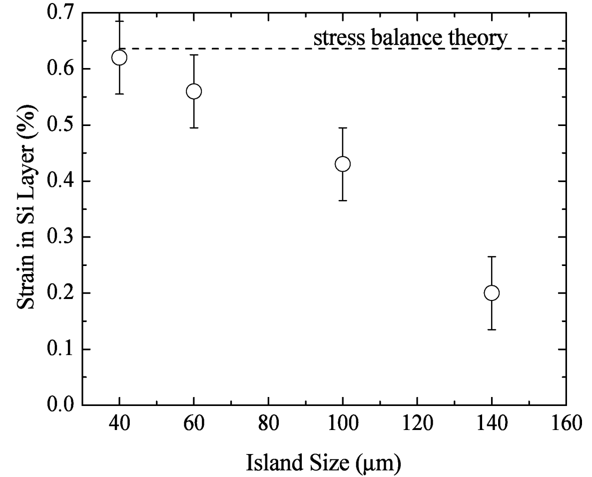


Fig. 8. Island-size dependence of the silicon strain, measured at island center, in 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si on 200-nm BPSG after 1 h annealing at 800 °C.

The strain level in the silicon film is 0.73%, even higher than the strain (∼0.6%) obtained in the nitride-free 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si sample. The higher strain stems from the much thinner (10 nm) Si layer used in the sample with a nitride layer. When the silicon nitride layer is accounted for as an effective silicon layer, the final strain in the 10-nm silicon film is in line with stress balance prediction (Fig. 2), which shows that the strain is 0.75% when there is a 5 nm nitride layer. The expected strain would have been much higher (0.89%) if the silicon nitride layer had not been considered. The excellent dopant diffusion suppression of the 5-nm nitride film discussed above suggests that an even thinner silicon nitride layer can be used to suppress diffusion and allow more strain in the silicon.

III. Device Fabrication and Characteristics

A. Device Fabrication

Self-aligned long-channel n-channel MOSFETs were fabricated using the strained-silicon film, obtained from the 30-nm $Si_{0.7}Ge_{0.3}$/25-nm Si on 200-nm BPSG (as described in the previous section), for the device channel. In this case, the nitride barrier layer from the previous section was not used. The SiGe/Si bi-layer was annealed for 1 h at 800 °C and the generated strain level in the silicon varied with island size (Fig. 8). The silicon strain was negligible in islands larger than 200 μm due to the slow lateral relaxation of large islands. For a fair comparison, the control (unstrained) devices were fabricated on the same sample using islands larger than 3 mm, where strain in the silicon layer was nearly zero. (Note smaller unstrained-silicon islands could be realized at the cost of an extra masking step by removing the SiGe layer in the desired islands before the annealing, so that there would be no driving force for the silicon to expand [13]). The gate stack was comprised of tetraethylorthosilicate (TEOS) oxide and poly silicon, both deposited at 625 °C using low-pressure chemical vapor deposition (LP-CVD). Two gate oxide thicknesses (26 and 300 nm) were used. The deposited TEOS oxide was used instead of thermal oxide to avoid any change in the strain in the thin silicon layer resulting from the softening of the BPSG at the oxidation temperature. (Simple relaxation would reduce the tensile strain in the silicon, and compressive stress in the gate oxide from thermal oxidation might lead to an increase in the tensile strain.) Phosphorous implantation (35 keV, 1×10^{15} cm^{-2}) was used to dope the source/drain and the gate poly. A blanket layer of 300-nm low-temperature PE-CVD SiO_2 was deposited prior to a 1 h implant anneal at 800 °C. The thick stack on top of the channel, consisting of PE-CVD SiO_2, gate poly, and TEOS gate dielectric, helped to retain the strain in the channel during the 800 °C anneal, during which the underlying BPSG was viscous. After device fabrication, Raman spectroscopy was performed on a device channel $(L = 10\ \mu m)$ after removing the gate polysilicon. No change in the silicon strain was observed during the device processing (Fig. 3). Based on the SIMS of other samples annealed at 800 °C [Fig. 6(a)], the doping level in the nominally "undoped" channel is expected to be less than 2×10^{17} cm^{-3}.

B. Device Results

1) Threshold Voltage and Subthreshold Swing: Both strained and unstrained n-channel MOSFETs were well behaved with strained devices exhibiting much higher drive current (Fig. 9) than the unstrained control devices on the same substrate. The buried BPSG serves as a backgate dielectrics and the voltage applied to the substrate can also modulate the carriers in the channel. Fig. 10 depicts the transfer characteristics of a strained device with 26-nm TEOS gate dielectric at different substrate biases. The substrate bias not only changed the threshold voltage, but also affected the subthreshold swing. Fig. 11 plots the dependence of the top-gate threshold voltage on the applied voltage on the silicon substrate. The threshold voltage was extracted by linearly extrapolating drain current versus gate-source bias to the x-axis intercept for a fixed drain-source voltage of 0.01 V. The threshold voltage is similar in both strained and unstrained devices. The linear dependence of the threshold voltage on the applied voltage on the substrate indicates the devices operate at the fully depleted mode [2], which is consistent with the thin silicon channel (∼25 nm) used here. We attribute the large negative threshold voltage (−32

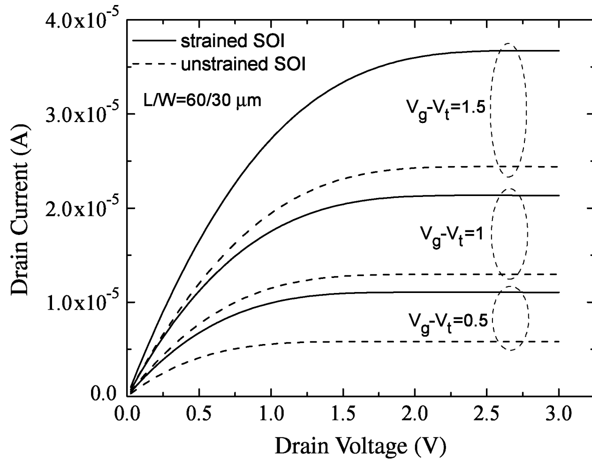


Fig. 9. Output characteristic of FETs in 25-nm Si on BPSG with strain levels of 0.56% and zero (control device). Channel width and length were 60 μm and 30 μm, respectively, and the substrate-source bias was -15 V.

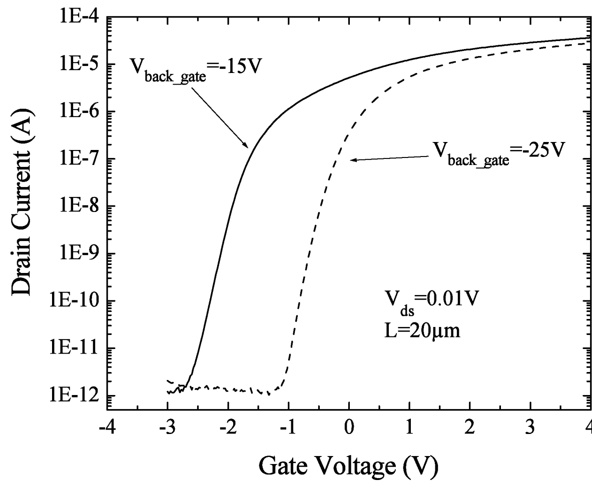


Fig. 10. Drain current as a function of gate voltage measured on a strained device ($\varepsilon = 0.56\%$) at different substrate-source biases. Drain bias was 0.01 V. Channel length and width were 20 μm and 280 μm, respectively.

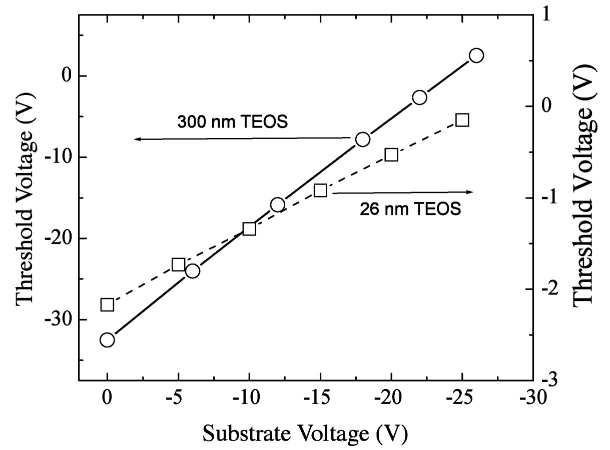


Fig. 11. Substrate-bias dependence of top-gate threshold voltage, measured on strained NFETs for gate oxide thickness of 300 nm (left vertical axis) and 26 nm (right vertical axis). The linear dependence shows that the devices operate in the fully depleted mode.

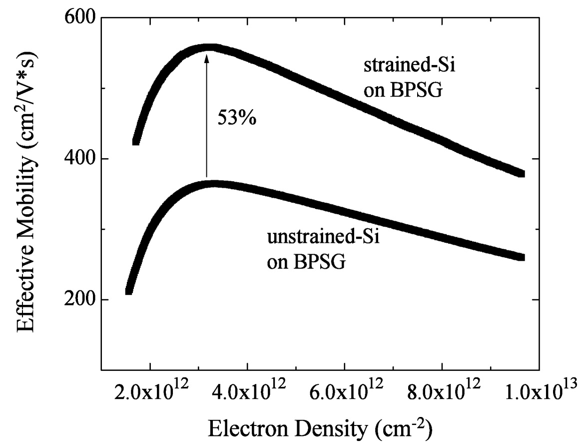


Fig. 12. Dependence of the enhancement of effective electron mobility on carrier density, where enhancement is defined as the ratio of mobility in devices fabricated on 60-μm islands ($\varepsilon = 0.56\%$) to that in devices with zero strain on BPSG.

V for 300-nm TEOS and -2.1 V for 26-nm TEOS) when the substrate was grounded to a high density of positive interface charges at the bonding interface between the strained-silicon and the BPSG layers, estimated to be $\sim 2 \times 10^{12}$ cm^{-2}. In n-channel FETs with 300-nm TEOS gate oxide fabricated on bulk silicon substrates, the threshold voltage is 2.7 V, which indicates that the TEOS oxide is not the cause of the large negative threshold voltage observed in devices fabricated on BPSG.

Strained and unstrained devices have similar subthreshold characteristics, with the best subthreshold swing of about 130 mV/dec for substrate bias more negative than -15 V. This is worse than the expected slope of near 60 mV/dec for FETs in fully depleted thin SOI films [2], We feel this degradation also stems from the poor electrical properties of the bonded interface, since a high interface-state density adds to parasitic capacitance and reduces the gate control over the channel region [23]. An interface of silicon and thermal silicon dioxide should have superior quality to that of Si/BPSG. One might try to overcome the poor Si/BPSG interface by a modification of the bonding process: forming a thin thermal silicon dioxide on the silicon prior to the wafer bonding.

2) Mobility Enhancement: As shown in Fig. 9, the strained-silicon devices exhibited enhanced current due to a higher mobility. The effective electron mobility was extracted from the drain current $I_{\rm DS}$ in the linear regime:

$$I_{\rm DS} = \left(\frac{W}{L}\right) \mu_{\rm eff} Q V_{\rm DS} \tag{5}$$

where Q is the carrier concentration and $V_{\rm DS} = 10$ mV. The $V_{\rm GS}$ dependence of the gate-to-channel capacitance was measured and was integrated to obtain the carrier concentration Q [24]. In the linear regime, the change in the surface potential across the channel can be ignored. Fig. 12 shows the measured effective electron mobility as a function of carrier concentration for both strained and unstrained FETs on BPSG with same long-channel device geometry, with a substrate bias of -15 V. The peak mobility enhancement was about 53%. The mobility enhancement was lower in devices fabricated on larger islands as a result of lower strain on larger islands. On 140-μm islands,

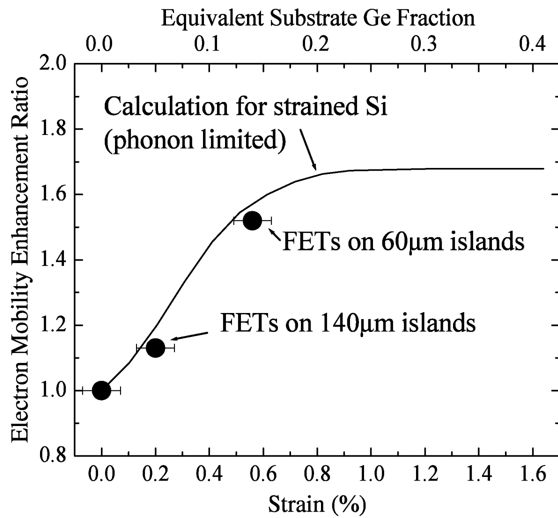


Fig. 13. Enhancement of electron mobility in the strained-silicon devices on BPSG compared to control silicon devices on BPSG as a function of strain in the silicon channel layer. Also shown on the top x axis is the Ge fraction in relaxed SiGe buffers in conventional strained Si on relaxed SiGe structures to give the same strain as that on the lower x-axis. The solid line is a prediction of mobility enhancement due to a reduction of phonon scattering due to strain [1].

where the strain was only ~0.20% due to insufficient lateral relaxation, the mobility enhancement was 13% (Fig. 13). In both cases, however, the mobility enhancement was in good agreement with that expected from a reduction in phonon scattering caused by the strain (shown as a solid line in Fig. 13 [1]).

IV. Summary

Ultrathin tensile s-SOI without a SiGe layer in the final structure was successfully fabricated using stress balance between transferred SiGe and Si films on compliant BPSG. Silicon thicknesses as small as 10 nm with strains as high as 0.73% could be achieved. The approach requires only very thin epitaxial layers without thick buffers and the compliant process enables a change in in-plane lattice constant without misfit dislocations. Dopant diffusion from BPSG could be completely suppressed by a thin silicon nitride film. N-channel MOSFETs fabricated in 25-nm strained-silicon films show good characteristics with mobility enhancement in excess of 50%.

Acknowledgment

The authors would like to thank S. R. Shieh and T. S. Duffy of Princeton University for assistance on Raman Scattering, and A. Margarella at Northrop-Grumman for deposition of BPSG films.

References

[1] S. I. Takagi, J. L. Hoyt, J. J. Welser, and J. F. Gibbons, "Comparative study of phonon-limited mobility of two-dimensional electrons in strained and unstrained Si metal–oxide–semiconductor field-effect transistors," *J. Appl. Phys.*, vol. 80, pp. 1567–1577, Aug. 1996.

[2] J. P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 2nd ed: Kluwer , 1997.

[3] K. Suzuki, T. Tanaka, Y. Tosaka, H. Horie, and Y. Arimoto, "Scaling theory for double-gate SOI mosfets," *IEEE Trans. Electron Devices*, vol. 40, no. 12, pp. 2326–2329, Dec. 1993.

[4] Z. Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadas, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Device Lett.*, vol. 22, no. 7, pp. 321–323, Jul. 2001.

[5] L. J. Huang, J. O. Chu, S. A. Goma, C. P. D'Emic, S. J. Koester, D. F. Canaperi, P. M. Mooney, S. A. Cordes, J. L. Speidell, R. M. Anderson, and H. S. P. Wong, "Electron and hole mobility enhancement in strained SOI by wafer bonding," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1566–1571, Sep. 2002.

[6] S. Eguchi, J. L. Hoyt, C. W. Leitz, and E. A. Fitzgerald, "Comparison of arsenic and phosphorus diffusion behavior in silicon-germanium alloys," *Appl. Phys. Lett.*, vol. 80, pp. 1743–1745, Mar. 2002.

[7] K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, and M. Ieong, "Fabrication and mobility characteristics of ultrathin strained Si directly on insulator (SSDOI) MOSFETs," in *IEDM Tech. Dig.*, Dec. 2003, pp. 3.1.1–3.1.4.

[8] T. S. Drake, C. N. Chleirigh, M. L. Lee, A. J. Pitera, E. A. Fitzgerald, D. A. Antoniadis, D. H. Anjum, J. Li, R. Hull, N. Klymko, and J. L. Hoyt, "Effect of rapid thermal annealing on strain in ultrathin strained-silicon on insulator layers," *Appl. Phys. Lett.*, vol. 83, pp. 972–977, Sep. 2003.

[9] T. A. Langdo, M. T. Currie, A. Lochtefeld, R. Hammond, J. A. Carlin, M. Erdtmann, G. Braithwaite, V. K. Yang, C. J. Vineis, H. Badawi, and M. T. Bulsara, "SiGe-free strained Si on insulator by wafer bonding and layer transfer," *Appl. Phys. Lett.*, vol. 82, pp. 4256–4258, June 2003.

[10] G. Taraschi, A. J. Pitera, L. M. McGill, Z. Y. Cheng, M. J. L. Lee, T. A. Langdo, and E. A. Fitzgerald, "Ultrathin strained Si-on-insulator and SiGe-on-insulator created using low temperature wafer bonding and metastable stop layers," *J. Electrochem. Society*, vol. 151, pp. G47–G56, Jan. 2004.

[11] C. W. Leitz, M. T. Currie, A. Y. Kim, J. Lai, E. Robbins, E. A. Fitzgerald, and M. T. Bulsara, "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," *J. Appl. Phys.*, vol. 90, pp. 2730–2736, Sept. 2001.

[12] M. T. Currie, S. B. Samavedam, T. A. Langdo, C. W. Leitz, and E. A. Fitzgerald, "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," *Appl. Phys. Lett.*, vol. 72, pp. 1718–1720, Apr. 1998.

[13] H. Z. Yin, K. D. Hobart, R. L. Peterson, F. J. Kub, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Fully depleted strained-Si on insulator NMOSFETs without relaxed SiGe buffers," in *IEDM Tech. Dig.*, 2003, pp. 3.2.1–3.2.4.

[14] H. Yin, K. D. Hobart, F. J. Kub, S. R. Shieh, T. S. Duffy, and J. C. Sturm, "Strain partition of Si/SiGe and $SiO_2/SiGe$ on compliant substrates," *Appl. Phys. Lett.*, vol. 82, pp. 3853–3855, Jun. 2003.

[15] H. Yin, R. Huang, K. D. Hobart, Z. Suo, T. S. Kuan, C. K. Inoki, S. R. Shieh, T. S. Duffy, F. J. Kub, and J. C. Sturm, "Strain relaxation of SiGe islands on compliant oxide," *J. Appl. Phys.*, vol. 91, pp. 9716–9722, Jun. 2002.

[16] H. Z. Yin, R. Huang, K. D. Hobart, J. Liang, Z. Suo, S. R. Shieh, T. S. Duffy, F. J. Kub, and J. C. Sturm, "Buckling suppression of SiGe islands on compliant substrates," *J. Appl. Phys.*, vol. 90, pp. 6875–6882, Nov. 2003.

[17] K. D. Hobart, F. J. Kub, M. Fatemi, M. E. Twigg, P. E. Thompson, T. S. Kuan, and C. K. Inoki, "Compliant substrates: a comparative study of the relaxation mechanisms of strained films bonded to high and low viscosity oxides," *J. Electron. Mater.*, vol. 29, pp. 897–900, Jul. 2000.

[18] K. Nassau, R. A. Levy, and D. L. Chadwick, "Modified phosphosilicate glasses for VLSI applications," *J. Electrochem. Soc.*, vol. 132, pp. 409–415, Feb. 1985.

[19] J. Mattews and A. Blakeslee, "Defects in epitaxial multilayers part I: Misfit dislocations," *J. Cryst. Growth*, vol. 27, pp. 118–125, Dec. 1974.

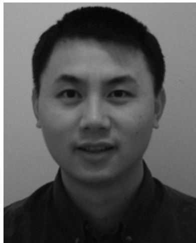
[20] R. People and J. Bean, "Calculation of critical layer thickness versus lattice mismatch for Ge_xSi_{1-x}/Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, pp. 322–324, Aug. 1985.

[21] U. Wieser, D. Iamundo, U. Kunze, T. Hackbart, and U. Konig, "Nanoscale patterning of Si/SiGe heterostructures by electron-beam lithography and selective wet-chemical etching," *Semicond. Sci. Technol.*, vol. 15, pp. 862–867, Aug. 2000.

[22] A. Nakajima, Q. D. M. Khosru, T. Yoshimoto, and S. Yokoyama, "Atomic-layer-deposited silicon-nitride/SiO_2 stack—a high potential gate dielectric for advanced CMOS technology," *Microelectron. Reliab.*, vol. 42, pp. 1823–1835, Dec. 2002.

[23] K. Tokunaga and J. C. Sturm, "Substrate bias dependence of subthreshold slopes in fully depleted silicon-on-insulator MOSFETs," *IEEE Trans. Electron Devices*, vol. 38, no. 8, pp. 1803–1807, Aug. 1991.

[24] Z. B. Ren, B. Doris, P. Oldiges, T. Kanarsky, O. Dokumaci, R. Roy, M. K. Ieong, E. C. Jones, and H. S. P. Wong, "An experimental study on transport issues and electrostatics of ultrathin body SOI pMOSFETs," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 609–611, Oct. 2002.



Haizhou Yin (S'02–M'04) received the B.S. degree in physics from Peking University, Beijing, China, in 1996 and the M.A. and Ph.D. degrees in electrical engineering from Princeton University, Princeton, NJ, in 1999 and 2004, respectively.

At Princeton University, he worked on SiGe-related electronic materials and transistors. He demonstrated high-quality relaxed SiGe on insulator by compliant substrates and fabricated SiGe-free strained Si transistors on insulator. He joined the Department of Exploratory Device and Integration at IBM, Hopewell Junction, NY, in 2004. His current research focuses on strained Si/SiGe devices and hybrid crystal orientation transistors for the extension of CMOS scaling beyond 65-nm gate lengths. He has authored or coauthored more than 20 research papers, and has written a book chapter on SiGe heterojunction bipolar transistor with J. C. Sturm.

Karl D. Hobart (M'00) received the B.S. degree in physics from the University of Illinois, Champaign-Urbana, in 1984 and the M.S. and Ph.D. degrees in electrical engineering from the University of Delaware, Newark, in 1987 and 1990, respectively.

His post-doctoral work at the Naval Research Laboratory (NRL) concentrated on molecular beam epitaxy of silicon and germanium alloys and material characterization. In 1993 he joined SFA, Inc. as an On-site Contractor at NRL where he led an effort for the growth, fabrication, and characterization of microwave power SiGe heterojunction transistors. In 1995, he joined the Microelectronics Device Physics Section at NRL. His interests presently lie with wafer bonding technology for power electronic devices and alternative substrates. He is presently Head of the High Power Devices Section in the Power Electronics Branch. He has been an author or coauthor on over sixty technical articles and holds 14 patents.

Dr. Hobart is a member of the MRS and ECS.

Rebecca L. Peterson (S'98) received the B.S.E.E. from the University of Rochester, Rochester, NY in 1996 and the M.S.E.E. from the University of Minnesota, Duluth, in 2000. She is currently pursuing the Ph.D. degree in electrical engineering at Princeton University, Princeton, NJ.

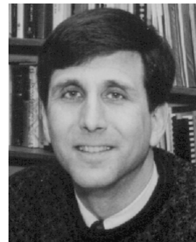
Her current research areas are strain engineering of semiconductors via wafer bonding techniques, and strained-silicon transistor technology. More generally, she is interested in materials development for high-frequency integrated circuits.

Ms. Peterson was the recipient of a National Science Foundation Graduate Fellowship in 1996, an Automatic RF Techniques Group (ARFTG) Student Fellowship in 1999, and an American Association of University Women (AAUW) Selected Professions Fellowship in 2004–2005.

F. J. Kub received the B.S. degree from South Dakota State University, Brookings, in 1972, the M.S.E.E. degree from the University of Minnesota, Duluth, in 1974 and the Ph.D. degree in electrical engineering from the University of Maryland, College Park, in 1985.

Since 1985, he has worked at the Naval Research Laboratory (NRL), Washington, DC, where he is the Supervisor of the Power Electronics Branch. His research interests include the areas of power electronic devices and wafer bonding research. Prior to joining the NRL, he was with the Westinghouse Advanced Technology Laboratory, Baltimore, MD, in the area of CCD device physics and processing, photodetectors for acousto-optic signal processing, and VLSI process development.

Dr. Kub has served on the International Symposium on Power Semiconductor Devices in 2003 and the Imager and Sensor Subcommittee of the International Solid State Circuits Conference from 1994 to 2002. He was Associate Editor of IEEE TRANSACTIONS ON CIRCUIT AND SYSTEMS from 1997 to 1999. He has more than 100 publications and has been awarded 25 patents.



James C. Sturm (S'81–M'85–SM'95–F'01) was born in Berkeley Heights, NJ, in 1957. He received the B.S.E. degree in electrical engineering and engineering physics from Princeton University, Princeton, NJ, in 1979 and the M.S.E.E. and Ph.D. degrees in 1981 and 1985, respectively, both from Stanford University, Stanford, CA.

In 1979, he joined Intel Corporation, Santa Clara, CA, as a Microprocessor Design Engineer, and in 1981 he was a Visiting Engineer at Siemens Company, Munich, Germany. In 1986, he was with the faculty of Princeton University in the Department of Electrical Engineering, where he is currently a Professor and Director of the Princeton Institute for the Science and Technology of Materials (PRISM). In 1994 to 1995, he was a von Humboldt Fellow at the Institut fuer Halbleitertechnik at the University of Stuttgart, Stuttgart, Germany. He has worked in the fields of silicon-based heterojunctions, three-dimensional (3–D) integration, silicon-on-insulator, optical interconnects, TFTs, and organic light-emitting diodes. Current research interests include silicon-germanium and related heterojunctions, SOI and 3-D integration, large-area electronics, flat panel displays, organic semiconductors, and the nano-bio interface.

Dr. Sturm is a member of the American Physical Society and the Materials Research Society, and was a National Science Foundation Presidential Young Investigator. He has won over eight awards for teaching excellence from both Princeton University and the Keck Foundation. In 1996 and 1997, he was the technical program chair and general chair of the IEEE Device Research Conference, respectively. He served on the organizing committee of IEDM (1988 to 1992 and 1998 to 1999), having chaired both the solid-state device and detectors/sensors/displays committees. He also has been a symposium organizer for the Materials Research Society and on the SOS/SOI, EMC, and several other conference committees.