Complementary Metal–Oxide–Semiconductor Thin-Film Transistor Circuits From a High-Temperature Polycrystalline Silicon Process on Steel Foil Substrates

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***Abstract*—We fabricated CMOS circuits from polycrystalline silicon films on steel foil substrates at process temperatures up to 950 °C. The substrates were 0.2-mm thick steel foil coated with 0.5-μm thick SiO_2. We employed silicon crystallization times ranging from 6 h (600 °C) to 20 s (950 °C). Thin-film transistors (TFTs) were made in either self-aligned or non-self-aligned geometries. The gate dielectric was SiO_2 made by thermal oxidation or from deposited SiO_2. The field-effect mobilities reach 64 cm^2/Vs for electrons and 22 cm^2/Vs for holes. Complementary metal-oxide-silicon (CMOS) circuits were fabricated with self-aligned TFT geometries, and exhibit ring oscillator frequencies of 1 MHz. These results lay the groundwork for polycrystalline silicon circuitry on flexible substrates for large-area electronic backplanes.**

***Index Terms*—Complementary metal-oxide-semiconductor devices (CMOS), thin-film circuits, thin-film transistors (TFTs).**

I. Introduction

INTEGRATING switching matrices with driver circuits is becoming more attractive for the backplanes of displays, sensor arrays, and of other large-area electronics applications [1], [2]. The currently dominant display backplane technology is based on hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs). It is difficult to use a-Si:H TFTs for driver circuits, because the electron mobility in a-Si:H is low and p-channel TFTs cannot be made [3]. Therefore, separate integrated circuit (IC) drivers are made externally and connected to the backplane in hybrid configurations. Integration of the backplane switching matrix with the drivers would reduce the display manufacturing cost and also the failures that arise from the large amount of external wiring. Fully polycrystalline silicon (polysilicon) [4], hybrid polysilicon/a-Si [5], and nanocrystalline silicon [6] are candidate materials for this integration.

Manuscript received February 25, 2002; revised August 28, 2002. This work was supported by DARPA's High-Definition Systems and Molecular Level Printing Programs. The review of this paper was arranged by Editor T. Skotnicki.

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Digital Object Identifier 10.1109/TED.2002.804702

Polysilicon films best suited for TFTs are made by crystallization of a-Si:H precursor films [3]. Crystallization techniques [7] include furnace annealing [8], rapid thermal annealing by lamp heating [9], and laser crystallization [5], [10]. Furnace annealing produces highly uniform polysilicon films over large areas, and is a proven batch process. Because the strain points of affordable substrate glasses lie about 600 °C, crystallization and further processing are restricted to temperatures at or below $\sim$ 600 °C, which requires crystallization and ion-implant annealing times as long as 20 h [11], [12]. Catalyzed crystallization can reduce this time to $\sim$ 5 h [13]–[15], which still is long when compared to the process step throughput of one plate per minute desired of the single-substrate cluster tools employed in the manufacture of active-matrix liquid-crystal displays. To find a fast and furnace-based crystallization process for large areas of low-cost substrates to enable the integration of driver circuits for active matrices has been the primary goal of our research [24]–[26].

a-Si:H TFTs have been successfully fabricated on stainless steel substrates at process temperatures up to 300 °C [16]. The melting points of steels lie about 1400 °C, close to the melting point of single crystal silicon of 1414 °C. This paper shows that integrated silicon/steel structures can be processed together to very high temperature as long as they are prevented by barrier layers from reacting with each other. The temperature for crystallizing the amorphous precursor film can be raised to raise the crystal nucleation rate and the crystal growth rate exponentially, so that the crystallization time is reduced dramatically [17]–[19]. In this way, we utilize the high-temperature tolerance of steel to develop a polysilicon-on-steel process that begins with the rapid furnace crystallization time of a-Si:H of minutes or seconds.

Another attractive feature of steel substrates is their flexibility and ruggedness. a-Si:H TFTs on sufficiently thin steel foil substrates can be bent to a radius of curvature as small as 1 mm without degradation of TFT performance [20], [21]. This is attractive for fabricating flexible displays and sensor arrays, and indeed organic light emitting diodes driven by a-Si:H TFTs on thin steel foil have been demonstrated [22]. We expect that TFT arrays on thin steel could eventually be processed in a roll-to-roll fashion in analogy to the existing manufacture of a-Si:H solar cells [23] on stainless steel foil. Of course, because steel is

opaque, it can be used for emissive and reflective, but not transmissive displays.

We crystallized polysilicon films on steel at temperatures ranging from 600 °C to 950 °C, with crystallization time ranging from ∼ 6 h at 650 °C to 20 s at 950 °C. To test mobility, we first made coplanar top-gate TFTs in a non-self-aligned geometry with a deposited source/drain, and then in a more conventional self-aligned geometry with ion-implanted source/drain. In some of our TFTs we grew the gate dielectric by the direct oxidation of the polysilicon (-on-steel) as is done in a conventional IC process. Using the self-aligned TFT process, we also made polysilicon complementary metal-oxide-semiconductor (CMOS) circuits on steel with CMOS inverters and ring oscillators.

II. Experiments

A. Substrate Preparation

The 200-μm thick foils of AISI grade 304 stainless steel (Fe/Cr/Ni 72/18/10 wt.%) were cleaned with acetone and methanol. To reduce the roughness of the steel foil surface, a 210-nm thick planarizing film of phosphorus-doped (0.5%) spin-on glass was applied to both sides and baked. Then, a 270-nm thick film of SiO_2 was deposited on both sides by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 250 °C. Substrates were then heated in a tube furnace from 450 °C to 800 °C and cooled to 600 °C, at a heating/cooling rate of 5 °C/min. Fig. 1 shows the scanning electron micrographs (SEMS) of (a) a bare AISI 304 steel surface and (b) the substrate surface coated with the ∼ 0.5 μm SiO_2 layer and annealed. The ∼0.5-μm thick insulation layer reduced the RMS surface roughness from 5 nm for bare steel foil to $<$ 2 nm.

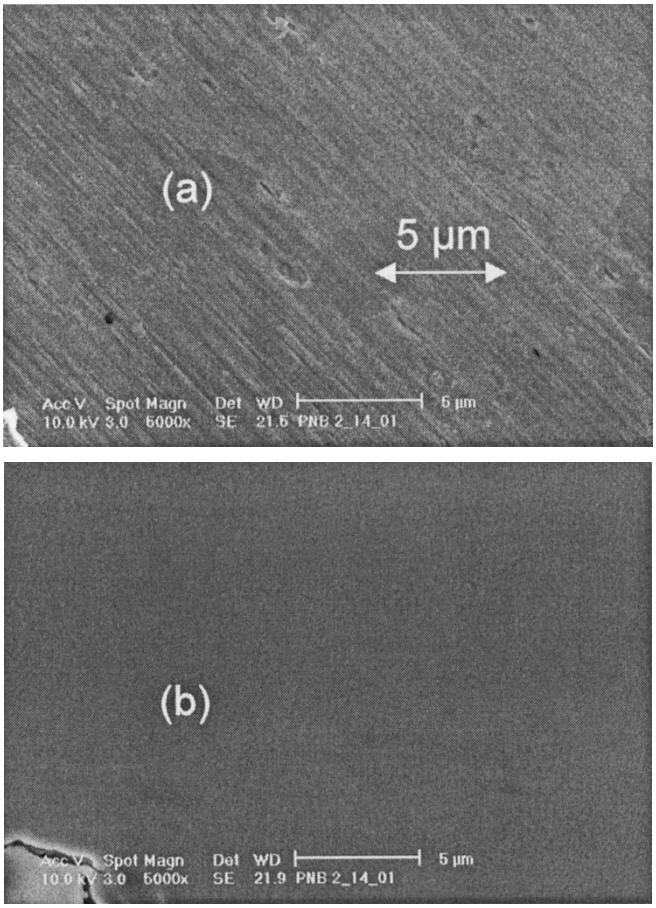

Fig. 1. SEM of (a) bare AISI 304 steel surface and (b) substrate surface after ∼ 0.5 μm SiO_2 insulation layer.

B. Deposition and Crystallization of Hydrogenated Amorphous Silicon

After the insulation layer deposition and annealing described above, a 160-nm thick precursor film of a-Si:H was deposited by PECVD from pure silane at a substrate temperature of 150 °C. Based on previous work in our lab, the hydrogen content of these films is 3×10^{21} atoms/cm^3 [15]. Raising the crystallization temperature exponentially raises both the crystal nucleation rate and the crystal growth rate, so that the crystallization time is reduced dramatically. In TFT technology, 600 °C is the maximum process temperature imposed by the softening of glass substrates. Because the rate of nucleation has a higher activation energy than the rate of crystal growth [17]–[19], raising the crystallization temperature above 600 °C increases the number of nuclei, reduces their size, and reduces the field effect mobility [27]. However, above some temperature the rate of nucleation begins to drop because the size of the critical nucleus grows [17]. Somewhere above 850 °C the nucleation rate is expected to drop while the growth rate keeps rising [17], so that at still higher temperature the grain size and hence the field effect mobility are expected to rise again [28]. Koster [17] suggested that the grain size starts increasing around 850 °C, but Hatalis [28] used rapid thermal annealing to find that the minimum grain is obtained at ∼ 1100 °C. We explored crystallization temperature up to 950 °C.

1) Low-Temperature Crystallization: We first exposed the a-Si:H precursor film for 1 h to a hydrogen glow discharge to create seed nuclei and reduce the crystallization time [15]. These films then were crystallized at one of four different annealing temperature/time combinations: 1) 600 °C for 6 h; 2) 650 °C for 1 h; 3) 700 °C for 10 min; and 4) 750 °C for 2 mim. These crystallization times were chosen assuming an activation energy of 2.7 eV for crystal growth in the a-Si: H precursor films after exposure to the hydrogen discharge for pre-seeding [15]. For crystallization, the a-Si:H film was first heated in the 400 °C zone of the furnace in nitrogen for 30 min and then was transferred in less than 3 s to the center zone set at the crystallization temperature. The completion of crystallization of all samples was confirmed by measuring *ex situ* the ultraviolet reflectance at $\lambda = 276$ nm[8], [9].

2) High-Temperature Crystallization: The a-Si:H precursor films for crystallization at 950 °C were not hydrogen-plasma-treated. These films were heated in the 400 °C zone of the furnace for 30 min, transferred to the 950 °C zone and heated there for either 20 s or 20 min in nitrogen, and then cooled in the ∼ 400 °C zone. UV reflectance indicated complete crystallization. The mismatch in thermal expansion coefficients α between the circuit materials (α of fused quartz $= 0.6 \times 10^{-6}$ K^{-1}, α of silicon $\cong 4 \times 10^{-6}$ K^{-1}) and the steel substrate ($\alpha =$

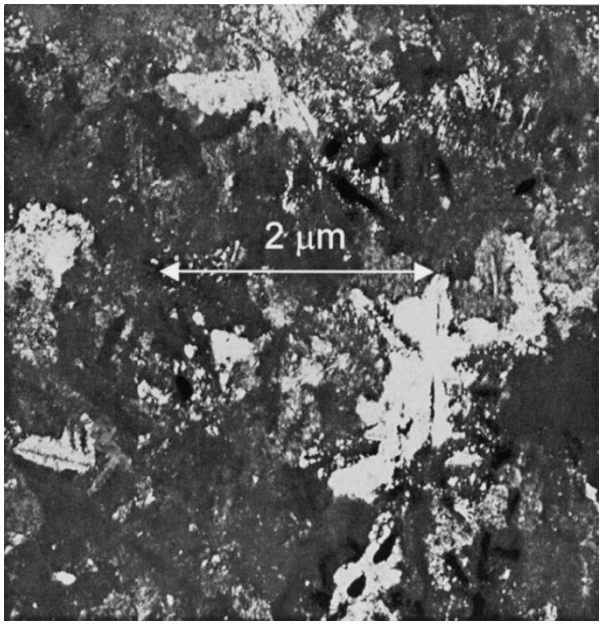

Fig. 2. Dark-field transmission electron micrograph of a 160-nm thick polycrystalline film made on a SiO_2/steel substrate by crystallization at 950 °C20 s. The grain size is $\sim$ 0.5 μm.

18×10^{-6} K^{-1}) does not produce cracks or delamination, even though the range of process temperature is nearly 1000 °C and the calculated compressive strain in the silicon layer may go as high as 1% when the sample is cooled to room temperature following crystallization at 950 °C. Fig. 2 is a transmission electron micrograph of such a polysilicon film crystallized at 950 °C/20 s. Its average grain size is $\sim$ 0.5 μm.

The dark conductivities σ of all polysilicon films were measured at room temperature to check for possible doping by contamination from the metal substrate. They lie at $\sim$ 10^{-6} S $\cdot$ cm^{-1}, i.e., not much above the conductivity of intrinsic polysilicon film prepared on glass substrates [29]. Fig. 3 shows the conductivities in function of temperature of a polysilicon film crystallized at 600 °C and a PECVD a-Si:H film deposited at 250 °C using a recipe optimized for a-Si:H TFTs (which is different from the deposition of a-Si:H for the TFTs of this paper). The thermal activation energies are 0.53 eV and 0.72 eV for polysilicon and a-Si:H films, respectively. The activation energy of 0.53 eV suggests that the Fermi level is pinned in midgap. This could occur if the films are completely free of dopants, or if the Fermi level is pinned by defects, possibly related to metal contamination in the polysilicon or at its interfaces. Further annealing (40 min) left the dark conductivity unchanged. Further data suggesting an absence of metal contamination will be described in Sections III-B and III-C.

C. Thin-Film Transistor Fabrication

All transistors were made in the top-gate coplanar source/drain geometry. Initially a low-temperature device fabrication process (maximum of 350 °C) with deposited source and drain layers was used to gauge the quality of the polysilicon films directly after the recrystallization process, and the results were reported in previous paper [24]. Once the high-temperature capability of the polysilicon-on-steel had been ascertained, a self-aligned process with ion-implanted source and drain was used, requiring anneals over 600 °C. Finally, the deposited gate SiO_2 was replaced with a thermal SiO_2. In this paper, we will describe the self-aligned TFTs with the two gate oxides.

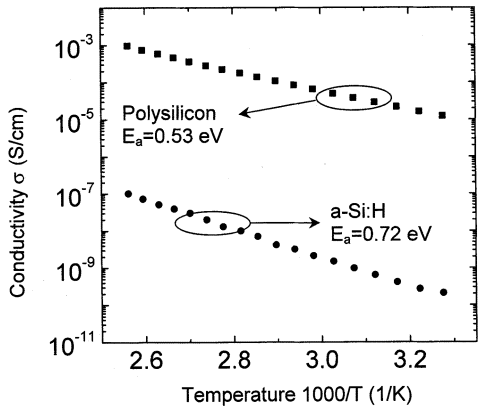

Fig. 3. Conductivity in dark of polysilicon and a-Si:H films. The polysilicon film was formed by furnace crystallization at 600 °C/6 h. For comparison, the a-Si:H film was grown by PECVD at 250 °C.

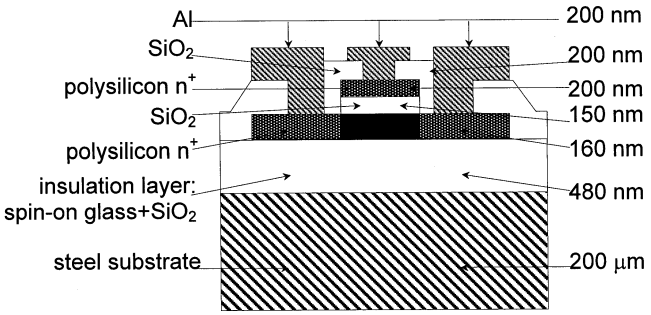

Fig. 4. Schematic cross section of an n- or p- channel polysilicon transistor on steel substrate with ion-implanted source/drain. The transistor with thermal oxidation process has the same structure except that the gate dielectric is 51 nm dry SiO_2.

1) High-Temperature Process—Self-Aligned Structure With Deposited Gate Oxide: The precursor a-Si:H film was crystallized at 950 °C for 20 s or 20 min, and the active area defined by reactive ion etching (RIE) (see Fig. 4). 150-nm gate SiO_2 was deposited by PECVD at either 250 °C or 350 °C. 200-nm intrinsic a-Si:H was deposited by PECVD at 270 °C and then patterned by RIE to form the eventual gate. Then the SiO_2 layer was wet-etched to form the source and drain openings. For n-/p-channel TFTs, the source and drain were implanted with phosphorus/boron at 50/35 keV and a dose of 2×10^{15} cm^{-2}. The implant damage was annealed and the gate silicon was crystallized by a 30-min furnace anneal at 750 °C. Then the sample was immersed in a hydrogen glow discharge at 350 °C for 1 h. A 200-nm SiO_2 passivation layer was deposited by PECVD at 250 °C, and source/drain and gate contact windows were opened by wet etch of the passivation SiO_2. Then, 300-nm Al was thermally evaporated and patterned to form the source/drain and gate electrodes. Finally, the TFTs were annealed in forming gas at 250 °C for 15 min. The highest process temperature after crystallization was the 750 °C post ion-implant anneal. Channel

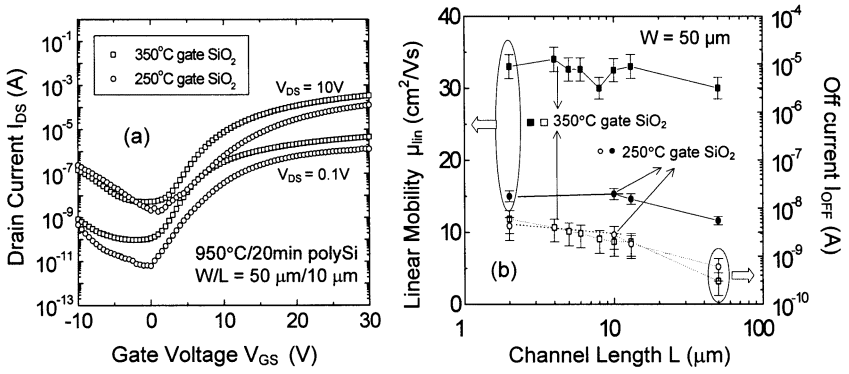

Fig. 5. (a) Transfer characteristic of two self-aligned TFTs made of 950 °C/20 min polysilicon with 350 °C and 250 °C gate SiO_2. (b) Mobility and OFF current versus channel length for TFTs with gate SiO_2 deposited at 250 °C and 350 °C.

lengths ranged from 10 μm to 1 μm. TFTs were also simultaneously fabricated with a ring geometry for the active channel, for films crystallized at 750 °C/2 min. With this geometry, effects of the edge of the channel could be avoided.

2) Self-Aligned TFT With Thermal Gate Oxide: The ability to crystallize device-grade films at 950 °C suggested that the gate dielectric might be grown by direct oxidation of the polysilicon films, instead of PECVD.

Polysilicon was formed by 950 °C/20 s crystallization and then individual TFT islands were defined by RIE. The polysilicon was oxidized in flowing dry O_2 for 40 min at 950 °C in a tube furnace. The oxidation was followed by a 20-min N_2 anneal at the same temperature, and then a 30-min N_2 anneal at $\sim$ 500 °C. A lightly doped silicon wafer with [111] orientation was oxidized with the same process. The resulting oxide thickness on the [111] wafer was measured with a Dektak surface profiler and by ellipsometry to be 51 nm. We made TFTs with the same structure as illustrated in Fig. 4.

D. CMOS Polysilicon TFT Circuits on Steel

To explore the eventual feasibility of polysilicon driver circuits on flexible substrates, CMOS polysilicon circuits were fabricated on steel with a 6-mask process (polysilicon island, gate, n^+ implant, p^+ implant, contact via, metal) and tested. Following the substrate preparation, 150-nm a-Si:H was deposited by PECVD at 150 °C and crystallized at 750 °C/2 min to form the channel layer. No active-layer implant was used. 150-nm gate SiO_2 was deposited by PECVD at 350 °C. 200-nm intrinsic a-Si:H was deposited by PECVD at 270 °C and then patterned by RIE to form the eventual gate. Then the SiO_2 layer was wet-etched to form the source and drain openings. The n^+ and p^+ source/drain (and gate doping) were implanted separately with phosphorus (at 50 keV and a dose of 2×10^{15} cm^{-2}) and boron (at 35 keV and a dose of 2×10^{15} cm^{-2}) using $\sim$ 1 μm AZ5214 photoresist as implant selection mask. The mask photoresist was carefully removed with trichloroethane, acetone and isopropanol after each implant, then the sample was cleaned first with an $H_2O_2 : H_2SO_2 = 1 : 2$ mixture and then in diluted 1:100 HF. The implant damage was annealed and the gate silicon was crystallized by a 30-min furnace anneal at 750 °C. Then, the sample was immersed in a hydrogen glow discharge at 350 °C for 1 h. A 200-nm SiO_2 passivation layer was deposited by PECVD at 250 °C, and source/drain and gate contact windows were opened by wet etch of the passivation SiO_2. 300-nm Al was thermally evaporated and patterned to form the source/drain and gate electrodes. Finally, the TFTs were annealed in forming gas at 250 °C for 15 min.

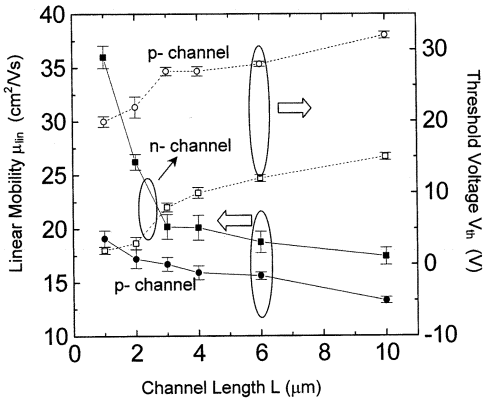

Fig. 6. Linear mobilities and absolute values threshold voltages of open-end n- and p-channel TFTs plotted versus channel length from 1 μm to 10 μm.

III. Results and Analysis

All the TFTs on the flat and grounded steel foil were evaluated with a HP 4155 parameter analyzer. Transfer characteristic (drain current I_{DS} against gate source voltage V_{GS}) and output characteristic (drain current I_{DS} against drain source voltage V_{DS}) were used to derive the device performance and material properties. Drain current ON/OFF ratio is defined as the ratio of highest drain current (on current) to lowest drain current (off current) at $V_{DS} = 10$ V. The dc characteristic of the CMOS inverters were evaluated with the same HP 4155 parameter analyzer, and the transient characteristics of the CMOS inverters and CMOS ring oscillators were evaluated with a Tektronix 3200 digital oscilloscope.

A. Self-Aligned TFT With Deposited Gate Oxide

Self-aligned TFTs were made of polysilicon crystallized at 950 °C/20 s or 950 °C/20 min using 250 °C or 350 °C gate oxide, or crystallized at 750 °C/2 min using 350 °C gate oxide. Effective channel length measurements (done for 950 °C/20 min annealing) showed that the effective channel

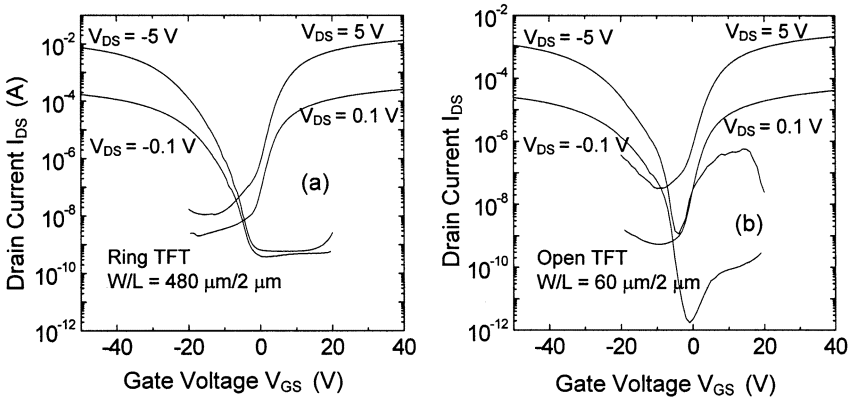

Fig. 7. Transfer characteristics of (a) conventional n- and p- channel TFTs and (b) n- and p- channel ring TFTs with closed gate.

length differed from the drawn channel length at most 0.25 μm. For channel lengths of 5 μm, the 950 °C TFTs have electron mobilities $\mu_{e,lin}$ of 6 ± 0.6 cm$^2 \cdot$ V^{-1}s^{-1} and 15 ± 2.5 cm$^2 \cdot$ V^{-1}s^{-1} for 20 s or 20 min annealed polysilicon with 250 °C gate oxide, respectively. The higher $\mu_{e,lin}$ of the 20-min-annealed polysilicon TFT may be the result of the reduction of grain boundary defects by high-temperature annealing. Fig. 5(a) compares the transfer characteristics of two TFTs made from 950 °C/20 min polysilicon with 350 °C and 250 °C gate SiO_2. The uniformly high linear mobilities ($>$ 30 cm$^2 \cdot$ V^{-1}s^{-1}) of the TFTs with 350 °C gate SiO_2 for all TFT channel lengths, shown in Fig. 5(b), point to the importance of the quality of the gate dielectric and of its interface with the channel material. The transistors made with 20-min annealed polysilicon have the same OFF current as the transistors made with 20-s annealed polysilicon. Excess metallic contamination (Fe, Cr) from steel would likely cause many midgap states and thus a large number of generation centers. Since longer annealing did not increase the leakage current, this data again shows that metallic contamination is not affecting the TFT performance.

One advantage of polysilicon over a-Si:H is its CMOS capability, since p-channel devices are fundamentally not available in a-Si:H technology. In preparation for making CMOS circuits, we fabricated p-channel polysilicon TFTs using the self-aligned structure described above. The polysilicon was formed by furnace crystallization of 150 °C a-Si:H at 950 °C/20 s or 750 °C/2 min. The 950 °C and 750 °C TFTs have hole linear mobilities of $\mu_{lin} = 22 \pm 2$ cm$^2 \cdot$V^{-1}s^{-1} and 14 ± 1.6 cm$^2 \cdot$V^{-1}s^{-1}, respectively. The threshold voltages V_{th} of both TFTs were negative, ~ -20 V.

Fig. 6 contains a plot of the field effect mobility and the threshold voltage in function of channel length, which ranges from 1 μm to 10 μm, for p- and n- channel TFTs made with 750 °C/2 min polysilicon and 350 °C gate oxide. The TFTs with channel lengths $L \leq 2$ μm shows substantially better performance than the TFTs with longer channels, in particular the n-channel devices. This result suggests that the grain size in 750 °C/2 min polysilicon may be as large as 2 μm, or that 1-h long post ion-implantation hydrogenation was not long enough for TFTs with channels ≥ 2 μm. The earlier results on TFTs fabricated on silicon wafer substrates with channel length ranging

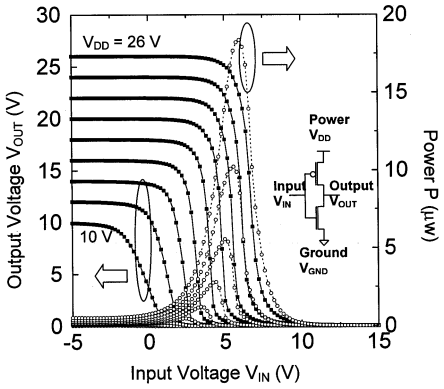

Fig. 8. DC output characteristic of CMOS inverter made with polysilicon TFTs on steel with channel width $W = 60$ μm and length $L = 6$ μm.

from 2 μm to 14 μm show similar trend: the channel mobility decreases as the channel length increases [30]. These results suggest that the transistor performance is correlated with grain size. Polysilicon TFTs have higher carrier mobility and lower threshold voltage when there are fewer grains along the channel [31]. The high values of V_{th}, especially for TFTs with long channels, may be a result of contamination caused by the need to process in a laboratory outside of our microelectronic clean room. Steel substrates are not allowed in this clean room.

B. Self-Aligned TFT With Thermal Oxide

Taking advantage of the high-temperature capability of steel substrates that we had proven at this point, we explored the possibility of transferring standard IC fabrication techniques to polysilicon-on-steel process. This was the purpose of thermal oxidation of the polysilicon TFTs on steel to form SiO_2 gate dielectric. The TFT fabrication process is described in Section II-C3. These transistors have a channel length of 5 μm, and an average $V_{th} = 8.5 \pm 0.8$ V, $\mu_{e,lin} = 27 \pm 2.2$ cm$^2 \cdot$ V^{-1}s^{-1} and $\mu_{e,sat} = 32 \pm 3.1$ cm$^2 \cdot$V^{-1}s^{-1}, and the OFF current $I_{\rm DS}$ is 35 ± 22 pA per μm of channel width at $V_{\rm DS} = 10$ V. Note that even after 40 min at 950 °C during oxidation, the OFF current remains in the same order as that of the low-temperature TFTs, and of the self-aligned TFTs with 250 °C deposited gate oxide.

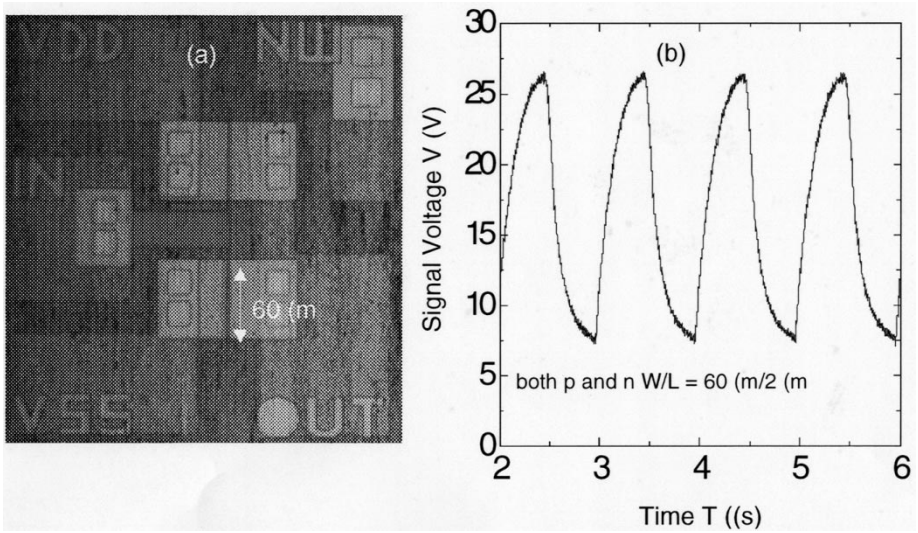

Fig. 9. (a) The top-view microscope picture of a CMOS inverter made on steel made with TFTs with $W = 60\ \mu$m and $L = 2\ \mu$m. (b) AC output signal of the CMOS polysilicon inverter operating at 1 MHz with power supply $V_{\rm DD} = 30$ V.

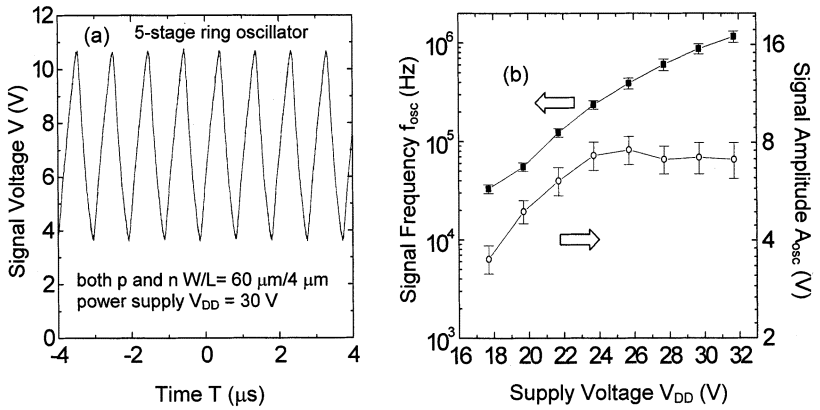

Fig. 10. (a) Output signal of a 5-stage ring oscillator made with CMOS polysilicon inverters on steel. TFTs have channel width $W = 60\ \mu$m and length $L = 4\ \mu$m. (b) Oscillation amplitude and frequency versus the power supply voltage.

C. Effect of TFT Geometry

The edge leakage current was studied by comparing the electrical characteristics of the two types of TFTs fabricated with the self-aligned process: 1) a ring TFT, the drain of which is surrounded by the gate, which eliminates effects at the edge of the gate; and 2) a conventional TFT where the active gated channel includes the edge of the polysilicon island. Fig. 7 shows the transfer characteristics of (a) n- and p-channel ring TFTs and (b) conventional n- and p- channel TFTs, all on the same wafer. OFF currents of the ring TFTs are 23 pA/μm and 1.2 pA/μm for n- and p- channels, respectively, substantially lower than the OFF currents of open-ended TFTs, i.e., 500 pA/μm and 22 pA/μm for n- and p- channels, respectively. This result shows that edge leakage contributes to the OFF current, and points to the need for careful surface passivation.

D. CMOS Polysilicon TFT Circuit on Steel

Fig. 8 shows the dc output characteristics of a CMOS inverter made from polysilicon TFTs with channel width length $L = 6\ \mu$m and $W = 60\ \mu$m. Both the output voltage and the power are plotted on a linear scale against the input voltage. This inverter has a full range swing from the power supply voltage $V_{\rm DD}$ to ground. The output voltage gain K is defined as $\Delta V_{\rm OUT}/\Delta V_{\rm IN}$ at the threshold voltage. This inverter has a gain K of ~ 25 at $V_{\rm DD} \geq 20$ V. The threshold voltage is not exactly half of $V_{\rm DD}$ due to the difference between the n- and p-channel TFT threshold voltages.

Fig. 9(a) is the optical micrograph of a CMOS inverter on steel, the ac output characteristics of which are plots in Fig. 9(b). The CMOS polysilicon inverter operates at 1 MHz with a power supply $V_{\rm DD} = 30$ V and an input signal peak-peak amplitude of 22 V. The n- and p- channels have width $W = 60\ \mu$m and length $L = 2\ \mu$m. The RC time constants for the rise and fall phases are $T_r = 190$ ns and $T_f = 130$ ns, respectively. These values are consistent with the calculated channel resistance $R_{\rm ch}$ of the transistor and load capacitance $C_{\rm para}$, which is the parasitic capacitance of the output contact pad to the steel substrate. The propagation delay in the rise phase can be calculated by the following:

$$T_f = C_{\rm para} \cdot R_{\rm ch} = C_{\rm para} \cdot \frac{V_{\rm DS}}{I_{\rm ch}} \tag{1}$$

$$I_{\rm ch} = \mu_e \cdot \frac{W}{L} \cdot \left(\frac{\varepsilon_{\rm ox}\varepsilon_0}{t_{\rm ox,gate}}\right) \cdot (V_{\rm GS} - V_{n,th}) \cdot V_{\rm DS} \quad (2)$$

$$R_{\rm ch} = \left[\mu_e \cdot \frac{W}{L} \cdot \left(\frac{\varepsilon_{\rm ox}\varepsilon_0}{t_{\rm ox,gate}}\right) \cdot (V_{\rm GS} - V_{n,th})\right]^{-1} \quad (3)$$

$$C_{\rm para} = \left[\frac{A_{D/S}}{t_{\rm ox,ins}} + \frac{A_{\rm metal}}{(t_{\rm ox,ins} + t_{\rm ox,pass})}\right] \cdot (\varepsilon_{\rm ox}\varepsilon_0). \quad (4)$$

The load capacitance $C_{\rm para} = 0.96$ pF is calculated from the geometry of the output pad. $A_{D/S}$ is the drain area of the pull-down and pull-up devices, i.e., the drains of the n-channel TFT and p-channel TFTs. $A_{\rm metal}$ is the metal pad area. $t_{\rm ox,ins}$ and $t_{\rm ox,pass}$ are the thicknesses of insulation SiO_2 (480-nm spin-on-glass and PECVD SiO_2 between the polysilicon and the steel substrate) and the passivation SiO_2 (200-nm PECVD SiO_2), and the gate capacitance of 0.055 pF is negligible compared with the load capacitance; using $\mu_{lin} = 20$ cm$^2 \cdot$ V^{-1}s^{-1}, $\varepsilon_{\rm ox}$ of $SiO_2 = 3.9$, a gate SiO_2 thickness $t_{\rm ox,gate} = 150$ nm, $V_{\rm GS} = 18$ V as the input HIGH voltage, $V_{n,th} = 3$ V for the n-channel threshold voltage, and $R_{\rm ch} = 5.7 \times 10^3 \Omega$, the calculated value of the fall time $T_{f,\rm calc} = 5.8$ ns. The experimental value $T_f = 130$ ns is larger than the calculated theoretical value. We believe this is because the circuit performance is limited by the oscilloscope input capacitance, which is ~ 10 pF.

Fig. 10 shows (a) the ac signal of a 5-stage ring oscillator made with the CMOS polysilicon inverters and (b) the oscillation amplitude and frequency versus the supply voltage. In Fig. 10, the TFTs have channel width $W = 60$ μm and length $L = 4$ μm. The oscillation frequency $f_{\rm osc}$ is 1.03 MHz and its amplitude $A_{\rm osc}$ is 7.1 V at a power supply voltage $V_{\rm DD} = 30$ V. The oscillation frequency rises when the power supply voltage $V_{\rm DD}$ is raised above 15 V. The oscillation amplitude $A_{\rm osc}$ saturates at 7.1 V as the power supply $V_{\rm DD}$ is increased.

IV. Summary

We fabricated polycrystalline silicon TFTs on flexible steel substrates. The polysilicon was formed by crystallization of amorphous silicon at temperatures ranging from 600 °C to 950 °C on SiO_2 coated steel substrates. Ring oscillators with gate delay of ~ 100 ns were demonstrated. Due to their tolerance of high-process temperatures, steel substrates enable much shorter crystallization times than glass substrates, and are tolerant of conventional high-temperature silicon processing methods. The tolerance of high-process temperature enables direct thermal oxidation of polysilicon on steel was used to grow gate dielectric. The polysilicon TFT performance shows no evidence of contamination from steel substrate. These complementary polysilicon TFT circuits on steel foil demonstrate a new route to large-area, flexible TFT backplanes with the performance required for driver and matrix circuits of displays, sensor arrays, and mechatronic materials.

Acknowledgment

M. Wu thanks the Princeton Plasma Physics Laboratory for a tuition fellowship and a summer stipend. The circuit masks were written at the NSF-supported Penn State Nanofabrication Facility. The authors also wish to thank Prof. S. J. Fonash for sharing the cost of mask fabrication.

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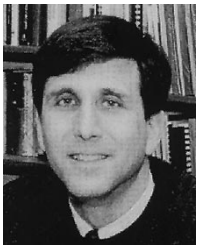

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