Thin-film transistor circuits on large-area spherical surfaces

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We report amorphous silicon (a-Si:H) thin-film transistors (TFTs) fabricated on a planar foil substrate, which is then permanently deformed to a spherical dome, where they are interconnected to inverter circuits. This dome subtends as much as 66° (~1 sr) with the tensile strain reaching a maximum value of ~6% on its top. Functional TFTs are obtained if design rules are followed to make stiff TFT islands of limited size on compliant substrates. Photoresist patterns for island interconnects are made on the flat structure, are plastically deformed during the shaping of the dome, and then serve to delineate interconnects deposited after deformation by lift-off. We describe the effect of deformation on the TFTs before and after deformation and the performance of TFT inverter circuits. Our results demonstrate that the concept of stiff circuit islands fabricated on deformable foil substrates is a promising approach to electronics on surfaces with arbitrary shapes. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1502199]

There is growing interest in flexible electronics, including foldable displays, sensor skins, and electronic textiles. To date, research on curved electronics has been on the cylindrical deformation of thin-film devices on polymer or metal foils.[1–5] In these cases, the devices can be put either in tension (bending outwards) or in compression (bending inwards) by elastic deformation. The strain in the devices can be kept small simply by reducing the substrate thickness, and no substantial change in device characteristics has been observed for bending radii down to 2 mm.[5] Newer concepts, however, require the fabrication of electronics on ''nondevelopable'' surfaces, such as a spherical surface, which can be made from a flat sheet only by plastic deformation. A spherically curved focal plane detector array[6] is one example that offers many optical advantages over a planar array. In this letter, we show how functional circuits of amorphous-silicon thin-film transistors (TFTs) can be made and interconnected on a spherical surface. Two options exist for making such circuits: one, to fabricate the circuits on a flat sheet, which then is deformed to a sphere, and two, to fabricate the circuit directly on the sphere. We pursue the first option because it makes use of standard microfabrication methods.

Deformation of a flat sheet to a spherical shape is inherently more difficult than to a cylindrical one: In spherical deformation the strain is determined by the shape and cannot be reduced by thinning the substrate. For example, the *average* tensile strain in a foil deformed by expansion to a spherical dome with a 66° field of view (1 sr) is ~6%.[7] This level of strain exceeds the tensile fracture limit of device materials (such as silicon and silicon oxide of, typically, ~0.5%), which would crack during deformation to a 1 sr sphere. Here, we show that this problem can be resolved by fabricating stiff device islands on a compliant substrate, deforming the structure to a sphere such that plastic flow is concentrated in the substrate material between the islands, and fabricating only the final interconnects on the sphere.

Figure 1(a) shows a spherical dome of a 50-μm-thick Kapton® E polyimide foil bearing amorphous-silicon islands. The TFTs fabricated in such islands have the conventional staggered bottom-gate, back-channel-etch structure of Fig. 1(b). The fabrication is a modified version of one used previously in our laboratory for a-Si:H TFTs on plastic substrates.[8] All TFT silicon layers were deposited using a three-chamber rf-excited plasma-enhanced chemical vapor deposition system at 150 °C substrate temperature. The polyimide substrate was first passivated with a 0.5-μm-thick layer of SiN_x (layer 1) for planarization and chemical barrier. Next, a 100-nm-thick Cr (layer 2) was thermally evaporated and wet etched to create the gate electrode. The TFT trilayer consisted of 360 nm of SiN_x (layer 3), 200 nm of undoped a-Si:H (layer 4), and 50 nm of n^+ a-Si:H (layer 5). Another 100-nm-thick Cr layer (layer 6) was then evaporated and wet etched to serve as the source–drain contact. The active region for the TFT was defined by reactive ion etching (RIE)

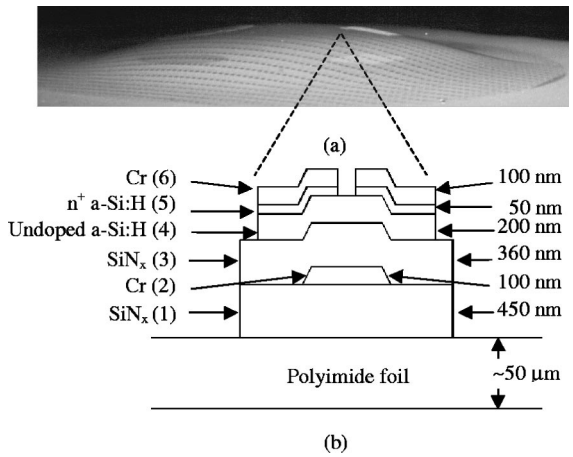

FIG. 1. (a) Spherical dome of polyimide foil bearing a-Si:H islands. (b) Cross section of the TFT island structure on a polyimide substrate.

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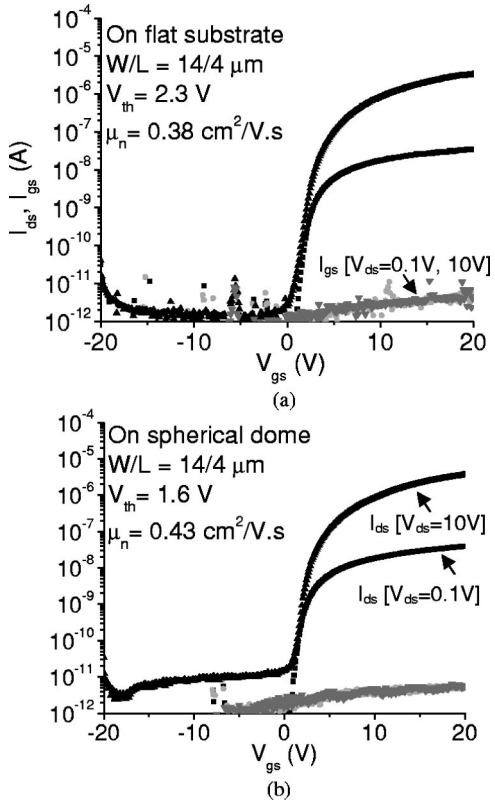

FIG. 2. TFT transfer and gate leakage characteristics, (a) before and (b) after spherical deformation to 66° field of view. ($40\times40\ \mu m^2$ SiN_x island, gate width $W=14\ \mu m$, and gate length $L=4\ \mu m$).

of the n^+ and undoped a-Si:H (layers 4 and 5) in a mixture of SF_6 and CCl_2F_2. The transistors' channel regions were yet to be defined at this stage. SiN_x (layers 1 and 3) was then etched by RIE in a mixture of CF_4 and O_2. Regions protected by photoresist then became isolated device islands, which would withstand the subsequent substrate expansion. Outside the active device area but still on the islands, the dry etch stops at the first Cr layer, so this patterning step also etched windows into the SiN_x gate dielectric layer (layer 3) to create openings where the gate layer could be contacted. Finally, the channel region was defined by removing n^+ a-Si:H (RIE in CCl_2F_2) between the source/drain contacts by using the initially defined Cr source/drain layer (layer 6) as a mask.

To perform the deformation, the substrate was clamped by a circular ring of 6 cm in diameter.[7] Pressurized gas then deformed the material within the clamped ring to a spherical dome with 66° field of view under pressure, relaxed to 58° field of view after the pressure release. The substrate was held at 150 °C to soften the polymer substrate, which allows us to achieve larger crack-free device islands after deformation than possible with deformation at room temperature. Previous work[7] has shown that deforming at 150 °C increases the yield of 50 μm crack-free islands from 0% to more than 90%.

The transistors are little affected by the deformation process. Figure 2 shows the transfer and gate leakage characteristic of the TFTs before and after the substrate deformation to ~1 sr, which corresponds to raising the center of the foil by 0.9 cm. The threshold voltage (V_{th}) and the electron mobility in saturation (μ_n) are calculated from the transfer characteristic in saturation at the source–drain voltage $V_{ds}=10$ V. Deformation raised the average mobility (of five devices tested) from 0.39 to 0.42 $cm^2/V\,s$ (an increase of ~7.7%), and reduced the average threshold voltage from 2.1 to 1.6 V. The gate currents remained below 1×10^{-11} A ($<2\times10^{-13}$ A/μm^2). A decrease in the threshold voltage from 3.5 to 2.6 V (average of ten devices) and an increase in the mobility from 0.28 to 0.36 $cm^2/V\,s$ (an increase of ~28%) were also observed after a separate batch of similarly fabricated devices was held at ~150 °C for 20 min without any deformation. Both groups of devices had similar increases in off current. (The difference in initial as-fabricated characteristics for these two groups is within the normal variability of research-grade TFT processing from substrate to substrate in our single substrate deposition system.)

Since both the mechanical deformation and the heating process used to soften the substrates can contribute to the change in device characteristics, we need to know the amount of strain in the device islands after deformation. Due to the nature of amorphous silicon, direct measurement of the strain distribution is difficult. Therefore, we performed finite-element mechanical modeling of the strain distribution in the semiconductor island. We assumed the island thickness to be 1 μm with a Young's modulus E of 200 GPa for all TFT layers.[9] For simplicity, round islands (50 μm in diameter) were modeled. We have obtained the mechanical properties of polyimide (Kapton® E) at deformation temperature (150 °C) by using the properties at room temperature,[10] and scaling them according to the temperature effect on the stress–strain relationship of a similar polyimide film (Kapton® HN), described in Ref. 11. The result showed that the maximum circumferential strain produced in the island during deformation is ~0.32% while pressure is applied. After the pressure is unloaded the strain is reduced to ~0.29%.

Tensile strain raises the electron field-effect mobility in a-Si:H at room temperature.[12] The relative increase of mobility for a uniaxial strain of 0.29% along the direction of the channel is 7.25% (Ref. 12) (for similar TFTs without heating after processing). This result is similar to our experiment data (devices with an increase of ~7.7% in mobility after deformation). However, our experiments showed that heating to 150 °C alone can result in up to a ~28% increase in TFT mobility for our amorphous-Si TFT process, and heating could also change the dependence of mobility in strain. Furthermore, TFTs on spherical domes are under a biaxial strain (both in the perpendicular and parallel directions to the channel) but the effect of strain perpendicular on mobility in an orthogonal direction in a-Si TFTs is not well known. Thus, at present not enough is known to quantitatively predict the mobility change of the a-Si TFTs from the predicted strain.

The fabrication of circuits requires metal interconnects between device islands. Because most of the deformation takes place in the between islands region, the local strain far exceeds the average value.[7] In the present experiment the strain between islands is more than 8%. Consequently, metal interconnect lines made between device islands before deformation would fracture during deformation. Patterning interconnects after deformation would require photolithography and alignment on the sphere, for which no simple technology

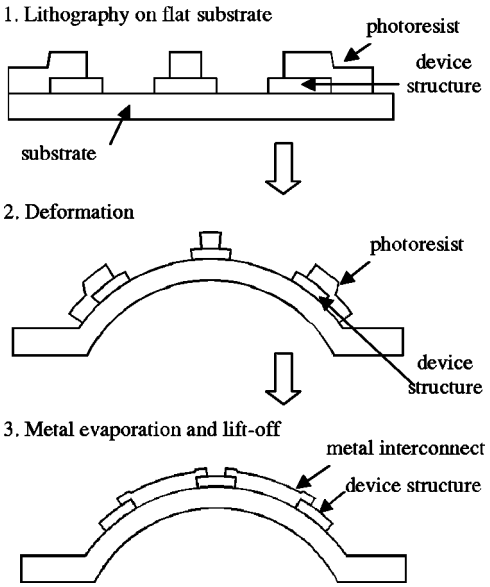

FIG. 3. Lift-off process.

exists. This obstacle was overcome with the approach[13] described in Fig. 3.

A sacrificial layer of photoresist was patterned by conventional photolithography on the flat substrates after the devices were finished. The substrate was then deformed to a spherical dome, and the photoresist underwent this large plastic deformation (8%) without cracking. A 450-nm-thick Al layer was thermally evaporated on the dome after deformation, and then patterned to interconnects by lift-off through stripping the photoresist. The pull-down and pull-up transistors on different islands were connected through this process to form an inverter circuit. The characteristics of an inverter made on a spherical dome are shown in Fig. 4. The transfer curve of the inverter begins to switch at input voltage of ~ 2 V, corresponding to the threshold voltage of the pull-down transistor as expected. The drop of the output voltage for high input voltage is limited by the fact that the pull-up transistor does not turn off when the input is high as it does in a complementary metal–oxide–semiconductor circuit with a *p*-channel pull-up.

In summary, thin-film transistor circuits on spherical domes were fabricated by first making the devices with conventional processes in islands on flat polyimide substrates.

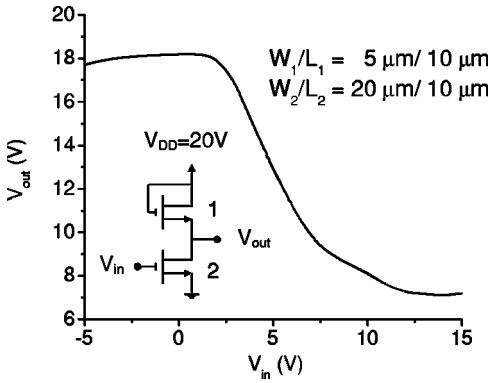

FIG. 4. Transfer curve of a pair of inverters made on the spherical dome by connecting TFTs on separate islands.

The substrates were deformed plastically such that the tensile strain was concentrated in the interisland regions, and with little effect on the TFTs. Interconnects were made by lift-off using prepatterned photoresist that deformed plastically together with the substrate, demonstrating a viable approach for achieving electronics on arbitrary surfaces.

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