

Integrated Amorphous and Polycrystalline Silicon Thin-Film Transistors in a Single Silicon Layer

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Abstract—Using a masked hydrogen plasma treatment to spatially control the crystallization of amorphous silicon to polycrystalline silicon in desired areas, amorphous and polycrystalline silicon thin-film transistors (TFTs) with good performance have been integrated in a single film of silicon without laser processing. Both transistors are top gate and shared all process steps. The polycrystalline silicon transistors have an electron mobility in the linear regime of $\sim 15 \text{ cm}^2/\text{Vs}$, the amorphous silicon transistors have a linear mobility of $\sim 0.7 \text{ cm}^2/\text{Vs}$ and both have an ON/OFF current ratios of $> 10^5$. Rehydrogenation of amorphous silicon after the 600°C crystallization anneal using another hydrogen plasma is the critical process step for the amorphous silicon transistor performance. The rehydrogenation power, time, and reactor history are the crucial details that are discussed in this paper.

Index Terms—Crystallization, hydrogen, hydrogen plasma, silicon, thin-film transistors (TFTs).

I. INTRODUCTION

FOR large area electronics, there has been considerable interest to integrate both amorphous silicon ($a\text{-Si:H}$) thin-film transistors (TFTs), for low leakage in the OFF state, and polycrystalline silicon (poly-Si, polysilicon) TFTs, for high drive currents, on the same substrate. This might be done to integrate polysilicon drivers in flat panel displays using $a\text{-Si:H}$ TFTs in pixels. This paper describes the use of selective crystallization using hydrogen plasma treatment of $a\text{-Si:H}$ to achieve this aim. Exposure of $a\text{-Si:H}$ to atomic hydrogen can reduce its crystallization time [1]–[4]. Specifically, we reported earlier that a room temperature hydrogen plasma exposure in a parallel plate diode type reactive ion etcher (RIE) reduces the crystallization time of $a\text{-Si:H}$ by a factor of 5 compared to the untreated film [1]. This plasma-enhanced crystallization can also be spatially controlled by masking with patterned silicon oxide or silicon nitride, so that both amorphous and polycrystalline areas can be realized simultaneously at desired locations [1], [5].

Integration of $a\text{-Si:H}$ and poly-Si TFTs is traditionally difficult for three reasons. First, the conventional $a\text{-Si:H}$ TFT fabrication process is a low-temperature process ($< 350^\circ\text{C}$) [6], while the poly-Si TFT fabrication requires a $500\text{--}600^\circ\text{C}$ crystallization anneal to form the polycrystalline layer, if no laser

processing is involved. Second, one would like to deposit only a single Si layer instead of two ($a\text{-Si:H}$ and poly-Si) to save cost. Third, the structure and fabrication sequence of $a\text{-Si:H}$ TFTs and poly-Si TFTs are quite different (e.g., bottom gate versus top gate process), so that few process steps can be shared.

Various techniques have been tried to integrate $a\text{-Si:H}$ and poly-Si TFTs on the same substrate. One method is excimer laser annealing to crystallize the chemical vapor deposited (CVD) deposited $a\text{-Si}$ selectively and fabricate bottom gate transistors in both the amorphous and polycrystalline regions [7]–[9]. Another method uses crystallization of a thin (20 nm) $a\text{-Si:H}$ layer deposited by plasma-enhanced CVD (PECVD) using Ar and XeCl ($300 \text{ mJ}/\text{cm}^2$), and subsequent deposition of a thick (200 nm) $a\text{-Si:H}$ layer and patterning the $a\text{-Si:H}$ to realize staggered layers of poly-Si and $a\text{-Si:H}$. Top gate TFTs were then fabricated in the two regions [10]. Both of these methods involve laser processing, which has relatively low throughput and also can lead to variable film quality due to variations in laser beam power and width. Also, the latter method involves fabrication of TFTs in staggered layers, i.e., the transistors are not in a single silicon layer.

In this paper, a method is presented for integrating $a\text{-Si:H}$ and poly-Si transistors together starting with a single Si layer. The approach shares all fabrication steps between the two transistors, except for the one initial step, which defines the regions to be selectively crystallized. The fabrication involves no laser processing. The work is based on our earlier work on the crystallization of amorphous silicon in selected areas to crystallize silicon using a patterned hydrogen plasma exposure [1], [2]. In this process, we have two key steps:

- 1) Selective hydrogen plasma-enhanced crystallization using a SiN_x cap layer on the $a\text{-Si:H}$ region to locally prevent the hydrogen-plasma-induced nucleation.
- 2) Rehydrogenation of the amorphous region after the 600°C anneal to obtain device quality $a\text{-Si:H}$.

We have previously reported this basic approach and the material properties of the rehydrogenated amorphous silicon films [11]. In this paper, we present the details of the optimization of the device processing conditions to obtain optimum integrated amorphous and polycrystalline silicon transistor performance.

II. MATERIAL AND DEVICE PROCESSING SEQUENCE

Hydrogenated amorphous silicon ($a\text{-Si:H}$) films of thickness 150 nm were deposited by plasma-enhanced chemical vapor deposition (PECVD) using pure silane on Corning 1737 glass substrates at a substrate temperature of 150°C , 13.56 MHz rf power of $\sim 0.02 \text{ W}/\text{cm}^2$, and pressure of 66 Pa. Before the

Manuscript received July 3, 2000. This work was supported by DARPA Grant F-33615-98-1-5164 through ONR [N66001-97-1-8904] and the Princeton Program in Plasma Science and Technology (DOE Contract DE-AC02-76-CHO-3073). The review of this paper was arranged by Editor D. P. Verret.

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Publisher Item Identifier S 0018-9383(01)02349-8.

hydrogen plasma treatment to seed the subsequent crystallization, patterned layer of SiN_x was deposited to locally mask the seeding. SiN_x was used as the masking layer instead of SiO_2 in our earlier work [1], [2] and the reasons will be discussed in detail in the next section. The SiN_x was deposited by PECVD at 200 °C using 5 sccm of SiH_4 , 50 sccm of NH_3 and 220 sccm of H_2 , at a pressure of 66 Pa, and an rf power density of 0.09 W/cm^2 [12]. The SiN_x was then patterned by lithography and etched with dilute (1 : 10) hydrofluoric acid. The subsequent rf plasma exposure was done in a parallel plate RIE at room temperature with hydrogen at an rf power density of 0.8 W/cm^2 , pressure of 6.6 Pa and exposure time of ~ 60 min. The rf frequency was 13.56 MHz. The sample was placed on a 125 mm Si wafer during the exposure to minimize aluminum contamination due to aluminum sputtered from the electrode onto the sample surface [2]. All samples were annealed in a furnace at 600 °C in N_2 for 3–5 h with the SiN_x capping selected $\alpha\text{-Si:H}$ regions so that hydrogen outdiffusion from the amorphous regions is minimized. UV reflectance was done on all samples to monitor the crystallization process. Based on earlier work [13], the saturation of growth of the reflectance peak at 276 nm is used as an indication of complete crystallization of the sample.

The 3–5 h anneal at 600 °C is sufficient to convert the areas previously exposed to hydrogen plasma to polycrystalline silicon, while the areas under silicon nitride remained amorphous.

Even though the amorphous regions were capped with SiN_x during the crystallization anneal, hydrogen content in the film fell to ~ 0.3 at. % from ~ 15 at. % (as measured by integrated infrared absorption at 630 cm^{-1}) in the original as-grown film [11], [14]. This results in many unpassivated dangling bonds in the $\alpha\text{-Si}$, so that the resulting film was of poor device quality. The electron field-effect mobility in TFTs with no rehydrogenation was only $0.02\text{ cm}^2/\text{Vs}$ (sample 1, Table II). Rehydrogenation of the film is therefore essential to improve the TFT performance. This was done by exposing the sample to a hydrogen plasma at rf power of $0.2\text{ W}/\text{cm}^2$ and substrate temperature of 350 °C and chamber pressure of 133 Pa for ~ 75 min. Further details on the effect of the rehydrogenation on the material characteristics of the amorphous silicon such as infrared absorption and defect densities has already been reported [11]. Table I summarizes the effect of rehydrogenation on the material characteristics of the amorphous silicon films.

The process flow for the TFT fabrication is shown in Fig. 1. The process is not self-aligned, and is similar to the inverted-staggered process typically used for $\alpha\text{-Si:H}$ TFTs in active-matrix-liquid-crystal displays. Both the transistors are top-gate (which is unusual for $\alpha\text{-Si:H}$ TFTs), and share all process steps. The lithography mask used to pattern the nitride layer to mask the seeding plasma is the only difference between the two devices.

After the rehydrogenation step, ~ 50 nm of n^+ microcrystalline ($\mu\text{c-Si:H}$) silicon was deposited by PECVD using SiH_4 , H_2 and PH_3 , at a pressure of 120 Pa, rf power of $\sim 0.3\text{ W}/\text{cm}^2$, and at a substrate temperature of 340 °C [15] [Fig. 1(a)]. Device islands were then defined by dry etching in a SF_6 and CCl_2F_2 plasma at an rf power of $\sim 0.3\text{ W}/\text{cm}^2$ and pressure of 13 Pa. Future channel regions were defined by dry etching just the n^+ $\mu\text{c-Si:H}$ layer in a separate etching step using a CCl_2F_2 and

TABLE I
MATERIAL CHARACTERISTICS OF THE $\alpha\text{-Si:H}$ FILMS DEPOSITED AT 150 °C, AFTER DEPOSITION, AFTER 600 °C ANNEAL WITH SiN_x CAP ON, AND AFTER REHYDROGENATION AT 350 °C FOR 75 MIN. AT RF POWER OF $0.2\text{ W}/\text{cm}^2$

Material Properties	$\alpha\text{-Si}$ as-deposited at 150 °C	$\alpha\text{-Si:H}$ after 4 h anneal at 600 °C (with cap)	$\alpha\text{-Si:H}$ after optimal rehydrogenation
Net Hydrogen content (at. %)	15	0.3	4.4
Midgap density of states (cm^{-3})	6×10^{17}	4×10^{19}	6×10^{18}
Tauc optical gap (eV)	1.8	1.6	1.7
Dark conductivity activation energy (eV)	0.96	0.18	0.79

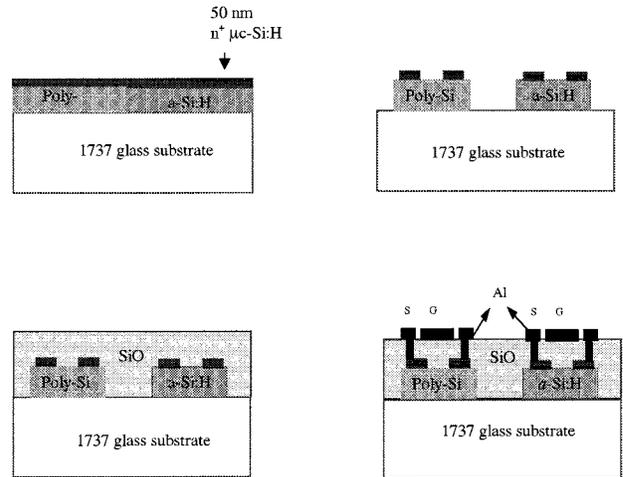


Fig. 1. Schematic of the process flow of fabrication of top-gate integrated $\alpha\text{-Si:H}$ and poly-Si TFTs on glass substrate with the cross section of the final structure.

O_2 plasma at an RF power of $0.08\text{ W}/\text{cm}^2$ and pressure of 13 Pa [Fig. 1(b)]. During the etching step, laser interferometry is used to detect end-point and accurately determine the thickness of the layer etched. The sample was then rinsed first with sulfuric acid and hydrogen peroxide solution and then dilute hydrofluoric (HF) acid to clean the surface. This may help to smooth the surface, which will become the channel, due to the chemical etching that occurs.

The gate dielectric, 130–180 nm of SiN_x or SiO_2 , was then deposited by PECVD at a substrate temperature of about 250 °C [Fig. 1(c)]. Contact holes were then made to the source and drain regions by etching in dilute HF and aluminum was evaporated and patterned to form the gate, and source and drain contacts [Fig. 1(d)]. The samples were then annealed at 225 °C in forming gas to reduce contact resistance.

III. CRITICAL PROCESS PARAMETERS

Fabrication of the integrated TFTs required the careful optimization of many parameters. The three most important parameters were the following.

- 1) Deposition temperature of the original PECVD $\alpha\text{-Si:H}$, which determines the selective crystallization window.
- 2) Type of capping layer used during selective plasma exposure and subsequent selective crystallization.
- 3) Rehydrogenation condition, which is necessary to realize device quality $\alpha\text{-Si}$ after the high temperature anneal.

TABLE II

TFT CHARACTERISTICS FOR SEVERAL COMBINATIONS OF PROCESSING CONDITIONS. THE OPTIMUM CONDITION IS HIGHLIGHTED. THE STANDARD PROCESS FLOW SHOWN IN FIG. 1 WAS USED FOR FABRICATION OF THE TRANSISTORS. I_{OFF} IS DEFINED AS THE MINIMUM CURRENT FOR ANY V_{GS} AT $V_{DS} = 10$ V, AND THE I_{ON}/I_{OFF} RATIO IS CALCULATED WITH ABOVE I_{OFF} AND I_{ON} AT $V_{GS} = 20$ V AND $V_{DS} = 10$ V

S. No	Growth temp. (°C)	<i>a</i> -Si:H (nm)	Cryst. Temp/time	Rehydrogenation		Gate Dielec. (nm)	<i>a</i> -Si:H TFTs					Poly-Si TFTs			
				RF (W)	Exp. (min)		μ cm ² /Vs	V_{TH} (V)	S V/dec	ON/OFF	I_{off} (fA/ μ m)	μ cm ² /Vs	V_{TH} (V)	S V/dec	ON/OFF
1	150	150	600°C/4 h	0	0	SiN _x / 170	0.02	6	2	5x10 ⁴	8	7	3.3	1.3	5x10 ⁴
2	250	150	600°C/5 h	45	60	SiN _x / 170	0.01	1.5	1.2	10 ³	50	3	1.4	1.1	2x10 ⁵
3	150	150	600°C/4 h	45	60	SiN _x / 170	0.24	4.2	1.1	4x10 ⁵	30	9	1.5	1.2	<10 ⁵
4	150	150	600°C/4 h	20	60	SiN _x / 170	0.03	5	1.3	10 ⁵	4	6	3	1.5	2x10 ⁵
5	150	150	600°C/4 h	90	60	SiN _x / 170	0.02	3	1.3	10 ⁵	5	8	1	1	3x10 ⁴
6	150	150	600°C/4 h	45	30	SiO ₂ / 170	0.05	5	1.3	4x10 ⁴	5	12	1.5	1.2	3x10 ⁴
7	150	150	600°C/4 h	45	60	SiO ₂ / 130	0.5	5	1	5x10 ⁵	100	14	1	1	10 ⁵
8	150	150	600°C/4 h	45	75	SiO ₂ / 180	0.8	5	1	10 ⁶	10	15	2	1	2x10 ⁵
9	150	150	600°C/4 h	45	90	SiO ₂ / 120	0.1	1	0.7	4x10 ⁴	40	14	0	2	2x10 ⁵
10	150	75	600°C/5 h	20	60	SiN _x / 170	0.01	5	1.2	8x10 ⁴	3	1	4	1.2	2x10 ⁵
11	150	300	600°C/4 h	45	75	SiO ₂ / 180	0.6	6	0.95	5x10 ⁵	50	12	1	1.2	10 ⁴
12	150	150	625°C/1 h	45	60	SiO ₂ / 130	0.7	4	1	10 ⁵	100	8	0	0.9	5x10 ³
13	150	150	625°C/1 h	45	75	SiO ₂ / 130	1.2	6	0.4	10 ⁷	1	9	1	1	2x10 ⁵

In addition to optimizing the above process parameters, we also evaluated the impact of thickness of original *a*-Si:H film, temperature of crystallization anneal, type of gate dielectric and post metal hydrogenation. We will refer to sample numbers of Table II in the following discussion.

A. Deposition Temperature of Amorphous Silicon

Selective crystallization is crucial to integration of the *a*-Si:H and poly-Si TFTs. This requires a window between the crystallization times of the seeded regions to that for the covered untreated regions. Maximizing this window helps in improving the quality of the *a*-Si:H TFTs. In our earlier work we found that the growth temperature of *a*-Si:H impacts the crystallization time of the untreated *a*-Si:H films, while crystallization time of the hydrogen-plasma-treated films (seeded regions) showed no dependence on the growth temperature of the *a*-Si:H films [2]. Films deposited at 150 °C had the largest crystallization window of > 14 h at 600 °C, compared to ~ 8 h at 600 °C for the 250 °C films. The *a*-Si:H TFTs show improved performance when the *a*-Si:H films are deposited at 150 °C (sample 3) instead of 250 °C (sample 2), as can be seen in Fig. 2. Possibly the more porous structure of the *a*-Si:H deposited at 150 °C facilitates rehydrogenation, and therefore produces TFTs with μ_n of 0.24 cm²/Vs instead of 0.01 cm²/Vs for the 250 °C film. The large difference in mobilities might also be due to larger contact resistance in case of sample 1.

In addition, the poly-Si field-effect mobility was also higher for the 150 °C sample compared to the 250 °C sample, 9 cm²/Vs instead of 3 cm²/Vs. The higher hydrogen content for the 150 °C sample [2] facilitates nucleation and growth of larger grains [16], which in turn led to the higher electron field-effect mobility (μ_n) for the poly-Si TFTs. All the TFTs in this case had SiN_x as the gate dielectric.

B. Capping Layer for Selective Crystallization

The capping layer must provide a barrier against the hydrogen plasma during seeding, and also serve as a diffusion barrier

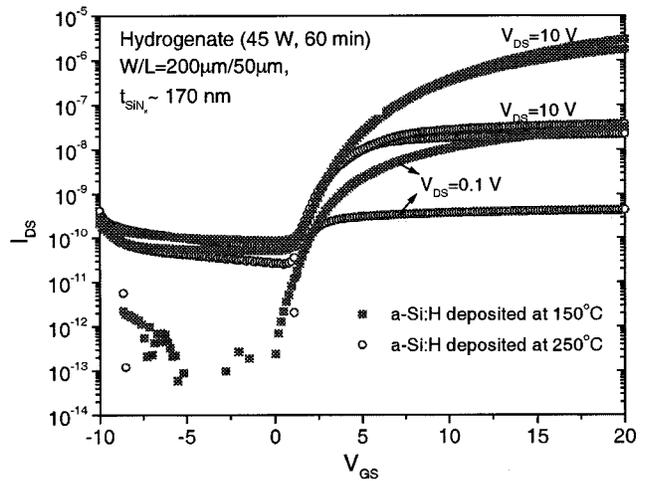


Fig. 2. Subthreshold characteristics of *a*-Si:H TFTs for two different growth temperatures of the *a*-Si:H precursor film (samples 2 and 3 of Table II); 150 °C yielded improved I_{ON} and better I_{ON}/I_{OFF} .

against hydrogen outdiffusion during the high temperature (≥ 600 °C) anneal when the exposed regions crystallize. Silicon nitride is far superior in these respects to SiO₂. The normal SiN_x growth temperature is ~ 300 °C or higher, which alters the characteristics of the as-deposited *a*-Si:H film grown at 150 °C and reduces its crystallization time from 20 h to ~ 12 h at 600 °C. This might be because the hydrogen in the *a*-Si:H begins to out diffuse at a few degrees above the growth temperature [17]. Therefore, the SiN_x deposition recipe was changed to 200 °C, and hydrogen dilution was used during SiN_x growth to reduce the hydrogen content in the SiN_x film and make the film denser [12] and hence a better diffusion barrier.

The SiN_x is also better than SiO₂ in another respect. Regions of *a*-Si:H film covered by the nitride film crystallize slower than those in which the nitride has been removed. The SiN_x has a larger lattice constant than the *a*-Si:H and is deposited at higher temperature than the *a*-Si:H film (200 versus 150 °C).

This results in tensile stress in the thin a -Si:H films, which inhibits nucleation during the subsequent crystallization, anneal [18]–[20]. This helps the regions covered by the nitride remain amorphous during the high temperature annealing, thereby increasing the selective crystallization window. All samples shown in Table I had SiN_x capping layer on the amorphous regions during the selective crystallization anneal.

C. Rehydrogenation Condition

Though SiN_x is used as a capping layer during the crystallization process, extensive hydrogen outdiffusion still does occur [11], [14]. The TFTs fabricated in a -Si directly after the crystallization anneal, without any rehydrogenation (sample 1), have poor mobilities of $\sim 0.02 \text{ cm}^2/\text{Vs}$, while the poly-Si TFTs have mobilities of $\sim 7 \text{ cm}^2/\text{Vs}$. Rehydrogenation is therefore required to passivate the dangling bonds in the amorphous region and thereby improve the electrical characteristics of the film. But rehydrogenation is a double-edged sword, as the hydrogen radicals abstract hydrogen from the a -Si:H layer and even etch the amorphous silicon layer by inserting in Si–Si bonds and creating volatile SiH_4 [21]. Therefore, the hydrogen plasma parameters, primarily the RF power and exposure time, have to be adjusted just right, so that the film is sufficiently hydrogenated but not etched. The rehydrogenation is done at low rf power and that the substrate temperature is raised to accelerate the hydrogen diffusion into the bulk of the film.

The original hydrogen plasma treatment to seed the crystallization before the 600°C anneal actually resulted in removal of hydrogen from the surface of the a -Si:H film [2]. The hydrogen passivation plasma discussed here, which results in hydrogen being added to the a -Si to passivate the dangling bonds, is fundamentally different, in that the pressure is higher and the rf power density is lower, so that the dc self-bias during rehydrogenation is $\sim 30 \text{ V}$. The estimated ion energy (from dc self-bias) is $\sim 30 \text{ eV}$ during the rehydrogenation versus $\sim 500 \text{ eV}$ during the hydrogen-plasma-seeding treatment. The optimum condition for rehydrogenation was found to be a hydrogen plasma at rf power density of 0.2 W/cm^2 , chamber pressure of 133 Pa , H_2 flow of 50 sccm , substrate temperature of 350°C , and exposure time of $\sim 75 \text{ min}$. The effect of rehydrogenation on the materials properties of the annealed a -Si:H films has been discussed elsewhere [11].

For proper hydrogenation, the chamber walls and the electrodes must be properly prepared prior to the rehydrogenation step. Immediately before rehydrogenation, it was necessary to deposit a -Si:H on dummy glass slides using the same sample holder as the one to be used for the actual rehydrogenation, to coat the chamber walls and the sample holder with a -Si:H film. This was done to minimize etching of a -Si:H film during the subsequent rehydrogenation step. During the rehydrogenation step, the a -Si:H film deposited on the walls and the electrodes is also etched and thereby the etching of the sample a -Si:H film is minimal (loading effect). This dummy coat of a -Si:H must be done at low temperatures ($<150^\circ\text{C}$), as the etch rate of a -Si:H during the hydrogen plasma exposure increases if the growth temperature of the a -Si:H is lowered and this ensures that the dummy a -Si:H film on the chamber walls and electrodes is

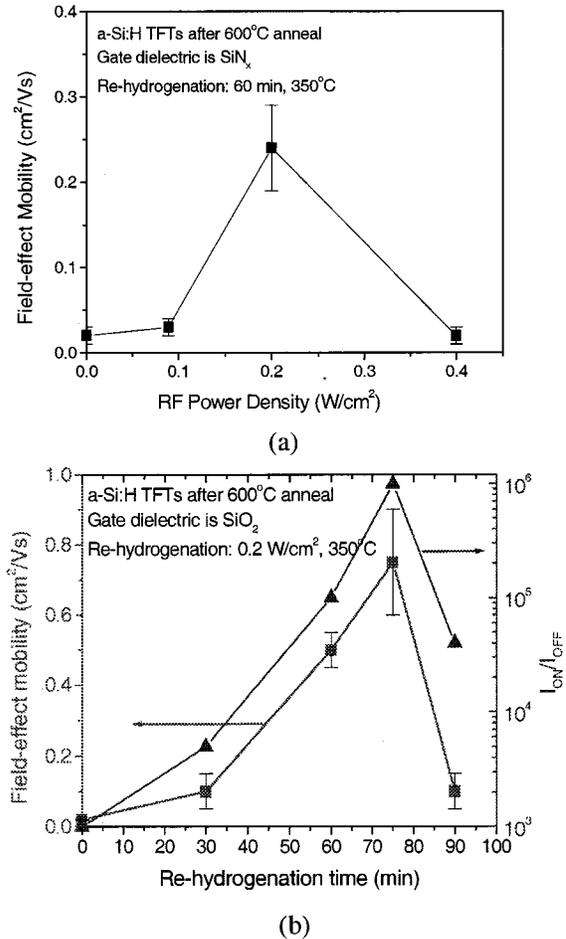


Fig. 3. Field effect mobility of the a -Si:H transistors for different rehydrogenation conditions (a) as a function of rf power (samples 3, 4, and 5) and (b) as a function of exposure time (samples 6, 7, 8, and 9 of Table II).

preferentially etched and the sample a -Si:H is not etched. The dummy coat also helps in conditioning the chamber and making the process invariant to previous history of the chamber. The etching effect of the hydrogen plasma was most severe when the rehydrogenation was done after the active islands were patterned, which reduces the effective area of the a -Si film exposed to the plasma (loading effect).

Fig. 3(a) shows the effect of rf power (samples 3, 4, and 5) and Fig. 3(b) illustrates the effect of plasma exposure time (samples 6, 7, 8, and 9) on μ_n and $I_{\text{ON}}/I_{\text{OFF}}$ of the a -Si:H TFTs, respectively. Increasing the rehydrogenation time beyond 75 min led to significant etching of the a -Si:H film. When the exposure time was increased to 90 min from 75 min, the hydrogen content of the film fell (Fig. 4) from 4.4 at. % to ~ 3 at. % (as measured by IR absorption at 630 cm^{-1}) with a corresponding reduction in field-effect mobility of the a -Si:H TFTs [Fig. 3(b)]. High rf power densities ($> 0.2 \text{ W/cm}^2$) led to etching in spite of all the chamber preparation. When the rf power was too low, the hydrogenation was not efficient, leading to poor field-effect mobility for the a -Si:H TFTs.

The poly-Si TFT characteristics were essentially unchanged as rehydrogenation was not a critical step for them. Any change

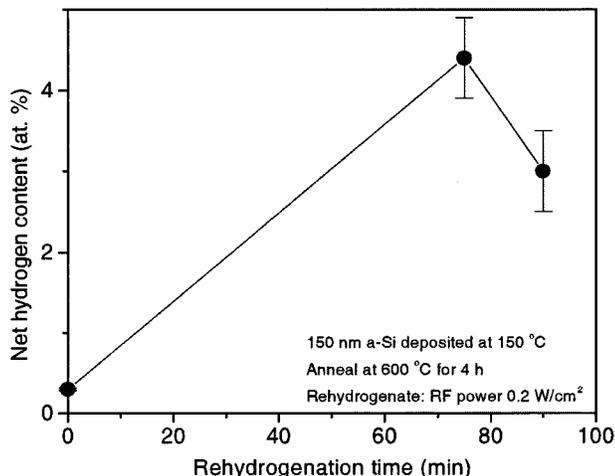


Fig. 4. Net hydrogen content as estimated from the integrated IR absorption near 630 cm^{-1} in the *a*-Si:H films after rehydrogenation for various exposure times. The hydrogen plasma conditions were: rf power density of 0.2 W/cm^2 , pressure of 133 Pa , and hydrogen flow rate of 50 sccm . The growth temperature of the initial *a*-Si:H film was $150\text{ }^\circ\text{C}$, deposited on SiO_2/Si substrate for infrared absorption measurement.

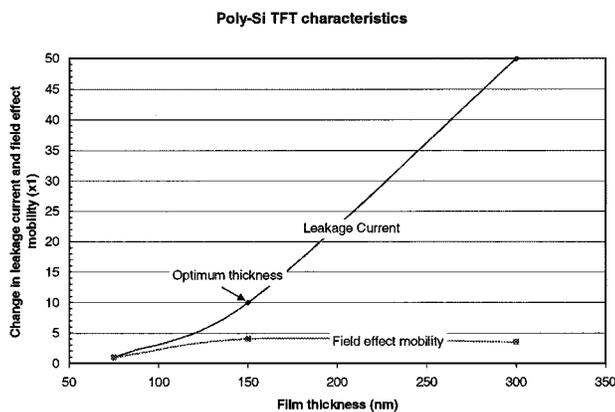


Fig. 5. Field-effect mobility and leakage current in poly-Si TFTs for various initial *a*-Si:H film thickness (samples 4 and 10, 7 and 11, Table II).

observed in the poly-Si performance when only the rehydrogenation conditions were changed (Table II) probably is due to a variation in the percentage of crystallinity of the film after the 4 h anneal at $600\text{ }^\circ\text{C}$.

D. Impact of Other Process Conditions

The OFF currents (I_{OFF}) of the poly-Si and *a*-Si:H TFTs reduced as the thickness the initial *a*-Si:H layer is reduced from 300 nm to 75 nm (Fig. 5). However, the mobility of the transistors also degraded for the thinner samples and 150 nm was found to be the optimum thickness (samples 3, 10, and 11).

When the annealing temperature was increased to $625\text{ }^\circ\text{C}$ from $600\text{ }^\circ\text{C}$, *a*-Si:H TFTs mobility increased to $0.7\text{ cm}^2/\text{Vs}$ from $0.5\text{ cm}^2/\text{Vs}$ for samples 12 and 7, respectively, without change in I_{OFF} . In fact, the higher temperature anneal led to better performance *a*-Si:H TFTs with field-effect mobility as high as $1.2\text{ cm}^2/\text{Vs}$ (Fig. 6), which is the highest reported for

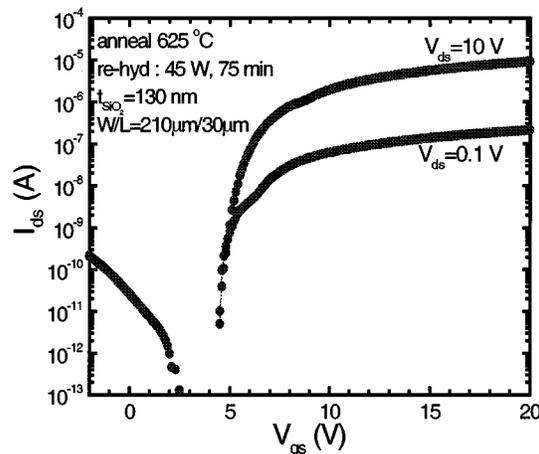


Fig. 6. Best *a*-Si:H TFT subthreshold characteristics for crystallization anneal at $625\text{ }^\circ\text{C}$ and rehydrogenation at 0.2 W/cm^2 for 75 min (sample 13, Table II).

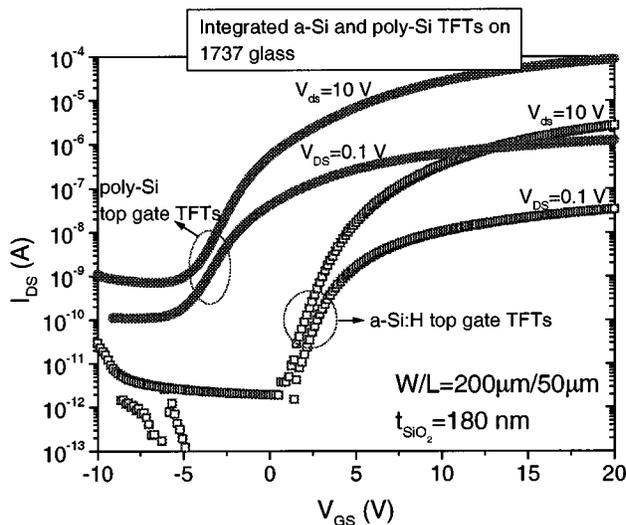


Fig. 7. Subthreshold characteristics of optimized *a*-Si:H and poly-Si TFTs made of the same *a*-Si:H precursor film on Corning 1737 glass substrate (sample 7). Poly-Si by crystallization of *a*-Si:H at $600\text{ }^\circ\text{C}$ in N_2 .

a-Si:H TFTs after a high temperature anneal, when the rehydrogenation time was increased to 75 min (sample 13) from the 60 min (sample 12). However, the field-effect mobilities of the poly-Si TFTs decreased from $15\text{ cm}^2/\text{Vs}$ to $9\text{ cm}^2/\text{Vs}$ for samples 8 and 13, respectively. The optimization of both poly-Si and *a*-Si:H TFTs will require more experiments with time-temperature programs for the crystallization anneal.

Traditionally *a*-Si:H TFTs have been fabricated with bottom gates and SiN_x gate dielectric to obtain the lowest interface state density. This led to improved μ_n and higher $I_{\text{ON}}/I_{\text{OFF}}$ [6]. But poly-Si TFTs are fabricated usually with top gates and SiO_2 as the gate dielectric [22]. Hence, a tradeoff is required. We compared SiN_x and SiO_2 as the gate dielectric in the top gate configuration for both the *a*-Si:H and the poly-Si TFTs. With SiO_2 as the gate dielectric, deposited at $250\text{ }^\circ\text{C}$ by PECVD, from SiH_4 and N_2O , and at rf power density of $\sim 0.1\text{ W/cm}^2$, the poly-Si TFTs had μ_n of $\sim 14\text{ cm}^2/\text{Vs}$ (sample 8). On the

other hand, TFTs with SiN_x as the gate dielectric, deposited at 300 °C by PECVD, using SiH_4 , H_2 and NH_3 , and at a rf power of $\sim 0.09 \text{ W/cm}^2$ had μ_n of $\sim 9 \text{ cm}^2/\text{Vs}$ (sample 3). Although the $\text{SiO}_2/a\text{-Si:H}$ interface state densities are higher than that of the $\text{SiN}_x/a\text{-Si:H}$ interface [23], the leakage currents were not significantly increased when SiO_2 was used as the gate dielectric instead of SiN_x for the $a\text{-Si:H}$ TFTs. But, the I_{ON} and hence μ_n were also higher ($0.5\text{--}1 \text{ cm}^2/\text{Vs}$ compared to $\sim 0.2 \text{ cm}^2/\text{Vs}$) with I_{OFF} of only $\sim 10\text{--}50 \text{ fA}/\mu\text{m}$, when SiO_2 was the gate dielectric instead of SiN_x . Therefore, overall we found SiO_2 to be superior gate dielectric for the fabrication of integrated poly-Si and $a\text{-Si:H}$ TFTs.

All the transistors were annealed in forming gas (10% H_2 in N_2) to reduce the contact resistance between the n^+ $\mu\text{c-Si:H}$ source and drain layers and the aluminum prior to current–voltage ($I\text{--}V$) measurement. In some cases, for the $a\text{-Si:H}$ TFTs without optimized rehydrogenation after the selective crystallization, a hydrogenation using a rf hydrogen plasma at rf power of 0.6 W/cm^2 and exposure time of 60 min reduced I_{OFF} from $\sim 250 \text{ fA}/\mu\text{m}$ to $\sim 30 \text{ fA}/\mu\text{m}$. But there was no change in μ_n of either the poly-Si or the $a\text{-Si:H}$ TFTs (sample 3). This step however, did not lead to such drastic reduction in I_{OFF} of sample 8, which was re-hydrogenated under the optimized conditions as discussed in previously. The implication is that post metal hydrogenation step is essential only if the prior rehydrogenation was incomplete, i.e., not all the dangling bonds in the $a\text{-Si:H}$ layer were passivated.

IV. OPTIMIZED TFT RESULTS

A complete optimization of all process parameters was not possible, but this section describes our best results to date of the $a\text{-Si:H}$ TFTs alone, poly-Si TFTs alone, and their integration.

The best performance of $a\text{-Si:H}$ TFTs in this process flow was achieved when the selective crystallization anneal was done at 625 °C instead of the usual 600 °C. This process yielded $a\text{-Si:H}$ TFTs with field-effect mobilities as high as $1.2 \text{ cm}^2/\text{Vs}$ with ON/OFF current ratio $> 10^7$, subthreshold slope of 0.4 V/decade and threshold voltage of $\sim 6 \text{ V}$ (sample 13, Table II). However, the field-effect mobility of the poly-Si TFTs was lowered to $\sim 9 \text{ cm}^2/\text{Vs}$ compared to $\sim 14 \text{ cm}^2/\text{Vs}$ for the poly-Si TFTs with the 600 °C crystallization anneal (sample 8, Table II).

The best performance for the nonself-aligned poly-Si TFTs was achieved for the process with 600 °C-crystallization anneal with SiO_2 as the gate dielectric. The field-effect mobility of these poly-Si TFTs was $\sim 14 \text{ cm}^2/\text{Vs}$ and the ON/current ratio was $> 10^5$ (sample 8, Table II). With the self-aligned process flow discussed elsewhere [24], for the blanket hydrogen-plasma-treated poly-Si TFTs, higher field-effect mobility and better ON/OFF current ratios of $\sim 33 \text{ cm}^2/\text{Vs}$ and $\sim 10^6$, and $\sim 75 \text{ cm}^2/\text{Vs}$ and $\sim 10^7$ for low temperature ($\leq 600 \text{ °C}$) and high temperature ($\leq 1000 \text{ °C}$) processes, respectively, can be achieved. With a laterally-seeded process flow, the performance of the low-temperature TFTs could be improved even further to achieve field-effect mobility as high as $75 \text{ cm}^2/\text{Vs}$ and ON/OFF current ratio greater than 10^7 [24].

To achieve optimum performance for both poly-Si and $a\text{-Si:H}$ TFTs with the same process flow, several tradeoffs

were required such as, 600 °C anneal instead of 625 °C anneal, SiO_2 instead of SiN_x as the gate dielectric, and the use of nonself-aligned process with deposited n^+ $\mu\text{c-Si:H}$ for source/drain contacts instead of self-aligned process with ion-implanted source/drain contacts. The optimum conditions for the fabrication of the integrated poly-Si and $a\text{-Si:H}$ TFTs after selective crystallization by annealing at 600 °C are those given for sample 8 in Table II. The μ_n in the linear regime were ~ 0.7 and $15 \text{ cm}^2/\text{Vs}$ for the $a\text{-Si:H}$ and poly-Si TFTs, respectively, with SiO_2 as the gate dielectric. I_{OFF} of $a\text{-Si:H}$ TFT is $\sim 10 \text{ fA}/\mu\text{m}$ and I_{ON} of the poly-Si TFT is $\sim 1 \mu\text{A}/\mu\text{m}$, with $I_{\text{ON}}/I_{\text{OFF}}$ of both types of devices $\geq 10^5$ (Fig. 7). These results compare favorably with work on integrating $a\text{-Si:H}$ and poly-Si TFTs by laser processing, which resulted in $a\text{-Si:H}$ TFTs with μ_n of $\sim 0.9 \text{ cm}^2/\text{Vs}$ and poly-Si TFTs with μ_n of $\sim 20 \text{ cm}^2/\text{Vs}$ [9]. These $a\text{-Si:H}$ TFTs also compare favorably with conventional inverted-staggered TFTs, which have μ_n of $\sim 1 \text{ cm}^2/\text{Vs}$ and $I_{\text{ON}}/I_{\text{OFF}} \sim 10^7$ [6]. A typical result for top-gate $a\text{-Si:H}$ TFT with SiN_x as the gate dielectric, is field-effect mobility of $\sim 0.4 \text{ cm}^2/\text{Vs}$ and ON/OFF current ratio of $\sim 10^5$ [25].

V. CONCLUSION

A masked exposure to a rf hydrogen plasma can be used to spatially control the subsequent crystallization of $a\text{-Si:H}$ to poly-Si, resulting in polycrystalline silicon and amorphous silicon areas on the same substrate. The selective crystallization effect has been used to fabricate TFTs in both the poly-Si and $a\text{-Si:H}$ regions in a single layer of silicon for the first time with no laser processing. Careful control of the rehydrogenation process achieved high field-effect mobility in the amorphous silicon after the 600 °C-crystallization process. Optimized transistor fabrication produced good TFT characteristics for both the poly-Si and $a\text{-Si:H}$ TFTs.

APPENDIX

EXTRACTION OF ELECTRICAL PARAMETERS

The I_{OFF} of Table II in all cases was the minimum value of I_{DS} at $V_{\text{DS}} = 10 \text{ V}$ when V_{GS} was scanned from -10 to 20 V . I_{ON} was the maximum I_{DS} at $V_{\text{DS}} = 10 \text{ V}$. The electron field-effect mobility was calculated from the maximum transconductance value ($dI_{\text{DS}}/dV_{\text{GS}}$) at $V_{\text{DS}} = 0.1 \text{ V}$, and threshold voltage was deduced from the intercept of the straight line fit to I_{DS} versus V_{GS} at $V_{\text{DS}} = 0.1 \text{ V}$.

In case of the polysilicon transistors, however, the effect of the source and drain contact resistance cannot be ignored, especially because this is not a self-aligned TFT and the source/drain contacts are not co-planar with the channel. In the linear region ($V_{\text{DS}} = 0.1 \text{ V}$) the drain to source current is given by

$$I_{\text{DS}} = \frac{\mu_{\text{eff}} C_{\text{ox}} W}{L} [V_{\text{DS}} (V_{\text{GS}} - V_{\text{TH}})]. \quad (1)$$

With contact resistance of R_D and R_S at the drain and source ends, and assuming a symmetric device with $R_D = R_S$, (1) can be rewritten as (ignoring second-order terms)

$$I_{\text{DS}} \approx \frac{kV_{\text{ds}}(V_{\text{GS}} - V_{\text{TH}})}{1 + 2kR_S(V_{\text{GS}} - V_{\text{TH}}) + kR_S V_{\text{DS}}} \quad (2)$$

where $k = \mu_{\text{eff}} C_{\text{ox}} W/L$ and R_S is the contact resistance at the source/drain. Equation (2) can be used to perform a least square fit of the data and the values of k , V_{TH} , and R_S can be extracted for one device of one channel length. For polysilicon TFTs, R_S was found to be as high as 300 k Ω in some cases for channel width of $\sim 200 \mu\text{m}$, which means that (1) would have resulted in a pessimistic estimate of μ_{eff} . Table II lists the values of field-effect mobility for the poly-Si TFTs calculated from (2). For the α -Si:H TFTs, on the other hand, the effect of the source/drain resistance was negligible as the channel conductance and mobilities are much lower than for the poly-Si TFTs.

ACKNOWLEDGMENT

The authors would like to thank Y. Chen for help in the TFT fabrication.

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