Suppression of Boron Penetration in P-Channel MOSFETs Using Polycrystalline $Si_{1-x-y}Ge_xC_y$ Gate Layers

E. J. Stewart, M. S. Carroll, and James C. Sturm, *Fellow, IEEE*

***Abstract*—Boron penetration through thin gate oxides in p-channel MOSFETs with heavily boron-doped gates causes undesirable positive threshold voltage shifts. P-channel MOSFETs with polycrystalline $Si_{1-x-y}Ge_xC_y$ gate layers at the gate-oxide interface show substantially reduced boron penetration and increased threshold voltage stability compared to devices with all poly Si gates or with poly $Si_{1-x}Ge_x$ gate layers. Boron accumulates in the poly $Si_{1-x-y}Ge_xC_y$ layers in the gate, with less boron entering the gate oxide and substrate. The boron in the poly $Si_{1-x-y}Ge_xC_y$ appears to be electrically active, providing similar device performance compared to the poly Si or poly $Si_{1-x}Ge_x$ gated devices.**

***Index Terms*—Annealing, boron, charge carrier mobility, MOSFETs, silicon alloys, stability.**

I. Introduction

P-CHANNEL MOSFETs with heavily boron-doped gates and thin gate oxides are susceptible to boron penetration through the gate oxide during postimplant anneals, resulting in undesirable positive threshold voltage shifts [1], [2]. Previously, it was reported that PMOS capacitors with thin polycrystalline $Si_{1-x-y}Ge_xC_y$ layers in the gates show significantly reduced boron penetration [3]. In this letter, we report p-channel MOSFETs with polycrystalline $Si_{1-x-y}Ge_xC_y$ gate layers. The main contributions of this letter are to show i) that devices with poly $Si_{1-x-y}Ge_xC_y$ gate layers have substantially reduced boron penetration and increased threshold voltage stability compared to devices with all poly Si gates or with poly $Si_{1-x}Ge_x$ gate layers, consistent with previous capacitor results, ii) the transconductance of the devices is well-behaved and consistent with the model of reduced boron penetration, and iii) the segregation of boron to poly $Si_{1-x-y}Ge_xC_y$ layers with high C levels is a possible mechanism for allowing less boron into the gate oxide and substrate. This combines to give a high boron level at the gate oxide interface for low gate depletion.

II. Device Fabrication and Characteristics

Field oxides (~500 nm) were first grown and patterned on n-type substrates (~1×10^{15} cm^{-3}), followed by ~7-nm gate oxidation in dry O_2 at 900 °C. Poly gate deposition was then performed by RTCVD at 625 °C, 700 °C, and 750 °C using SiH_4 and $SiCl_2H_2$ as silicon sources and GeH_4 and $SiCH_6$ as germanium and carbon sources, respectively. The first 60 nm of each gate was either poly $Si_{1-x-y}Ge_xC_y$ (12% Ge, 0.35% C), poly $Si_{1-x}Ge_x$, or poly Si; the remainder in all samples was poly Si, with a total gate thickness of ~500 nm (inset Fig. 1). Gates were patterned with gate lengths ranging from 2 μm to 50 μm. Gate, source, and drain for all samples were then simultaneously implanted with 2×10^{15} $cm^{-2}BF_2^+$ at 60 keV and annealed at 900 °C in N_2 for 20, 60, or 100 min to allow for boron activation and diffusion, followed by a standard backend process. Electrical characteristics and SIMS profiles were obtained to examine boron penetration and threshold voltage stability in all devices.

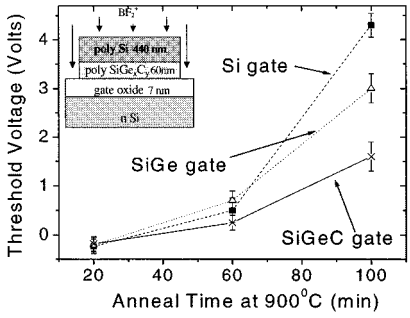

Fig. 1. Threshold voltage versus anneal time. All threshold voltages were extracted by the extended slope method on an I_D versus V_G plot ($V_{DS} = -0.1$).

Devices with $Si_{1-x-y}Ge_xC_y$ gate layers have substantially reduced boron penetration and increased threshold voltage stability compared to devices with all Si gates or with $Si_{1-x}Ge_x$ gate layers. Fig. 1 shows threshold voltage versus anneal time for these devices. All devices experience positive threshold voltage shifts with increasing anneal time, indicating boron penetration into the substrate. However, after 100 mins of annealing, the Si and $Si_{1-x}Ge_x$ gates have threshold voltages of 4.1 V and 3.0 V, respectively, whereas the $Si_{1-x-y}Ge_xC_y$ gate threshold voltage remains at 1.6 V. Furthermore, after the 100 min anneal, the Si and $Si_{1-x}Ge_x$ gates cannot be fully turned off, indicating enough boron has entered the substrate to prevent it from being fully depleted out. The $Si_{1-x-y}Ge_xC_y$ gates, however, for up to 100 min of annealing, maintain similar on/off currents as for shorter anneal times. Fig. 2 shows subthreshold characteristics for the 100 min annealed devices.

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The authors are with the Center for Photonics and Optoelectronic Materials, Department of Electrical Engineering, Princeton University, Princeton, NJ 08544 USA (e-mail: estewart@ee.princeton.edu).

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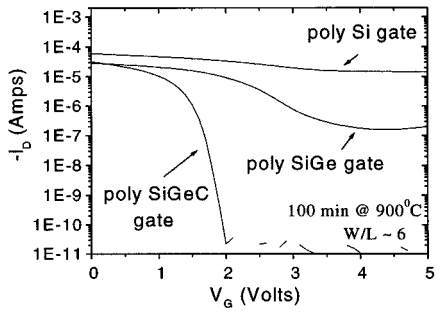

Fig. 2. Typical subthreshold characteristics after 100 min anneal.

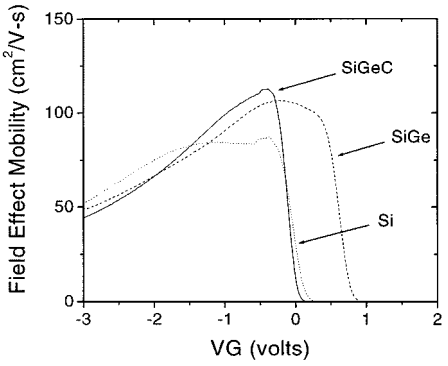

Fig. 3. Extracted mobility versus gate voltage for the 60 min anneal time.

Previously, improvement in threshold voltage stability in p-MOSFETs using p^+ poly $Si_{1-x}Ge_x$ gates has been reported [4]. However, as shown in Figs. 1 and 2, $Si_{1-x-y}Ge_xC_y$ gate layers show additional stability over the $Si_{1-x}Ge_x$ gate layers.

Field effect mobilities were examined to investigate the electrical activation of the boron in the $Si_{1-x-y}Ge_xC_y$ gates. Mobilities were extracted from the peak value of a dI_D/dV_g plot with $V_{DS} = -0.1$, assuming a constant gate capacitance equal to the oxide capacitance. Fig. 3 shows extracted mobility versus gate voltage for the 60 min annealed devices. Note the double peak beginning to appear in the Si and $Si_{1-x}Ge_x$ device plots, which indicates a buried channel starting to form due to large amounts of boron penetration [5]. Gate voltage was plotted instead of effective field because in buried channel devices the inversion layer charge, and hence E_{eff}, is not easily calculated due to the unknown effective gate capacitance. Fig. 4 shows the extracted mobility versus anneal time (points represent an average of over ten devices, with error bars showing the standard deviation). If the boron in the poly $Si_{1-x-y}Ge_xC_y$ gate layers is not active, large gate depletion might be expected to occur during turn-on as the gate voltage becomes negative. This would cause a drop in actual gate-channel capacitance, resulting in a smaller extracted mobility. Within error bars, however, the $Si_{1-x-y}Ge_xC_y$ gate devices do not show any decrease in extracted mobility compared to the Si gates, indicating the boron in the gates is electrically active. All device structures do exhibit some loss in extracted mobility with increasing anneal time. Decreased mobility has been previously observed with increasing boron penetration, and may be due to increased carrier scattering in the channel [6], [7]. Mobility does not decrease as rapidly with time for the $Si_{1-x-y}Ge_xC_y$ gates compared to the Si or

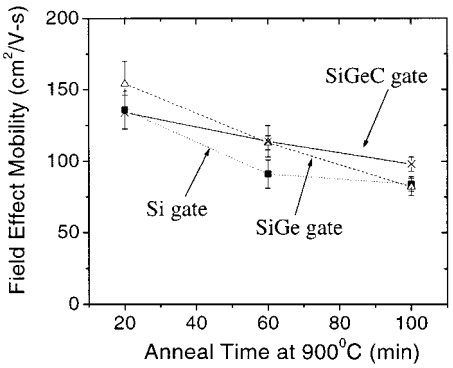

Fig. 4. Extracted peak mobility versus anneal time.

$Si_{1-x}Ge_x$ gates, however, consistent with less boron penetration in those devices.

III. Discussion

To probe what causes the suppressed boron penetration in the $Si_{1-x-y}Ge_xC_y$ gates, SIMS profiles of boron concentration versus depth were taken for the Si and $Si_{1-x-y}Ge_xC_y$ gates after the 20 and 100 min anneals. Profiles after the 20 min anneal are similar for the Si and $Si_{1-x-y}Ge_xC_y$ [Fig. 5(a)] devices, with boron concentration roughly flat throughout the gate at a level of $\sim 6 \times 10^{19}\text{cm}^{-3}$. While boron has a very low diffusion coefficient in *crystalline* $Si_{1-x-y}Ge_xC_y$ layers, it can clearly enter polycrystalline $Si_{1-x-y}Ge_xC_y$ layers without difficulty. This is presumably due to grain boundary mechanisms. After 100 mins of annealing, however, boron has started to accumulate in the $Si_{1-x-y}Ge_xC_y$ layer in the $Si_{1-x-y}Ge_xC_y$ samples, with the ratio of boron concentration in the $Si_{1-x-y}Ge_xC_y$ to that in the Si equal to $\sim$1.3 [Fig. 5(b)]. In the Si sample, the boron profile remains roughly flat and unchanged from the 20 min anneal (the Si profiles are not shown for brevity). This accumulation in the $Si_{1-x-y}Ge_xC_y$ layers should have the effect of keeping more total boron in the gate for a given anneal time, since more boron remains in the $Si_{1-x-y}Ge_xC_y$ layer and less penetrates into the oxide and substrate. Although difficult to resolve from the SIMS plots, for the 100 min anneal time the total amount of boron in the top 100 nm of the substrate is $\sim 1 \times 10^{12}\text{cm}^{-2}$ higher in the Si-gated device versus the $Si_{1-x-y}Ge_xC_y$-gated device, consistent with enhanced boron penetration in the Si-gated device.

It has been previously reported that in single crystal $Si_{1-x-y}Ge_xC_y$ (with similar Ge and C levels), boron diffusion can be an order of magnitude slower than in either single crystal Si or $Si_{1-x}Ge_x$ [8]. Slower boron diffusion has also been reported in polycrystalline $Si_{1-x}Ge_x$ compared to Si [9]. This raises the possibility that in the polycrystalline $Si_{1-x-y}Ge_xC_y$ gate samples, boron is simply taking longer to diffuse through the poly $Si_{1-x-y}Ge_xC_y$ layer before penetrating into the oxide. This might predict lower extracted field effect mobilities in the $Si_{1-x-y}Ge_xC_y$ devices for short anneal times, since there would be less dopant at the gate-oxide interface and therefore more gate depletion. Gate depletion was not observed in capacitance–voltage *(C–V)* measurements, however [3], and the FET mobility results in this paper show no detectable loss in performance in the $Si_{1-x-y}Ge_xC_y$ devices versus the Si or $Si_{1-x}Ge_x$ devices. Furthermore, the SIMS data show similar

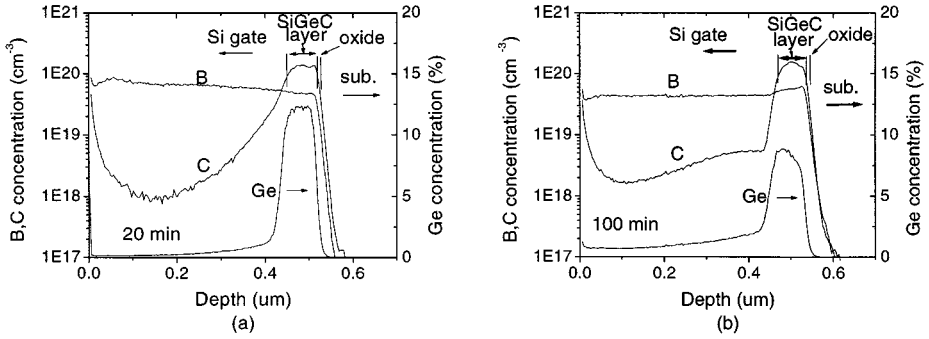

Fig. 5. SIMS profiles for Si/$Si_{1-x-y}Ge_xC_y$ gate after (a) 20 min anneal and (b) 100 min anneal.

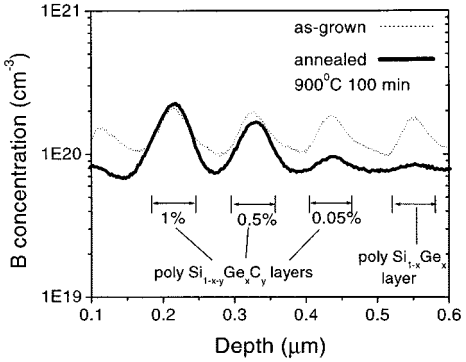

Fig. 6. Boron concentration profiles of $Si_{1-x-y}Ge_xC_y$/Si multi-layer sandwich structure before and after annealing at 900 °C for 100 mins in N_2.

boron concentrations at the gate-oxide interface after the 20 min anneal for the Si and $Si_{1-x-y}Ge_xC_y$ devices; after the 100 min anneal, boron levels are actually higher at the gate-oxide interface in the $Si_{1-x-y}Ge_xC_y$ samples. (As an aside, note that there was substantial diffusion of Ge out of the $Si_{1-x}Ge_x$ layer to the entire polycrystalline gate layer at 100 min [Fig. 5(b)], although the total amount of Ge was conserved. Like boron, apparently Ge (but not carbon) can diffuse relatively fast in polycrystalline layers.)

A separate experiment confirms strong boron segregation to poly $Si_{1-x-y}Ge_xC_y$ layers with high C levels annealed under these conditions. A multi-layer structure was grown, consisting of several poly $Si_{1-x-y}Ge_xC_y$ layers (Ge~20%, carbon percentages varied from 0 to 1%) sandwiched between poly Si layers. All layers were *in-situ* doped with boron at about 10^{20} cm^{-3}. This sample was annealed at 900 °C for 100 min in N_2, and SIMS profiles taken before and after the anneal (Fig. 6). Before the anneal, the poly $Si_{1-x-y}Ge_xC_y$ layers are *in-situ* doped slightly higher than the poly Si layers. If there were no segregation, this profile would be expected to flatten out during the anneal. However, in the $Si_{1-x-y}Ge_xC_y$ layer with the highest carbon level (1%), boron concentration actually increases during the anneal (ratio of boron concentration in this layer versus the adjacent poly Si layers after the anneal was ~3.2), indicating strong boron segregation to this layer. Segregation to $Si_{1-x}Ge_x$ was much weaker ($m = 1.1$), consistent with previous reports of boron segregation to single crystal $Si_{1-x}Ge_x$ from Si [10]. This further supports the hypothesis that the enhanced threshold voltage stability presented in this letter is due primarily to boron segregating to the $Si_{1-x-y}Ge_xC_y$ layers, and not due to a potentially lower diffusion coefficient.

IV. Summary

In conclusion, thin polycrystalline $Si_{1-x-y}Ge_xC_y$ gate layers are effective at suppressing boron penetration in p-channel MOSFETs and thus improving threshold voltage stability. Boron preferentially segregates to the $Si_{1-x-y}Ge_xC_y$ layers in the gate during postimplant anneals, and we believe this segregation is the driving force preventing boron from entering the gate oxide and substrate. Other than a suppression of boron penetration, the electrical behavior of the devices does not appear affected by the presence of C in the gate layers. Future work must examine poly $Si_{1-x-y}Ge_xC_y$ gates with thinner gate oxides and shorter, higher temperature anneals.

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