

Low-Temperature Preparation of Oxygen- and Carbon-Free Silicon and Silicon-Germanium Surfaces for Silicon and Silicon-Germanium Epitaxial Growth by Rapid Thermal Chemical Vapor Deposition

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Photoluminescence (PL) from commensurately strained SiGe layers grown directly on silicon substrates and secondary ion mass spectroscopy (SIMS) of buried Si/SiGe interfaces are used to evaluate different low-temperature cleaning methods of substrate surfaces for silicon and SiGe epitaxy in a nonultrahigh vacuum system. Both the sources of contamination as well as effective cleaning methods were investigated. The dominant source of contamination came from the wafer being outside the reactor, not in the load lock or deposition chamber itself. The optimum surface preparation depends on the ratios of HF, NH₄F, and deionized water of solutions that were used to remove the wet chemical oxide on the substrate surface. *In situ* bakes between 300 and 800°C in 0.25-250 Torr of hydrogen were examined after the *ex situ* clean using PL and SIMS measurements. An optimized *ex situ* clean [1:1000 HF(49%):deionized water (DI)] and *in situ* hydrogen bake (2 min at 800°C in 10 Torr) produces an oxygen- and carbon-free surface for silicon and SiGe epitaxy.

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Small thermal budgets for silicon processing are increasingly demanded by ultralarge scale integration (ULSI) technologies for various reasons such as the control of dopant diffusion. The desire to integrate SiGe-based heterojunction bipolar transistor (HBT) technologies with silicon complementary metal-oxide-semiconductor (CMOS) technology has introduced a new demand for low thermal budget Si/SiGe epitaxy.¹ It is now established that high quality silicon epitaxy can be grown by chemical vapor deposition (CVD) at relatively low temperatures ranging between 500-800°C, despite these temperatures being too low to desorb contaminants rapidly enough, such as oxygen, from the surface of the silicon during the silicon epitaxy.^{2,3} The low-temperature CVD growth of silicon is achieved by relying on either low partial pressures of contamination such as water vapor or hydrogen passivation to reduce the sticking coefficient of the contamination. However, an initial clean substrate surface is necessary for high-quality structures. Traditionally, CVD methods have relied on high temperature *in situ* cleaning steps such as hydrogen prebakes at 1000°C. Such temperatures often are unacceptable if there are already dopant device profiles in the substrate.

Several groups have reported oxygen- and carbon-free surfaces for subsequent epitaxy prepared by *in situ* hydrogen prebakes between 760-850°C after an *ex situ* wet clean. However, there is special emphasis in these reports on ultrahigh vacuum requirements and dry-pumped loading systems, and all of the reported cleaning procedures depend on wet chemical preparation that are not compatible with the exposed SiGe surfaces. In ultrahigh vacuum (UHV)CVD, no cleaning step at all beyond a wet *ex situ* clean (*e.g.*, an HF dip) is required for high quality epitaxy at 760°C, but often residual carbon and oxygen contamination still are found at the interface.⁴ In this paper we study the dependence of surface quality on *ex situ* wet cleaning and *in situ* hydrogen baking steps compatible with SiGe surfaces, without the need for UHV in the deposition chamber. Secondary ion mass spectroscopy (SIMS) of buried interfaces and photoluminescence (PL) from thin buried SiGe layers are used to measure contamination. We present a low-pressure cleaning technique compatible with SiGe surfaces that reduces oxygen and carbon contamination below the detection limits of SIMS for a rapid thermal chemical vapor deposition system (RTCVD) using only conventional rotary vane pumps.

This paper is divided into four parts. First, the standard procedure for epitaxial growth and interface characterization are described. Second, *ex situ* wet cleaning steps were examined. The third section

focuses on contamination introduced by the reactor and load lock. Finally the effect of *in situ* bakes before growth is examined in the section on Contamination from Reactor, Load-Lock, and Laboratory Environment.

Standard Growth and Characterization Procedures

Cleaning and growth procedures.—Standard growth procedures are now described. First, the wafers were chemically cleaned, beginning with the removal of the native oxide from p-type wafers (5-50 Ω-cm) using a ~5 min dilute HF dip [1:100 HF(49%):DI]. The surface was then chemically oxidized by immersing the wafer in H₂SO₄:H₂O₂(30%)1:1 at 70°C for 20 min. The oxide was then removed using an HF-based etch which leaves the surface hydrogen terminated.^{5,6} Unless otherwise noted, the HF(49%) to DI ratio for this last step was 1:1000. After the last HF step, the wafer was not rinsed in DI water, except when noted. The DI water resistivity was ~18 MΩ-cm, the total organic content (TOC) was <50 ppb, and the laboratory temperature was between 21 and 24°C with a relative humidity below 50%. All chemicals were obtained from J. T. Baker and were CMOS electronic grade. No precaution was taken to avoid dissolved oxygen in the DI water.⁷

Following the wet clean the wafer was placed on a quartz stand in the load-lock of the growth reactor, which was evacuated to ~50 mTorr by a standard rotary-vane mechanical pump. Three or four pump-purge cycles on the load-lock were performed before the wafer was introduced to the growth chamber. The pump-purge cycle consists of filling the load-lock to ~1 Torr with dry nitrogen before evacuation, and one cycle took an average of approximately 5 min. The wafer was then transferred to the growth chamber, which was kept between 1 and 10 Torr of hydrogen.

The growth chamber was a cold-wall system, using a bank of tungsten-halogen lamps to radiatively heat the wafer through a quartz tube. Immediately following the wafer transfer from the load-lock to the reactor, a flow of 1 slpm of hydrogen was passed through the reactor while the reactor pressure was maintained at 1 Torr. The hydrogen was purified through a Nanochem 3000 (Semi-Gas Systems, Inc., San Jose, CA) purifier, which is specified to reduce the impurity concentrations in the hydrogen to less than ten parts per billion (ppb). The growth of silicon and silicon-germanium layers was done by rapid thermal chemical vapor deposition (RTCVD)³ using dichlorosilane and germane as source gases and hydrogen as the carrier gas.

For our standard growth, a high-temperature clean (to desorb oxygen) in hydrogen at 250 Torr at 1000°C was then performed, followed by the growth of a high-temperature Si buffer layer at 1000°C.

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Low-temperature (e.g., 625°C for SiGe or 700°C for Si) layers were then grown following the buffer. The 1000°C cleaning step and buffer layer were frequently omitted or modified in the work described in this paper, since our goal was to develop cleaning steps which would not cause the diffusion of any existing dopant profiles. Silicon and SiGe layers are typically grown at 6 Torr in a 3 slpm hydrogen carrier with 26 sccm dichlorosilane and varying germane levels.

Characterization of interfaces.—All Si/SiGe interfaces were characterized using PL from the pseudomorphically strained SiGe layers, which were immersed in a bath of liquid nitrogen after growth. An argon ion laser tuned to 514 nm was used as the excitation source, and a liquid-nitrogen-cooled Ge detector combined with a lock-in amplifier was used to measure the emitted light. The pump power density was approximately ~ 50 mW/cm². Most of the minority carriers are generated in the substrate, and then diffuse to the SiGe quantum well.⁸ Therefore, the technique is best suited for structures without any barriers for carrier flow from the absorption region, a few micrometers into the substrate, to the SiGe layer. A typical spectrum is shown in Fig 1. Luminescence intensity from the strained SiGe layer is extremely sensitive to the carrier lifetime in the SiGe layer.^{3,9} Therefore any defects or contamination at the Si/SiGe interfaces which lead to increased nonradiative recombination of excited carriers reduce the overall luminescence intensity emitted from the Si_{1-x}Ge_x layer. The total integrated SiGe luminescence was normalized to the total integrated luminescence from the bulk silicon to account for any lifetime variation in the silicon substrates that would affect the PL intensity from the SiGe layer.

Some buried interfaces were also characterized using SIMS done at Evans East (East Windsor, NJ) using a 3 keV Cs⁺ primary ion beam. Sputter rates were between 5-15 Å/s, producing oxygen and carbon detection limits of approximately 10¹⁸ and 10¹⁷ cm⁻³, respectively, for most samples. Sputter rates were determined using profilometry leading to $\sim 5\%$ uncertainty in depth profiles, and chemical species concentrations were measured to within 15% error.

Different cleaning procedures resulted in some interfaces that were contaminated with carbon or oxygen. In these samples with higher oxygen or carbon levels at the Si/SiGe interfaces, the PL

intensity from the SiGe decreased, presumably due to recombination sites caused by the contamination (Fig. 1). Therefore, in this work the PL intensity is often used as a probe of interfacial cleanliness since data can be obtained more quickly than with SIMS. It also directly measures the electrical quality of the SiGe.

Ex situ Wet Cleaning

Introduction.—In this section, the chemical wet treatment performed on the wafer before being loaded into the reactor was studied and optimized. The treatment serves to remove the majority of surface contaminants and to passivate the surface against further contamination. p-Type silicon (100) surfaces were prepared with a series of different wet-cleaning methods. They were then loaded into the reactor, followed by growth of a thin ~ 200 Å Si_{0.8}Ge_{0.2} layer without any *in situ* cleaning step or buffer layers directly above the wet-cleaned surface. A 450 Å silicon layer was subsequently grown above the Si_{0.8}Ge_{0.2} layer. Thus carriers in the Si_{0.8}Ge_{0.2} layer are subject to effects of contamination on the original Si surface. In this set of experiments no *in situ* high-temperature cleaning process or high-temperature silicon buffer was grown, since our goal was to study the effect of only the wet clean.

After transferring the wafer from the load-lock to the growth chamber, the hydrogen flow rate was increased to 3 slpm and the pressure was raised to 6 Torr, followed by heating the wafer to the growth temperature of 625°C over a period of 2 min. When the growth temperature was reached, dichlorosilane is injected into the reactor chamber (in addition to the already flowing hydrogen) followed by germane injection approximately 5 s later, to grow the SiGe layer, at a growth rate of ~ 100 Å/min. Following the growth of the SiGe layer, the Ge source was turned off and a Si capping layer was grown after raising the temperature to 700°C for 15 min.

Germane is known to react with silicon dioxide to form the volatile species GeO_x. Oxide removal using germane at temperatures of 650-700°C has been reported.¹⁰ These reports found, however, that for submonolayer oxides, germanium adsorbs preferentially to the bare silicon surface rather than forming the volatile germanium-oxide.¹⁰ The sequence of dichlorosilane followed by germane was chosen to allow the SiGe layer to grow as soon as the germane was injected. Because the SiGe layer grows quickly on the silicon surface with no observable long incubation time, and the germane molecule prefers the open silicon surface site over that of the oxide site, it is concluded that the germane-induced oxide desorption has a negligible effect on the total oxygen concentrations buried at the interface between the silicon surface and the SiGe layer.

Following the initial HF dip and chemical oxidation as described earlier, the concentration (and thus pH) for the final HF step before loading was varied. The wafer was dipped in a final oxide etch with a pH of 1-7.8 for a minimum of 20 min. The HF to DI ratio for this final oxide stripping step was varied from 1 to a 1000 parts DI to one part HF (49%) (pH between 1 and 3) to determine the effect of the HF concentration. Less acidic solutions were also examined, using HF buffered with NH₄F (pH ~ 4) or slightly basic 40% NH₄F (pH ~ 7.8) instead of HF and water. Although the wafer surface becomes hydrophobic at shorter times [~ 10 min in 1:1000 HF(49%) in DI], the minimum 20 min etch time was chosen to insure sufficient time for the oxide removal reaction to go to completion. PL from Si_{1-x}Ge_x layers grown above surfaces that were rinsed in DI after an HF dip [1:1000 HF(49%) in DI] were completely quenched. Presumably, dissociated OH⁻ ions oxidize the silicon surface^{11,12} resulting in a poor Si/SiGe interface, which quenches the PL from the Si_{1-x}Ge_x layer. Therefore, after the dilute HF dip step any residual droplets on the mostly dry surface were blown off with nitrogen, but not rinsed. However, no SIMS or further work was done to confirm this hypothesis. The hydrogen passivated surface was then exposed to laboratory atmosphere for 1-20 min before loading into the load-lock. High quality interfaces were achieved even after 15-20 min of exposure to air, indicated by intense PL from Si_{1-x}Ge_x layers grown above the exposed surface.

A monotonic increase in the relative PL intensity from the Si_{0.8}Ge_{0.2} layer was found as the HF concentration was decreased

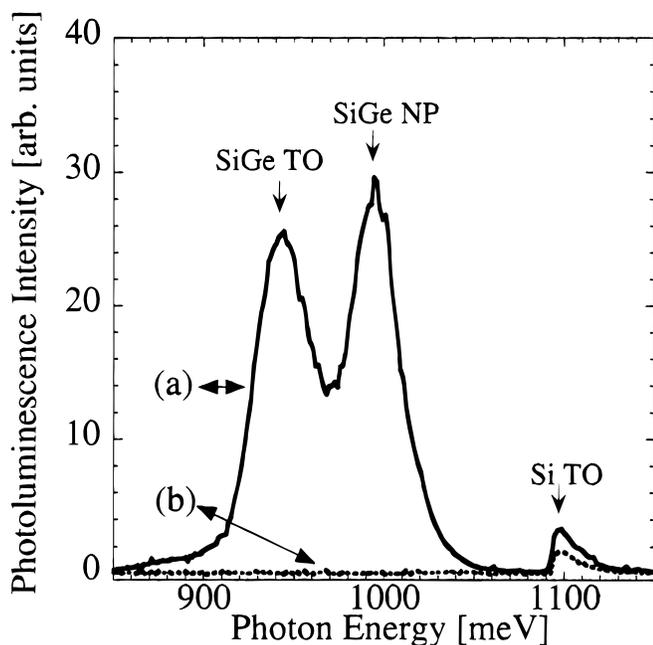


Figure 1. Typical photoluminescent spectrum at 77 K of a clean Si_{0.8}Ge_{0.2} 200 nm silicon layer capped with silicon. Sample (a) has an integrated contamination of carbon and oxygen below SIMS detection limits, while (b) has an integrated contamination of 2×10^{12} and 1×10^{14} cm⁻² of carbon and oxygen, respectively.

(Fig. 2), indicating less contamination. However solutions more basic than the most dilute HF dip led to a decrease in luminescence intensity from the $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer ($\text{pH} > 3$). This optimum treatment of $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ (70°C, 20 min) followed by a 1:1000 HF/DI dip (after removing the native oxide using a 1:100 HF/DI dip) was also applied directly to a $\text{Si}_{0.8}\text{Ge}_{0.2}$ surface. The $\text{Si}_{0.8}\text{Ge}_{0.2}$ surface was grown at 625°C on top of a 1000°C Si buffer followed by removing the exposed $\text{Si}_{0.8}\text{Ge}_{0.2}$ surface from the reactor and leaving it in the laboratory atmosphere for 3 days. The $\text{Si}_{0.8}\text{Ge}_{0.2}$ surface was then treated with the same wet clean as that used for the pure silicon surfaces followed by reinserting the $\text{Si}_{0.8}\text{Ge}_{0.2}$ surface into the reactor for the 700°C growth of a Si cap without any hydrogen baking. The PL intensity from the resulting structure was more intense, 7.4, than the case where the pure silicon surface was cleaned followed by a silicon capped $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer, 3.8 (Fig. 2). Thus we conclude the combination of $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ and 1:1000 HF/DI dip is also effective in preparing clean SiGe surfaces.

SIMS was available for silicon surfaces, which were not subjected to the standard wet chemical clean, but rather were prepared by silicon growth in the RTCVD reactor. The wafers were then removed from the reactor and immersed for various times in either 1:10 or 1:100 HF(49%):DI (pH of 1.4 or 1.9, respectively). The samples were then returned to the reactor through the standard loading procedure. The surfaces were then buried under an epitaxial SiGe layer and Si cap as described earlier in this section. The integrated carbon and oxygen levels are about five times higher for a pH of 1.4 than 1.9, and fluorine is only found for pH of 1.9 (Fig. 3).

This decrease in contamination as pH is raised (to at least to pH of 3) may be related to the fact that (111) microfaceting of the (100) silicon surface is known to increase with increasing pH,¹³ due to anisotropic etching by OH^- ions.^{14,15} The resulting monohydride-terminated (111) surface has an oxygen sticking coefficient about one-hundred times lower than the dihydride-terminated (100) hydrogen-passivated surface.¹⁶⁻¹⁸ Therefore less contamination and an increase in SiGe PL would be expected with increasing pH and increased microfaceting.

The increased fluorine contamination with increasing HF concentration has previously been observed.¹⁹⁻²¹ The observed increase in carbon contamination at low pH could also be due to organic content in the process chemicals, which would increase with increased process chemical concentrations.^{19,20} The reason for the decrease in

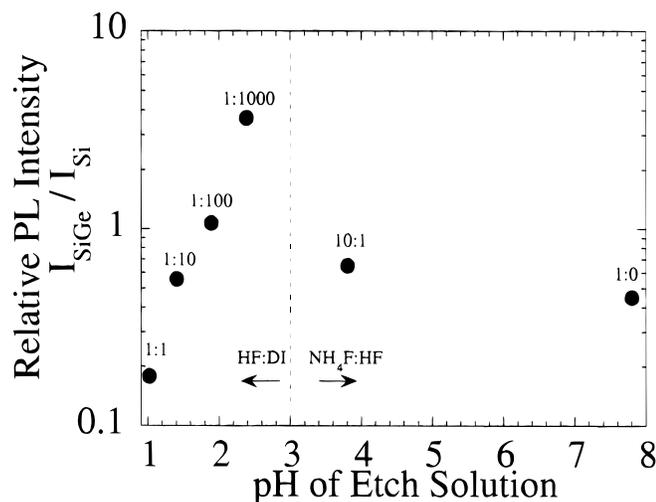


Figure 2. Relative photoluminescence SiGe/Si (PL) intensity at 77 K from commensurately strained $\text{Si}_{0.8}\text{Ge}_{0.2}$ alloys followed by silicon caps grown directly above wet chemically treated silicon surfaces vs. the pH of the solution used to etch the wet chemical oxide on silicon. The ratios of either HF (49%) to DI water, or NH_4F (40%) to HF (49%) are indicated above their respective points. In one case the HF dip was also done instead on top of SiGe, followed by a 700°C Si cap.

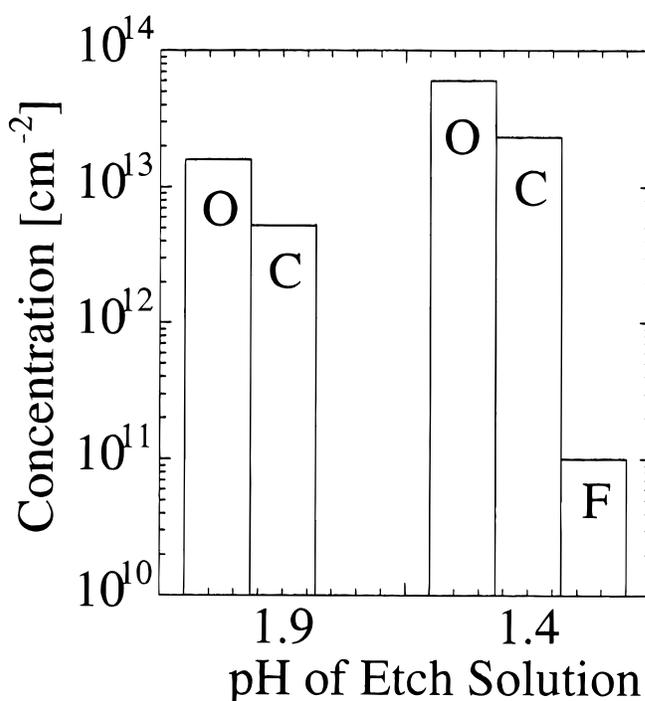


Figure 3. The carbon, oxygen, and fluorine concentrations detected by SIMS at Si/SiGe interfaces from SiGe layers grown directly at 625°C on Si surfaces treated with HF:DI solution of pH 1.4 and 1.9 to remove the wet chemical oxide, without a hydrogen prebake.

SiGe PL at pH greater than 3 is not known. Silicon substrates cleaned with NH_4F have been reported to have an increased density of crystallographic defects in the epitaxial silicon grown above the prepared surface,²² which could be responsible for the reduced PL. However, the epitaxial films were not examined for crystallographic defects, therefore, different surface termination or impurities from the NH_4F solution cannot be ruled out as causes for the PL quenching.

Contamination from Reactor, Load-Lock, and Laboratory Environment

Experiment.—In our system, wafers are introduced to the growth chamber through a load lock, which is pumped by a rotary vane pump using hydrocarbon-based oil. The load-lock was therefore examined as a source of carbon contamination. Clean pseudomorphically strained $\text{Si}_{0.8}\text{Ge}_{0.2}$ surfaces were prepared by growing a silicon epitaxial buffer layer followed by a thin 200 Å $\text{Si}_{0.8}\text{Ge}_{0.2}$ layer. Immediately after growth, the chamber was purged with a continuous flow of 3 slpm of hydrogen at 6 Torr. The wafer was allowed to cool for 15 min before being moved to the load-lock where parts or all of the loading procedure were simulated. After transferring back to the growth chamber, the wafer was then heated to 700°C (ramp rate 50°C/s) in 3 lpm H_2 , and after ~15 s at 700°C dichlorosilane was switched on to grow an epitaxial silicon cap (45 nm). No high-temperature cleaning steps in excess of 700°C were used. The upper SiGe/Si interface was then examined by SIMS and PL to look for contamination introduced by the load-lock.

Four experiments on SiGe surfaces were done before returning the wafer to the deposition chamber for a capping silicon layer: trial A: leave wafer in reactor; trial B: transfer wafer to load-lock + simulate load-lock pump-down; trial C: trial B + vent load-lock to atmosphere + load-lock pump-down; and trial D: trial C, except the wafer is moved to the fume hood.

To first determine whether the growth chamber itself contributes any contamination to the surface (apart from the load-lock), the SiGe layer wafer A was simply left in the growth chamber without being transferred to the load-lock. The wafer was allowed to cool in 3 slpm of H_2 at 6 Torr for 15 min. This time exceeds the time required to

transfer the wafer to the load-lock and therefore simulates a maximum contribution of the growth chamber's contamination to the wafer surface. The wafer was then reheated to 700°C, and a silicon cap was grown as described above. No oxygen or carbon was detected by SIMS at the interrupted SiGe/Si interface (Fig. 4, 6). This layer exhibited intense photoluminescence also indicating negligible contamination at the interface due to the 15 min spent in the reactor chamber between layers.

Wafer B was transferred to the load-lock after the SiGe growth. A purge cycle, consisting of pressurizing the load-lock to 1-10 Torr with dry nitrogen followed by evacuation with a rotary vane pump, was repeated six times to simulate the load-lock transfer without exposure to atmosphere. SIMS of the buried interface detected barely observable C and O peaks (Fig. 5 at depth of 0.13 μm) with integrated densities in both cases 10^{12} cm⁻². To simulate the entire loading process from removal of the substrate from the *ex situ* dilute HF dip to loading and purging of the load-lock, two more cases were examined: (wafer C) a strained SiGe layer was transferred to the load-lock, given a nitrogen purge cycle, left in the load-lock for 5 min with the door of the load-lock left slightly open to the laboratory atmosphere, and then sent through a second purge before being returned to the growth chambers. After SiGe growth, wafer D was taken out of the load-lock and moved to a chemical hood for 10 min, after which the wafer was returned to the reactor through the standard loading and purge cycles without any HF dip or wet processing.

SIMS of wafer B to (nitrogen only atmosphere in the load-lock) and of wafer C (door of load-lock slightly opened) showed only a small increase in contamination (Fig. 5, 6). However when the wafer was removed from the load-lock and exposed to atmospheric conditions of the laboratory (wafer D), the carbon and especially the oxygen contamination increased significantly (Fig. 6). Finally, to compare the susceptibility of SiGe surfaces to Si surfaces for contamination, in one case (wafer E) a virgin Si wafer was left in the fume hood for 10 min after a 100:1 DI:HF dip before loading and the growth of a silicon cap at 700°C. Oxygen and carbon concentrations for this wafer are five to ten times less than those of wafer D (Fig. 6), in which a presumably clean and H-terminated SiGe surface from the reactor was exposed similarly to air for 10 min.

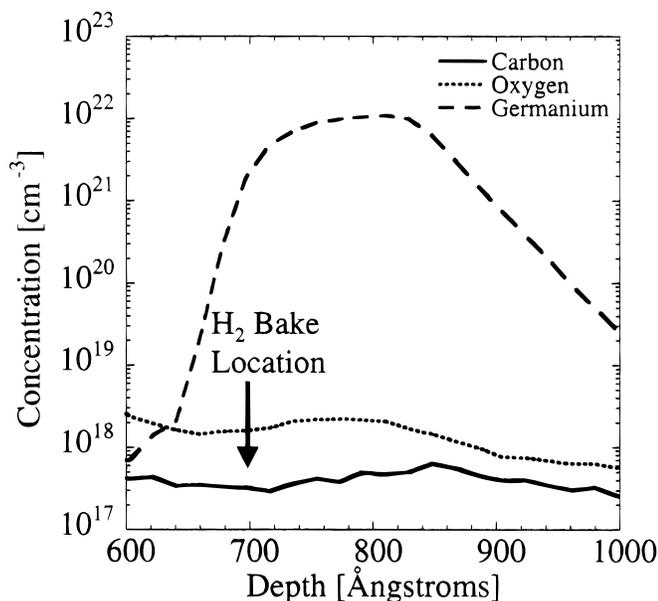


Figure 4. Oxygen, carbon, and germanium SIMS profiles of a sample in which a commensurately strained Si_{0.8}Ge_{0.2} surface prepared *in situ* by rapid thermal chemical vapor deposition, then allowed to cool for 15 min with 3 slpm of hydrogen flowing at 6 Torr before burying the test surface with silicon epitaxy using dichlorosilane at 700°C (wafer A). The hydrogen bake was done at the silicon depth of ~700 Å.

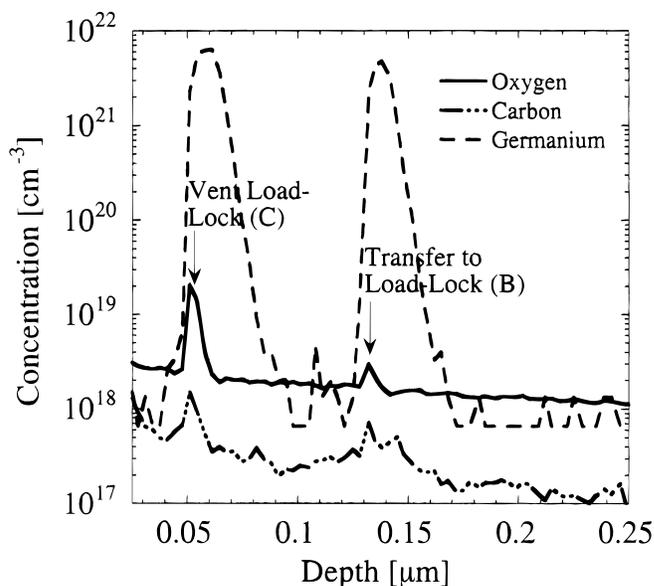


Figure 5. Oxygen, carbon, and germanium profiles at SiGe/Si interfaces when the sample was transferred to the load lock (B) without venting to air, and (C) with venting to air before silicon cap regrowth at 700°C.

Discussion.—Several conclusions can be drawn from this series of experiments. First, the reactor itself is a relatively clean environment for short times for cold hydrogen passivated surfaces. Most significantly, the load-lock itself introduces only minimal contamination. Most contamination is caused by the exposure of the wafer surface to the laboratory environment. Finally, the hydrogen-terminated surface of the *in situ* prepared SiGe surface is much more susceptible to oxygen and carbon absorption than a hydrogen-terminated Si surface. The difference in reactivity of the *in situ* prepared SiGe surface

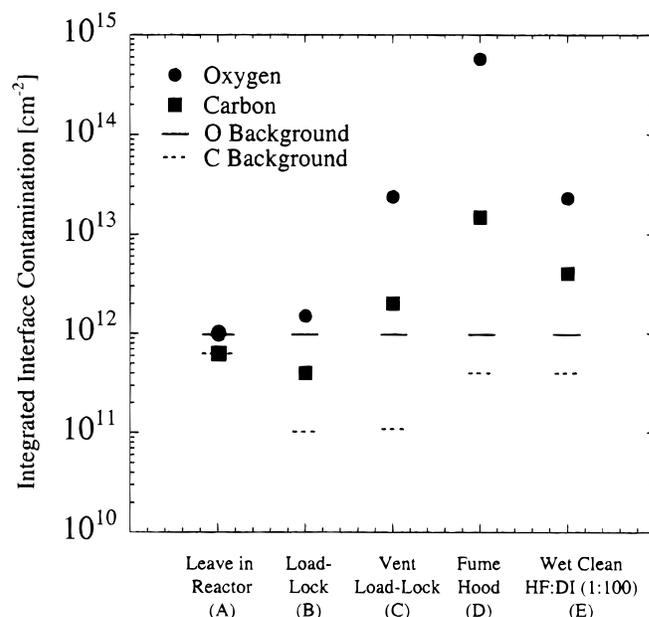


Figure 6. Integrated oxygen and carbon levels observed at SiGe/Si interfaces by SIMS for wafers A-D subjected to different conditions after SiGe growth before Si cap growth at 700°C without high-temperature cleaning. In case E, the test surface is not prepared *in situ* as in cases A-D, a silicon substrate surface after 1:100 HF:DI dip is transferred to the load-lock (total time in the fume-hood *ca.* 10-15 min) before silicon growth at 700°C. Note: solid and dashed lines indicates SIMS detection limits for oxygen and carbon, respectively (SIMS background multiplied by typical contamination peak widths).

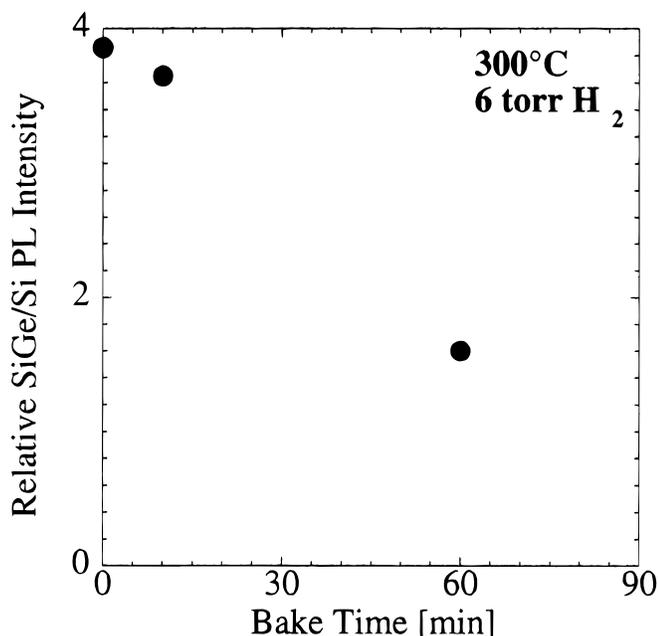


Figure 7. Relative SiGe/Si photoluminescence intensities from SiGe/Si layers grown directly on silicon (100) substrates prepared using 1:1000 HF(49%):DI and then baked in 6 Torr of H₂ at 300°C for different times before SiGe growth.

compared to the surface prepared in a 1:100 dilute HF dip may be due to differences in the stability of the hydride termination of the two cases, which can result from different reconstructions of the surface,²³ or because the H–Ge bond is weaker than the H–Si bond.²⁴

In Situ Wafer Cleaning

200-400°C prebakes.—The purpose of a very low-temperature (e.g., 200-400°C) bake is to desorb physisorbed chemical contamination from the surface before the chemical contamination can dissociate and chemisorb to the wafer surface, which occurs first at higher temperatures.²⁵ Any chemisorbed carbon that is consequently annealed at high temperature can form stable SiC precipitates on the surface²⁶ or diffuse into the bulk,²⁶ leading to undesirable defect formation.

To test the effectiveness of low-temperature prebakes on the interface quality, (100) wafers were subjected to the standard wet clean and loading procedure, followed by a low-temperature prebake before epitaxy. No high-temperature bake was used. The wafers were baked at ~300°C at 6 Torr under a hydrogen flow of 3 lpm. A 200 Å Si_{0.8}Ge_{0.2} layer was grown at 625°C immediately after the hydrogen bake, followed by a 450 Å silicon capping layer to reduce surface recombination effects on photoluminescence intensity.²⁷ The time dependence of the interface quality on the hydrogen prebake was examined using PL intensity (Fig. 7). Because the PL intensity decreased with extended low temperature prebaking it was concluded

that the surface quality is degraded, not enhanced by a low-temperature prebake in our system.

700-800°C bakes in hydrogen.—The complete removal of oxygen and carbon from silicon surfaces before epitaxy by baking in hydrogen atmospheres at higher temperatures (750-850°C) has been previously reported for UHV-CVD.^{4,28} Their success has been attributed to low oxygen and water-vapor partial pressures, below the critical levels required for clean silicon surfaces in a vacuum at a given temperature.^{29,30} References 4 and 28 stressed the importance of both the UHV system and the hydrocarbon-free “dry” load-lock system. Later, Wolansky *et al.* demonstrated that oxygen and carbon removal could be obtained at higher hydrogen pressures for nearly equivalent thermal budgets,¹ showing that UHV is not a necessary condition for the cleaning of the silicon surface in hydrogen at or under 800°C, and that the cleaning temperature could be reduced to as low as 760°C. However, some carbon contamination was seen at the cleaned interface by SIMS in that report. In our work, hydrogen bakes were examined for different pressures and temperatures ranging from 0.5 to 250 Torr and 700 to 800°C.

700°C bakes in hydrogen.—The growth of silicon epitaxial layers at 700°C was interrupted, after which the substrates were then allowed to cool to less than 200°C in 3 slpm hydrogen at 6 Torr in the reactor. In the Experimental part of the preceding section we showed this introduced no contamination to a SiGe surface. A silicon surface would presumably also remain clean due to the higher stability of hydrogen on its surface. After cooling, for approximately 15 min, the reactor pressure was set between 0.25 and 250 Torr, with a hydrogen flow of 3-4 lpm, immediately followed by reheating the wafer to 700°C. The temperature, flow, and pressure were maintained constant for between 2 and 15 min, with the exception of the hydrogen bake at 0.25 Torr in which the hydrogen pressure was held constant by turning off the hydrogen flow and sealing the chamber. After the hydrogen bake the pressure was then brought to 6 Torr with a flow of 3 slpm of hydrogen. Dichlorosilane was then added to the hydrogen stream to grow epitaxial silicon and bury the test interface. The oxygen and carbon adsorption rates during the bake were determined by dividing the integrated carbon and oxygen concentrations found at the interface (determined by SIMS), by their respective annealing times. At lower pressure, for example, 0.6 Torr, the adsorption rates for oxygen and carbon were 1.6×10^{14} and $1.4 \times 10^{12} \text{ cm}^{-2} \text{ min}^{-1}$, respectively (Table I). However, for pressures of 6 and 250 Torr of hydrogen both oxygen and carbon concentrations were below SIMS detection limits. For the 6 Torr case the adsorption rates were less than 7×10^{10} and $7 \times 10^9 \text{ cm}^{-2} \text{ min}^{-1}$, and for 250 Torr the detection limits were anomalistically high leading to a higher maximum bound on the adsorption rates, which were 5×10^{12} and $5 \times 10^{11} \text{ cm}^{-2} \text{ min}^{-1}$ for oxygen and carbon, respectively.

While the bakes at pressures at or over 6 Torr did not contaminate the surface, in our laboratory they have also not been effective at removing previously existing contamination, presumably because the temperature is too low for rapid enough desorption. A previously prepared SiGe surface exposed to atmosphere for over 3 days was prepared by wet cleaning, using the optimal 1:1000 HF(49%):DI

Table I. Integrated oxygen and carbon interface levels measured by SIMS and inferred adsorption rates for Si surfaces baked in hydrogen at pressures from 0.25 to 250 Torr for various times. All hydrogen pressures were maintained with a steady flow rate of 3-4 lpm of hydrogen and baked at 700°C except for 0.25 Torr, which was baked with no hydrogen flowing.

Pressure (Torr)	Time (min)	Oxygen (cm ⁻²)	Carbon (cm ⁻²)	Oxygen adsorption rate (cm ⁻² min ⁻¹)	Carbon adsorption rate (cm ⁻² min ⁻¹)
0.25	2	8.7×10^{14}	2.8×10^{12}	4.4×10^{14}	1.4×10^{12}
0.6	15	1.6×10^{15}	4.9×10^{12}	1.0×10^{14}	3.2×10^{11}
6	15	$\leq 1 \times 10^{12}$ a	$\leq 1 \times 10^{11}$ a	$\leq 7 \times 10^{10}$ a	$\leq 7 \times 10^9$ a
250	2	$\leq 1 \times 10^{13}$ a	$\leq 1 \times 10^{12}$ a	$\leq 5 \times 10^{12}$ a	$\leq 5 \times 10^{11}$ a

^a Indicates no O or C detected within the resolution of SIMS and the given rate is calculated from the limit of SIMS background for the sample.

ratio. The wafers were loaded into the RTCVD for the growth of a silicon cap at 700°C. The quality of the SiGe layer and its interfaces were probed by PL. Performing a 10 min bake at 700°C at 6 Torr in 3 lpm H₂ before the Si epitaxy showed no improvement in the SiGe/Si PL intensity compared to that of a wafer grown without such a step. Also, there was no observed PL dependence on when the dichlorosilane was introduced (*i.e.*, either before or after the wafer was heated to 700°C). Further work is needed to evaluate longer 700°C hydrogen bake times and pressures for any potential cleaning benefits.

800°C bake in hydrogen.—Since 700°C bakes were not effective, 800°C hydrogen bakes were tested to remove oxygen and carbon from the silicon surface after wet cleaning. Silicon surfaces were cleaned *ex situ* before introduction to the reactor, as described previously using the optimal 1000:1 DI/HF final dip (see the section on *Ex situ* Wet Cleaning). After loading, the hydrogen flow is set to 3-4 lpm and the hydrogen pressure in the reactor is brought to between 0.5 and 250 Torr. The wafer was then heated and held at 800°C for 1 min, after which the temperature was reduced to 625°C while stabilizing the pressure to 6 Torr (at 3 lpm H₂). After both pressure and temperature were stable (requiring ~1 min for all pressures except 250 Torr which required ~5 min), differential scanning calorimetry (DCS) followed shortly after by germane were injected into the reactor to grow a Si_{0.8}Ge_{0.2} (20 nm) layer, followed by a Si capping layer at 700°C. PL results, and integrated oxygen and carbon concentrations (by SIMS) at the lower Si/SiGe interface for different pressures and for different times at 800°C are shown in Fig. 8, 9, and 10, respectively.

If the hydrogen bake is omitted (wafer E, Fig. 6), the integrated O and C levels are 2.3×10^{13} and 4×10^{12} cm⁻². Performing a hydrogen bake for 1 min at 0.5 Torr slightly reduces the integrated oxygen level to 6.4×10^{12} cm⁻² and increased the carbon level to 6.6×10^{13} cm⁻². The 1 min 250 Torr bake dramatically increases the oxygen level to 9×10^{13} cm⁻² and drops the carbon level to 2×10^{12} cm⁻². The 1 and 10 Torr bakes both reduced the oxygen to ~10¹² cm⁻², and the carbon levels were little changed from the no-bake levels (~10¹³ cm⁻²). The SiGe/Si relative PL intensity dropped 10-100 times for 0.5 or 250 Torr cleans, corresponding to

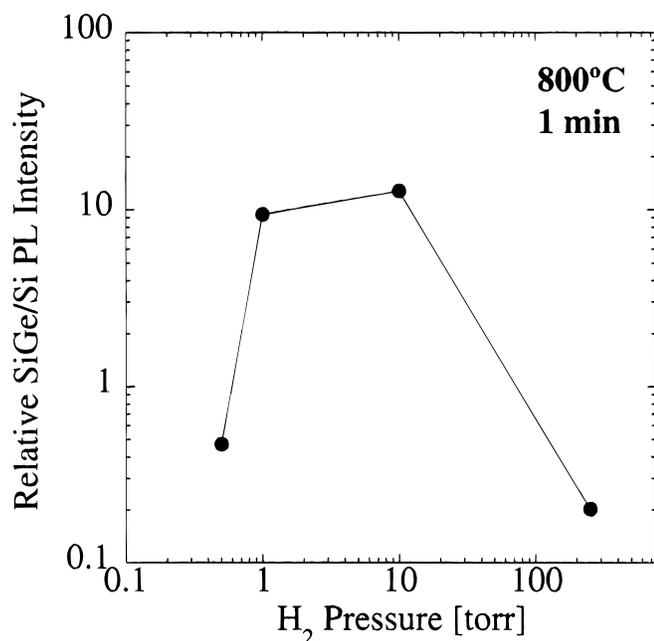


Figure 8. Relative SiGe/Si photoluminescence intensities from SiGe/Si layers (20 nm/45 nm) grown on silicon (100) substrates prepared using 1:1000 HF(49%):DI and then baked for 1 min at 800°C at different hydrogen pressures.

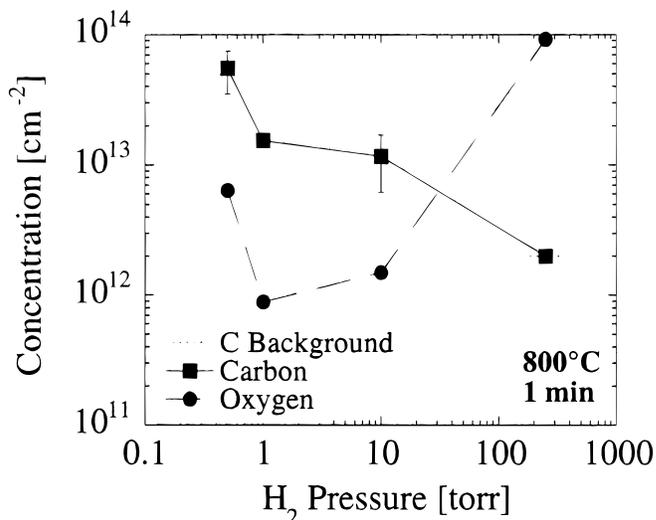


Figure 9. Integrated carbon and oxygen levels at SiGe/Si interfaces formed by growing SiGe on silicon (100) substrates prepared using HF dip and then baked for 1 min at 800°C at different hydrogen pressures.

the 10-100 times increase in oxygen or carbon levels, therefore, the SiGe/Si PL ratio was consistent with SIMS in showing that the 1-10 Torr cleans, which also had the lowest oxygen and carbon contamination, had the highest SiGe/Si PL ratios. The 1-10 Torr bakes increased the SiGe/Si PL ratios from one to four without a bake to nine to twelve; this is in comparison to a ratio of 10-20, which is commonly observed for Si/SiGe/Si structures grown under our best conditions (grown without interruption, to minimize contamination, after a 1000°C hydrogen clean and silicon 1000° buffer layer on the substrates).

A longer hydrogen bake of 2 min at 800°C and 10 Torr resulted in no detectable oxygen or carbon contamination above the SIMS background (Fig. 10), although the SIMS oxygen background was considerably higher in this case. The interrupted and uninterrupted growth were, therefore, indistinguishable with respect to PL and

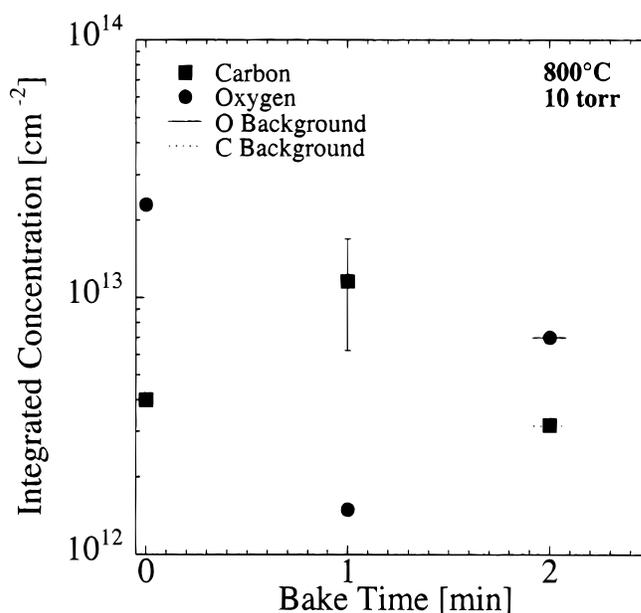


Figure 10. Integrated carbon and oxygen levels at Si/SiGe interfaces formed by SiGe growth on silicon (100) substrates prepared using an HF dip to remove the wet chemical oxide and baked at 800°C in 10 Torr hydrogen for various times. For a 2 min bake, the oxygen level was below that resolvable by SIMS.

SIMS measurements. This cleaning technique (800°C, 2 min, 10 Torr H₂) was also used in a Si/Si interface after *ex situ* wet cleaning, followed by 700°C Si growth where a phosphorus layer marked the location of the interrupted interface. Again, absolutely no carbon or oxygen was detected by SIMS at this interface, even with the integrated concentration detection limit due to SIMS background as low as 10¹² cm⁻² for oxygen and 4 × 10¹¹ cm⁻² for carbon (Fig. 11).

Discussion.—The net oxygen or carbon adsorption or desorption to or from the silicon surface at different temperatures and hydrogen pressures depends on the flux to the surface, the sticking fraction of the flux that sticks to the surface, and the desorption rate. Hydrogen passivation of the surface, which increases at increasing hydrogen pressure, can greatly reduce the sticking coefficient of oxygen.³¹ However, a simple hydrogen passivation model fails to explain why during an 800°C bake, the adsorbed oxygen increased as the hydrogen pressure was increased from 6 to 250 Torr (Fig. 9). The increase in oxygen contamination at higher hydrogen pressure could be the result of oxygen or water vapor impurities in the hydrogen gas. The two sources of oxygen/water contamination are then the background in the reactor and the carrier gas itself. Because the hydrogen entering the reactor is purified to a level 10 ppb, the hydrogen gas can only become the dominant source of oxygen at high hydrogen pressures.

Figure 12 schematically shows the two contributions to oxygen adsorption of hydrogen surface coverage and oxygen partial pressure, and their dependence on hydrogen pressure. The authors stress that this description is only a qualitative description, as details of the hydrogen surface coverage, and total oxygen background, are not exactly known. As the hydrogen pressure increases, the hydrogen coverage of the surface increases, which greatly reduces the number of open sites for O adsorption and thus the sticking coefficient.³¹ This explains the relatively high contamination levels resulting from bakes at pressures below 6 Torr at both 700 and 800°C. When the hydrogen pressure is too high, however, then the oxygen partial pressure, due to impurities in the hydrogen, may become so great that it produces an oxygen flux that cannot be compensated for by the additional hydrogen coverage. At 700°C the hydrogen coverage at high pressure is still sufficient to keep the increased oxygen contamination in the gas below detection limits (SIMS detection limits were

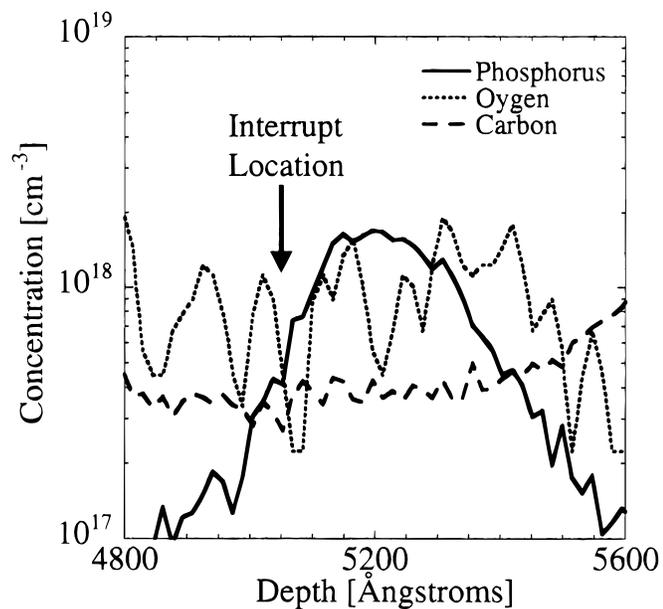


Figure 11. Oxygen, carbon, and phosphorus SIMS profiles of a sample in which the phosphorus-doped silicon marks the interrupt location, where the silicon surface is cleaned using the experimentally determined optimal *ex situ* and *in situ* conditions [*i.e.*, using a 1:1000 HF(49%):DI to strip the final chemical oxide followed by an 800°C, 10 Torr hydrogen bake for 2 min]. The silicon-cleaned interface is located at a depth of approximately 5050 Å.

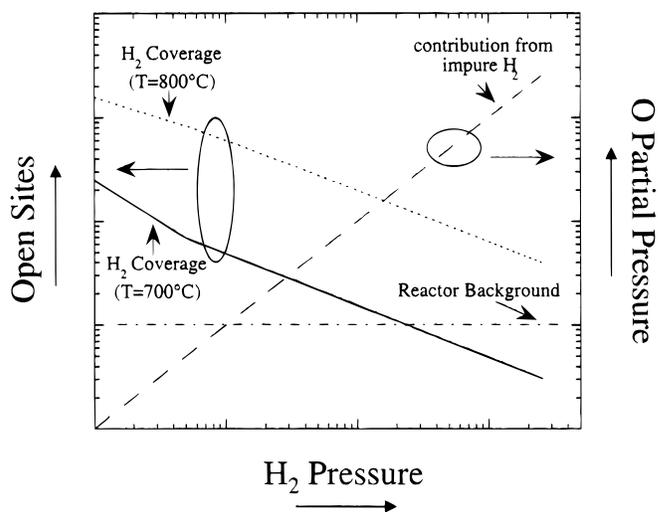


Figure 12. Schematic diagram of important mechanisms that determine the amount of oxygen sticking to the silicon surface during hydrogen baking. The decreasing fraction of open sites that are available for oxygen to stick (corresponding to increased hydrogen coverage) with increasing hydrogen pressure at 700 and 800°C are referenced to the left axis. Oxygen partial pressures due to the oxygen background in the reactor and from impurities in the hydrogen gas are referenced to the right axis.

high in this case, Table I). However, because silicon epitaxy in this reactor at higher hydrogen pressure (220 Torr, 700°C) has shown indications of unusually high oxygen concentrations⁹ and the oxygen SIMS detection limits were high (because of interference with surface contamination), it is still likely that the surface may be adsorbing oxygen at higher hydrogen pressures at 700°C. At 800°C the higher open site density *vs.* that at 700°C allowed the increased gas contamination level to cause significant surface contamination, so that high pressure bakes contaminated the surface (Fig. 9).

At 800°C, the cleanest surface was achieved between those two extremes, in the 1-10 Torr range. The inability to further clean surfaces at 700°C, while still maintaining low contamination at high pressures (oxygen and carbon below SIMS detection limits), can be attributed to an oxygen desorption rate near the rate of oxygen adsorption. If the accumulative rate is indeed desorptive at this temperature it is still too slow to make an observable effect for the bake times considered in this study.

The surface concentration of carbon is also observed to have a dependence on hydrogen pressure. At the lowest hydrogen pressure of 0.5 Torr, the detected carbon signal rose significantly, 6.6×10^{13} cm⁻², but at higher hydrogen pressures, 250 Torr, the carbon signal dropped to below the SIMS detection limits, 2×10^{12} cm⁻² after 1 min at 800°C (Fig. 9). The source of carbon depositing on the surface during baking at low hydrogen pressure, 0.5 Torr, is likely from reactor background contamination. Presumably increasing the hydrogen coverage of the surface, by increasing the hydrogen pressure, will reduce the overall adsorption of carbon from the chamber atmosphere. Indeed, less carbon is observed for higher hydrogen pressure bakes, however, it is also observed that carbon was removed from the silicon surface for high hydrogen pressures, 10 and 250 Torr, at 800°C. Two proposed mechanisms of carbon removal from the silicon surface during hydrogen baking at temperatures around 800°C are either desorption of carbon as hydrocarbons or methylsilanes,^{4,28} or diffusion of carbon from the surface into the silicon bulk.²⁶ However, further analysis of these two possible mechanisms goes beyond the scope of this work due to limits of SIMS resolution (*i.e.*, SIMS broadening and detection limits) and an incomplete knowledge of how much carbon is desorbed into the hydrogen atmosphere.

Conclusions

We have examined the effects of *ex situ* wet chemical cleaning and of hydrogen bakes on the ability to prepare clean silicon or sili-

con-germanium alloy surfaces for subsequent epitaxy by RTCVD. Ultrahigh-vacuum or dry-pumping techniques were not used either in the load lock or the growth reactor itself. Critical factors are the pH of the final HF treatment and the temperature and pressure of the hydrogen bake. 700°C bakes do not add contamination at sufficiently high hydrogen pressure, but are also ineffective at removing existing oxygen and carbon contamination. 800°C bakes between 1 and 10 Torr can effectively remove contamination and give interfaces which are indistinguishable by SIMS or photoluminescence from those grown without interruption.

The pressure dependence of the interface cleaning at 700 and 800°C may be understood by considering the effect of the hydrogen pressure on the reactivity of the surface. Because negligible dopant diffusion occurs for short times at 800°C, this demonstrated ability to grow pristine interfaces without exceeding 800°C after removing the wafer from the reactor will enable new strategies for device integration and fabrication.

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