High electron mobility polycrystalline silicon thin-film transistors on steel foil substrates

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Thin-film transistors have been fabricated in polycrystalline silicon films on steel foil. The polycrystalline silicon films were formed by the crystallization of hydrogenated amorphous silicon, which had been deposited on 200-μm-thick foils of stainless steel coated with $\sim$0.5-μm-thick layers of SiO_2. We employed crystallization temperatures (and duration) of 600 °C (6 h), 650 °C (1 h), and 700 °C (10 min). Top-gate transistors made from films crystallized at 650 °C have an average electron field-effect mobility of 64 $cm^2/V\,s$, with equal values in the linear and saturated regimes. Thus steel substrates permit a substantial reduction in crystallization time over glass substrates, and afford polysilicon with high electron mobility. © *1999 American Institute of Physics.* [S0003-6951(99)03041-7]

Considerable effort is expended at present to develop processes for making thin-film transistors (TFTs) of polycrystalline silicon (polysilicon) on glass substrates.[1] Owing to their high carrier mobilities compared to those in amorphous silicon, *n* and *p* type channel polysilicon TFTs conduct large currents when on, which qualifies them for use in driver circuits.[2] The capability of polysilicon to form *n* and *p* channel devices enables complementary metal–oxide–semiconductor (CMOS) circuits, which are the technology of choice when low power consumption is desired. Polysilicon films for TFTs are made by crystallizing amorphous silicon at elevated temperature. Because the strain points of affordable glass substrates lie just above 600 °C,[3] crystallization techniques are restricted to either furnace annealing up to 600 °C,[4] or rapid thermal processing by lamp heating,[5] or laser annealing.[6] Furnace annealing is preferred, as it is isothermal and thus produces uniform transport properties over the entire glass plate, which now may be as large as 0.5 m^2. However, conventional furnace crystallization at 600 °C takes close to one day. Catalyzed[7] and preanneal nucleation[8,9] approaches can cut this time to $\sim$5 h, which still is long when compared to the throughput of one plate per minute desired of the single-substrate cluster tools employed in the manufacture of active-matrix liquid-crystal displays.[1]

These results point to the need for isothermal annealing that can be conducted quickly on low-cost substrates. This can be done with silicon films on substrates of quartz glass,[4] but quartz glass substrates are expensive. Reducing the annealing time was our principal motive for experimenting with steel substrates, which can be heated to well above 600 °C. Previous work with steel foil substrate was limited to amorphous silicon TFTs (electron mobility $\sim$1 $cm^2/V\,s$) at temperature $\leqslant$350 °C,[10,11] and very recently, to laser crystallized films.[12] In the present study, we found that the crystallization of films of hydrogenated amorphous silicon (*a*-Si:H) by furnace annealing at temperatures up to 700 °C can be conducted in short times, and does produce polysilicon TFTs with high field-effect electron mobility.

200-μm-thick foils of American Iron and Steel Institute (AISI) grade 304 stainless steel (Fe/Ni/Cr 72/18/10 wt. %) were passivated on both faces by coating with a 210-nm-thick film of spin-on glass and a 270-nm-thick film of SiO_2 deposited by plasma-enhanced chemical vapor deposition (PECVD). Next, a 160-nm-thick precursor film of hydrogenated amorphous silicon (*a*-Si:H) was deposited at a substrate temperature of 150 °C, and then was exposed for 1 h to a hydrogen discharge to induce nucleation.[8,9] These films then were crystallized by furnace annealing at 600 °C for 6 h, or 650 °C for 1 h, or 700 °C for 10 min. The progress and completion of crystallization was monitored by measuring the ultraviolet reflectance at $\lambda = 276$ nm,[4,5] with the above times being the minimum required for crystallization of the films as monitored by ultraviolet reflectance.[13] The electrical conductivity at room temperature of all polysilicon films was 10^{-6}–$10^{-5}\ S\,cm^{-1}$, with a thermal activation energy of 0.53 eV. The performance of test transistors of *a*-Si:H made at 250–300 °C on the oxide-coated steel substrates without any recrystallization, and the conductivities of the polysilicon films, all suggested that the silicon films are not contaminated by metal from the steel substrate. Therefore, we proceeded to make TFTs of the polycrystalline layers.

Figure 1 shows a schematic cross section of a top-gate polysilicon TFT made on steel. Because we wanted our TFTs to measure the quality of the polysilicon films after the recrystallization process, all post-crystallization processing was done at low temperature. Therefore a conventional ion implantation source/drain process, which generally requires annealing at temperature >600 °C, was not used. TFTs were fabricated with a nonself-aligned top-gate process with a maximum process temperature of 350 °C. First, 75-nm-thick n^+ microcrystalline silicon (μc-Si) was deposited at 350 °C on the polysilicon channel layer to serve as the eventual source/drain. This layer was patterned by reactive ion etching (RIE), and the original polysilicon was patterned into

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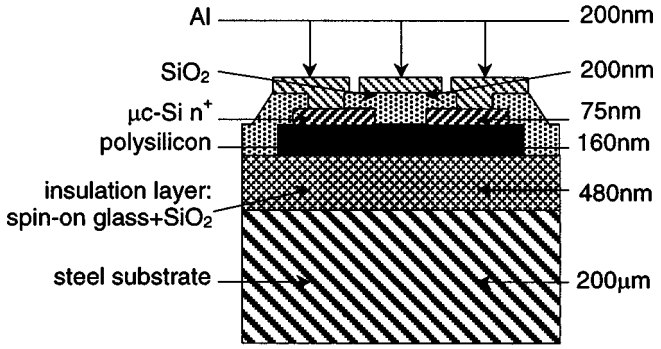

FIG. 1. Schematic cross section of a polysilicon top-gate transistors on a passivated steel substrate, showing materials used and their thickness.

islands by another RIE step. The 200-nm-thick gate oxide was then deposited by PECVD at 250 °C, followed by contact etching. 200 nm of aluminum was thermally evaporated and then patterned to form the gate and source/drain contacts. The final step in TFT fabrication was a 15-min long anneal at 250 °C in a hydrogen/nitrogen mixture. This process is not practical for short-channel TFTs with low parasitic resistance, but is sufficient to evaluate the mobility in long channels, so that the large parasitic source/drain resistance in our structure does not significantly affect the current and the extracted mobility. Channels were 45 μm long and 180 μm wide. The source/drain contact windows were opened with a wet etch.

Figure 2 shows the (a) transfer and (b) output characteristics of the transistors made with the 650 °C polysilicon, which have the highest current levels among the three groups, and transfer and output characteristics of transistors made with the 600 °C [(c),(d)] and 700 °C [(e),(f)] polysilicon. All measurements were made with the metal foil grounded. Transistors for all three annealing conditions had well-behaved characteristics. Table I lists the principal characteristics of all three groups of transistors. The threshold voltage and electron field effect mobility in the linear regime were extracted from the linear plot of I_{ds} vs V_{gs} with $V_{ds} = 0.1$ V, and the electron field-effect mobility in the saturated regime was obtained from a plot of $I_{ds}^{1/2}$ vs V_{gs} at $V_{ds} = V_{gs}$. The highest average mobility of 64 cm^2/V s observed both in the linear and saturated regimes, occurred for crystallization at 650 °C. Some devices had mobility as high as 85 cm^2/V s. This lies at the top of the range for furnace-annealed material.[1] Typical threshold voltages and subthreshold slope (with 10 V V_{ds}) are 7.2 V and 0.4 V/decade respectively. Note most significantly that the minimum off currents with $V_{ds} = 10$ V are in the 10^{-9} A range, independent of the annealing temperature. This is very important because it suggests that the polycrystalline films and carrier generation lifetimes are not adversely affected by metal con-

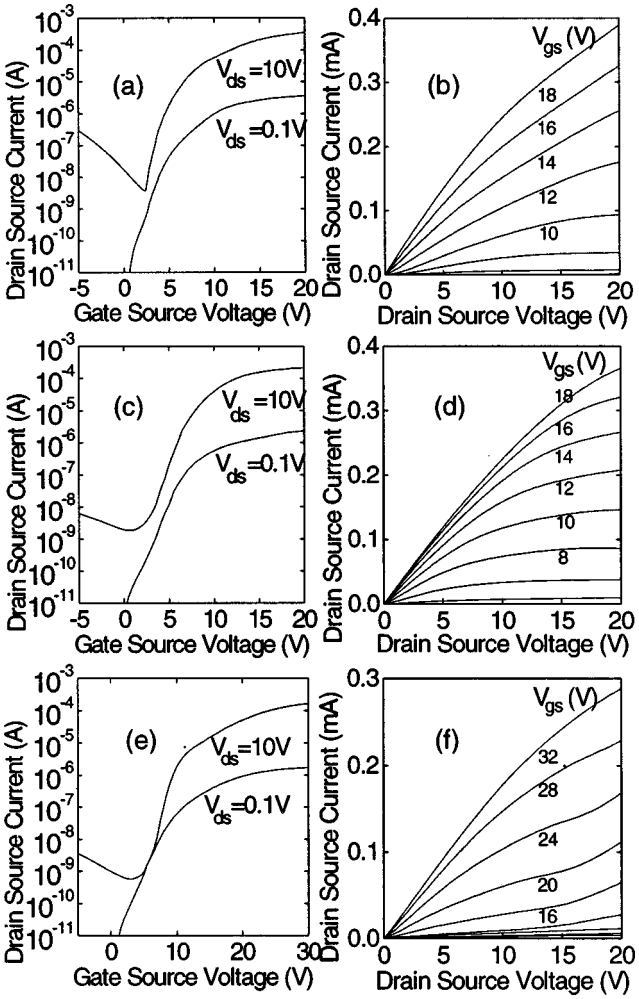

FIG. 2. (a) Transfer characteristics and (b) output characteristics of a top-gate TFT made by crystallization at 650 °C of silicon on steel, V_{ds} and V_{gs} are the drain source and gate source voltages. (c), (d) and (e), (f) are transfer and output characteristics of top-gate TFTs made by crystallization at 600 and 700 °C of silicon on steel. All TFTs have a dimension of $W/L = 180\ \mu$m/45 μm.

TABLE I. Electrical characteristics of the polycrystalline silicon thin-film transistors made on steel substrates. All electrical measurements are an average from ⩾10 devices.

Temp. of crystallization (°C)	Time of crystallization (min)	Polysilicon conductivity σ[a] (S/cm)	UV reflectance ΔR[b] (%)	ON current I_{ON}[c] (A)	OFF current I_{OFF}[d] (nA)	I_{ON}/I_{OFF}	Threshold voltage[e] (V)	Subthreshold slope[f] (V/decade)	Electron mobility (linear) (cm^2/V s)	Electron mobility (saturated) (cm^2/V s)
600	360	1.1×10^{-5}	6.7	$1.8\times10^{-4}\pm0.6$	2.5 ± 1	$\sim10^5$	7.0 ± 1.3	0.9 ± 0.4	31 ± 10	55 ± 11
650	60	2.0×10^{-6}	6.2	$3.8\times10^{-4}\pm0.2$	2.1 ± 1.7	$\sim10^5$	7.2 ± 1.8	0.4 ± 0.3	63 ± 11	64 ± 11
700	10	0.8×10^{-6}	5.5	$5.9\times10^{-5}\pm0.9$	0.59 ± 0.5	$\sim10^5$	8.0 ± 3.7	1.8 ± 0.7	13 ± 3.5	20 ± 4

[a]300 °C.
[b]UV reflectance difference from *a*-Si:H at 276 nm, for silicon wafer $\Delta R = 7.5\%$.
[c]$V_{gs} = 20$ V, $V_{ds} = 10$ V.
[d]$V_{ds} = 10$ V.
[e]$V_{ds} = 0.1$ V.
[f]$V_{ds} = 10$ V.

tamination from the substrate. For all three annealing temperatures, the threshold voltage were in the range of 7–10 V. The mobilities and subthreshold slope were poorer in the films annealed at 600 °C and especially 700 °C than those annealed at 650 °C (Table I). For example, the mobility for the 700 °C film was $\sim$13–20 $cm^2/V\,s$. One possible reason is incomplete crystallization. Note that differential thermal expansion between the SiO_2 passivation layer and the TFT materials, with coefficients of thermal expansion α of $\sim 4\times10^{-6}$ and $\alpha=18\times10^{-6}$ for SiO_2 and steel, respectively, does not seem to pose a systematic problem.

Our required annealing times are consistent with an activation energy of 2.7 eV to fully crystallize the *a*-Si:H precursor films.[11] Temperatures of $\sim$750 °C are expected to further reduce annealing times to $\sim$1 min. A very attractive feature of steel foil substrates is their ruggedness and flexibility.[11,14] Therefore, this work also suggests that conventional furnace processing can furnish rugged TFT backplanes with high-performance.

In summary, thin-film transistor of polycrystalline silicon can be made on steel, which allows process temperatures above 600 °C. The steel foil makes possible a great reduction in furnace annealing time compared to that on glass substrates by allowing higher temperature. Transistors made from 650 °C material have electron field-effect mobilities that are comparable to the highest values reported to date for furnace-crystallized polysilicon on glass substrates, and leakage currents are not adversely affected by contamination from the steel substrate.

Note added in proof: We recently learned that an article on ''Polysilicon Thin Film Transistors on Steel Substrates,'' by A. S. Howell, M. Stewart, S. V. Karnik, S. K. Saha, and M. K. Hatalis will be published in IEEE Electron Device Letters.

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