Substrate Bias Dependence of Subthreshold Slopes in Fully Depleted Silicon-on-Insulator MOSFET's

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***Abstract*—Subthreshold slopes in submicrometer n-channel MOSFET's in depleted silicon-on-insulator (SOI) films have been measured as a function of substrate bias and temperature, as well as drain bias. It is found that for low drain voltages, a simple capacitor model can explain the results. For large drain voltages, anomalously sharp subthreshold slopes are observed for very negative substrate biases, but the anomalous effects are greatly reduced with a more positive substrate bias. A qualitative model based on the charge state of the lower SOI interface is proposed to explain the dependence of the anomalous effects on substrate bias.**

I. Introduction

The dependence of drain current with gate voltage below threshold is an important characteristic of FET's for future scaling. As power supply voltages, and hence threshold voltages, are scaled down, a sharp subthreshold slope is required to reduce leakage currents and minimize required logic swings. In this paper, the dependence of subthreshold slope on substrate bias in submicrometer n-channel MOSFET's fabricated in silicon-on-insulator (SOI) films is reported. While the "bulk" of the SOI films themselves is depleted, the film interfaces may not be. The charge state of the lower SOI interface will be shown to play a critical role in determining the subthreshold slope, both in the "classical" case with small drain voltages and in the "anomalous" case with large drain voltages. In both cases, a depleted lower interface yields the optimum results.

II. Experiment

Silicon-on-insulator films were formed by the oxygen implantation and annealing (SIMOX) process, with an implant of 1.7×10^{18} cm^{-2} at 150 keV followed by annealing in nitrogen (1% oxygen) at 1200°C for 6 h. The underlying oxide thickness was 3500 Å and the SOI thickness after annealing was 1200 Å. Conventional FET fabrication was then performed using local oxidation for device isolation. Based on process simulation, a flat boron doping of $\sim 1.0 \times 10^{17}$ cm^{-3} is expected in the SOI films of the n-channel transistors. The final SOI film thickness after fabrication was 1000 Å.

Based on the SOI thickness and targeted doping, one would expect full depletion of the SOI film body when the transistor is "on," independent of substrate bias [1]. Shown in Fig. 1 is the measured threshold voltage for conduction along the top SOI–oxide interface in a long-channel (8-μm) device. Three distinct regions are seen which can be related to the charge condition of the lower SOI–oxide interface according to the model of Lim and Fossum [1]. (Top versus bottom channel conduction were separated by their gate voltage dependences.) Substrate voltages less than -10 V lead to accumulation at the lower SOI–oxide interface even though the film body itself is depleted. (All voltages in this work are measured with respect to the source node which was grounded.) Accumulation pins the potential at the lower SOI–oxide interface, leading to no dependence of the threshold voltage on substrate bias. For a substrate bias greater than -10 V, the lower interface (in addition to the film body) is depleted. In this case electric field lines from the top channel (upper SOI–oxide interface) are terminated in the substrate, and a dependence of the threshold voltage on substrate bias is observed. For a substrate bias greater than $+5$ V, the back interface is inverted, again pinning the lower interface potential and thus the top-channel threshold voltage. These three regions will be referred to later when interpreting subthreshold slope data.

Subthreshold characteristics were measured for n-channel devices with $L_{\text{eff}} = 0.4$ μm as a function of substrate voltage for various drain voltages at temperatures of 86.5, 300, and 370 K. No evidence of any sidewall conduction or subthreshold kinks were observed, nor was latching observed above threshold. Leakage currents at room temperature were ~ 1 pA/μm for a drain bias of 0.1 V and ~ 10 pA/μm for a drain bias of 3 V, and in both cases they were insensitive to substrate bias. The room-temperature suthreshold slope data are presented in Fig. 2 in terms of the normalized inverse subthreshold slope "n," where $n \cdot 2.30 \cdot kT/q$ of gate bias swing is required to change the subthreshold current by a factor of 10. One can discern two general trends. First, a small drain bias (≤ 1 V) yields a U-shaped curve, whereas large drain biases lead to a monotonic dependence of subthresh-

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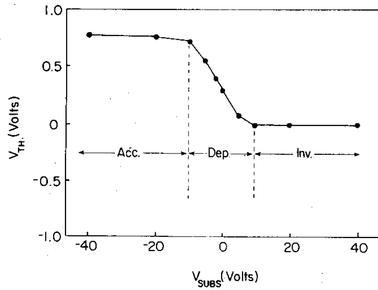

Fig. 1. Top-channel threshold voltage as a function of substrate–source bias. The channel length was 8 μm, and the drain voltage was 0.1 V.

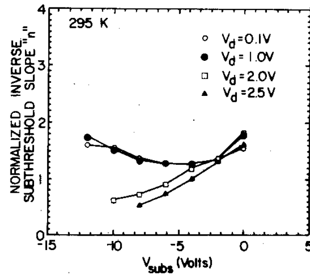

Fig. 2. Normalized inverse subthreshold slope "n" as a function of substrate bias and drain voltage at room temperature.

old slope on substrate bias. Models to explain these data will now be presented.

III. Results and Modeling

In the subthreshold region the drain current is proportional to the number of electrons injected over the source–channel surface barrier. The electrons subsequently diffuse to the drain. The current depends on the channel surface potential ϕ_s which is not directly controlled, but only coupled to capacitatively from the gate electrode. In the subthreshold region, the charge in the channel is negligible, and thus the change in channel potential with respect to gate voltage may be expressed as a simple capacitor–divider relationship

$$\frac{d\phi_{\text{surf}}}{dV_G} = \frac{C_{\text{gate}}}{C_{\text{gate}} + C_{\text{parasitic}}} \equiv \frac{1}{n} \tag{1}$$

where C_{gate} is the coupling between gate and channel and $C_{\text{parasitic}}$ represents all other capacitances coupling to the channel. Assuming that the electron distribution has zero width and is exactly at the silicon–silicon dioxide interface, C_{gate} is just the gate oxide capacitance. This coupling then leads to

$$I_D \propto e^{(q\phi_{\text{surf}}/kT)} \propto e^{(qV_G/nkT)}. \tag{2}$$

Hence the normalized subthreshold slope (n) data in Fig. 2 refer to the same n defined in (1), and thus subthreshold slope will clearly depend on parasitic channel capacitances.

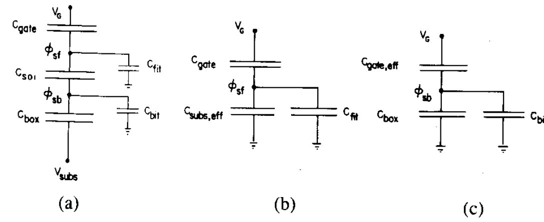

Fig. 3. (a) Capacitance model of the vertical SOI structure when the SOI film is depleted and effective capacitor model for gate-channel coupling efficiency for (b) depleted or accumulated lower interfaces, and (c) nearly inverted lower interfaces.

Fig. 3(a) shows capacitances associated with the SOI structure. C_{gate} is the gate capacitance, $C_{\text{SOI}} \equiv \epsilon_{\text{SOI}}/t_{\text{SOI}}$ is the capacitance of the SOI film body, and C_{box} is the capacitance of the underlying oxide. The front and back interface potentials (ϕ_{sf} and ϕ_{sb}, respectively) are coupled through C_{SOI} as pictured when the film is fully depleted. Interface-state capacitances C_{fit} and C_{bit} of the upper and lower SOI interfaces, respectively, have also been included. The capacitance of any possible depletion layer in the silicon substrate has been omitted for simplicity, but could be included into an effective lower oxide capacitance.

A. Small Drain Voltages

1) Depleted Lower Interface: When the lower interface is depleted, the potential at the lower SOI interface ϕ_{sb} can move, with a negligible change in the number of free carriers at the interface. The model of Fig. 3(b) is then valid, where $C_{\text{subs,eff}}$ represents the combination of C_{box} and C_{bit} (in parallel) in series with C_{SOI}. One finds

$$C_{\text{subs,eff}} = \frac{C_{\text{SOI}}(C_{box} + C_{bit})}{C_{\text{SOI}} + C_{box} + C_{bit}} \tag{3}$$

$$n = \frac{C_{\text{gate}} + C_{\text{subs,eff}} + C_{fit}}{C_{\text{gate}}}. \tag{4}$$

In the limit of a very thick underlying oxide and negligible interface states, $C_{\text{subs,eff}}$ approaches zero and n approaches its ideal minimum of 1.0 as first demonstrated by Colinge [2]. In the data of Fig. 2, for a drain voltage of 0.1 V, this minimum occurs for a substrate bias for ~ −5 V, indeed corresponding to the depleted lower interface condition of Fig. 1. The minimum "n" at room temperature for $V_D = 0.1$ is 1.3, however, not 1.0. Part of this discrepancy results from parasitic source-channel and drain-channel capacitances present in short-channel devices [3]. In all cases of substrate bias, a degradation in subthreshold slope is indeed seen in devices with a gate length under 2 μm, with the 2-μm and longer devices having a minimum $n \approx 1.15$. Given our SOI and gate oxide thickness and the finite lower oxide thickness of 3500 Å, one would expect a minium n of 1.07 if no interface states

were present. This difference between 1.07 and the measured 1.15 could be explained by an upper SOI-oxide interface state density of 7×10^{10} cm^{-2} · eV^{-1}, or a lower SOI-oxide interface state density of 8×10^{10} cm^{-2} · eV^{-1}, or some combination of these two.

It should be pointed out that given our SOI thickness and doping of 1000 Å and 1×10^{17} cm^{-3}, respectively, the band bending on the top SOI surface in the subthreshold (weak inversion regime) is ~0.6 V (compared to 0.8 V at threshold). According to the depletion approximation, this results in an 870-Å depletion, which is less than our film thickness. However, if the potential of the lower interface was raised by any small amount (~0.1 V) from flat band by the substrate bias, the film will be fully depleted because of the extra depletion from the lower interface, and the model of Fig. 3 is then valid. When the lower interface is accumulated (not depleted), the film will, strictly speaking, not be fully depleted. However, because the updepleted region (~130 Å) is small compared to the film thickness, the error in C_{SOI} will be neglected.

2) Accumulated Lower Interface: For large negative substrate–source bias (~ −10 V), the lower interface will be accumulated. This pins the potential at the lower SOI interface. The model of Fig. 3(b) is still valid, with the effective substrate capacitance now equal simply to the capacitance of the SOI film body. ($C_{\mathrm{subs,eff}} = C_{\mathrm{SOI}}$.) One now expects a degraded gate-channel coupling efficiency because C_{SOI} is large compared to the lower oxide capacitance which depressed $C_{\mathrm{subs,eff}}$ in the fully depleted case. In the long-channel limit

$$n = \frac{C_{\mathrm{gate}} + C_{fit} + C_{\mathrm{SOI}}}{C_{\mathrm{gate}}}. \tag{5}$$

This degradation in subthreshold slope is evident in Fig. 2 as the substrate bias is made more negative from −5 V, with $n = 1.8$ for a substrate bias of −10 V (lower interface accumulation according to Fig. 1). Assuming no interface states, (6) would predict $n \approx 1.7$, showing that the effect of interface states is negligible in this case.

3) Nearly Inverted Lower Interface: For sufficiently positive substrate bias, the initial conduction in the devices will be at the lower SOI-oxide interface, not at the conventional upper interface. Near the onset of this regime, the conduction can still be modulated by the top gate, although with a reduced coupling efficiency compared to conduction at the upper interface. The device can now be represented by a model similar to that of Fig. 3(b), but now we seek the coupling from the gate to the lower SOI-oxide interface as opposed to the top interface (Fig. 3(c)). $C_{\mathrm{gate,eff}}$ is an effective gate capacitance which represents this coupling from the gate electrode to the lower SOI-oxide interface potential. If one assumes C_{fit} is negligible

$$C_{\mathrm{gate,eff}} = \frac{C_{\mathrm{gate}} C_{\mathrm{SOI}}}{C_{\mathrm{gate}} + C_{\mathrm{SOI}}} \tag{6}$$

$$n = \frac{C_{\mathrm{gate,eff}} + C_{bit} + C_{box}}{C_{\mathrm{gate,eff}}}. \tag{7}$$

Since there is a lower effective gate capacitance and a higher parasitic channel capacitance in this case compared to those for the depleted lower interface (top channel conduction), a worse subthreshold slope (larger n) is expected.

It could be pointed out that with a substrate bias of 0 V a significant degradation of subthreshold slope is already observed, while according to Fig. 1 this is still the depleted lower interface condition. The three regions of Fig. 1 have been marked according to the lower interface charge condition when the upper interface is at the threshold condition. For $V_{\mathrm{sub}} \approx +2$ V, both interfaces are at the onset of inversion. If the gate voltage is then decreased from the threshold, both the upper and lower SOI surface potentials will decrease and both surfaces will enter the subthreshold regime. However, the upper potential will decrease faster than the lower potential since it is more closely coupled to the gate. The dominant conduction, although controlled by the gate voltage, will then clearly be at the lower SOI surface. This situation will still exist for slightly more negative substrate biases over large portions of the subthreshold curve, leading to a degraded subthreshold slope as just described. Thus the optimum subthreshold slope requires not only a depleted lower interface, but also negligible subthreshold conduction at the lower interface compared to the top interface.

B. Large Drain Voltages (>1 V)

For large drain voltages, the subthreshold slopes of Fig. 2 are similar to those of the small drain voltage case for a depleted lower interface or more positive substrate bias. For negative substrate biases, however, the results differ substantially from the low drain-bias case. The subthreshold slopes become anomalously sharp with $n < 1$. The sharp slopes are also accompanied by a reduction in threshold voltage compared to the small drain-bias thresholds of Fig. 1. Such effects have been reported previously in thick (~0.3 μm) SOI films that were not fully depleted [4], [5]. These effects are a serious impediment to the application of SOI to VLSI since they can cause early turn-on and a large off-current in transistors. The effects have been attributed [5] to the electron current causing a small hole current by avalanche at the drain junction. The holes get trapped in the SOI film body, raising its potential, thus lowering the threshold voltage which causes more electron current, and thus causing more holes in a positive feedback process.

These results differ from the previous results [4], [5] since in our experiments the SOI films are fully depleted, and it has been demonstrated here that the effect can be switched on and off by substrate bias. The dependence of anomalous slopes on substrate bias may be explained by a model similar to that used by Colinge to explain the absence of the "kink" effect (above threshold in saturation) in fully depleted SOI films [6]. Shown in Fig. 4 is

the electrical potential versus distance from source to drain in an SOI MOSFET in the subthreshold regime (flat-channel potential), plotted for both the upper and lower interfaces of the SOI film. The potential barrier from source to the top channel is on the order of a few tenths of an electron-volt. In Fig. 4(a) is the potential diagram for a fully depleted SOI film, indicated by little potential difference between the front and back of the SOI. Electrons traveling from source to drain will lie mostly at the top surface (higher potential). Electrons from avalanche will be collected by the drain, but holes from avalanche will go to the lower SOI interface (lower potential). Since the potential barrier from the source to the top channel is small in subthreshold, and the difference in potential between the surfaces is small, the holes face a relatively small barrier from channel to source. Therefore, holes will easily escape from the channel region to the source. Few holes will reside in the channel, and hence there is little shift in threshold voltages or anomalous feedback effects.

In the case of an accumulated lower interface (Fig. 4(b)) the lower SOI surface potential will differ substantially from that of the top surface, and holes from avalanche will face a large barrier (~ 1 eV) in order to escape the channel. Thus a large buildup of holes (to develop a bias to lower the barrier) will occur, leading to threshold-voltage lowering, feedback, and anomalous subthreshold slopes. It should be stressed that this is a qualitative model only, and it describes only the injection of holes from the SOI body under the channel to the source, and not recombination of the holes in the SOI body. Nevertheless, this result demonstrates that through control of the lower SOI interface charge condition, anomalously sharp subthreshold effects can be substantially reduced.

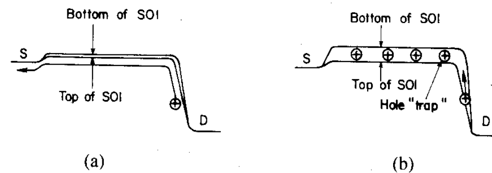

Fig. 4. Potential diagram of the upper and lower SOI surfaces of a depleted SOI transistor with (a) a depleted lower interface, and (b) an accumulated lower interface.

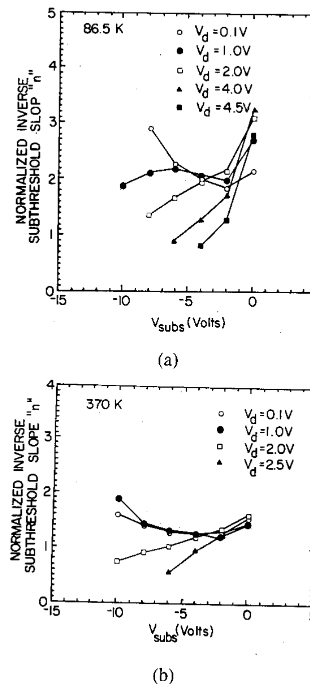

Fig. 5. Subthreshold slopes for the device of Fig. 2 at 86.5 K (a) and 370 K (b).

C. Temperature Dependence

Shown in Fig. 5 are subthreshold slope data versus substrate bias for the same device as in Fig. 2, but at 370 and 86.5 K. Qualitatively similar behavior is noted: a U-shaped curve for small drain voltages, and anomalously sharp slopes for an accumulated lower interface. Ideally, the normalized slope "n" should not depend on temperature. However, at 86.5 K, the minimum subthreshold slope for a drain voltage of 0.1 V was ~ 32 mV/decade, corresponding to $n = 1.8$, significantly larger than the minimum n at higher temperature. One possible explanation is that the subthreshold slope is degraded by spatial fluctuations in interface-state density [7]. The fluctuations might lead to insignificant effects at room temperature, but could cause substantially larger effects at lower temperature. Alternatively, the degradation at low temperature could result from a "U-shaped" density of interface states distribution with a minimum near midgap. Low temperature will require a greater surface potential for significant subthreshold current (compared to room temperature), resulting in the sampled interface states in the subthreshold regime at low temperature being nearer the conduction band, and hence larger in number [8]. Further work is needed to understand the details of this degradation. For larger drain voltages, anomalously sharp ($n < 1$) slopes are still seen at 86 K for accumulated substrates, just as at room temperature.

IV. Summary

Using a simple capacitive model, the substrate bias dependence of subthreshold slope in depleted silicon-on-insulator n-channel MOSFET's has been explained. The slope in all cases over a wide temperature range (86–370 K) depends on the charge state of the lower SOI–oxide interface. To obtain the best subthreshold slope in the case of small drain voltage, and to greatly reduce anomalous effects with large drain bias, a depleted lower interface is desired, with the dominant conduction occuring at the upper interface. This condition can easily be achieved for isolated devices by the application of an appropriate source–substrate bias. CMOS circuits require both p-MOS and n-MOS transistors, and the source voltage of the p-MOS devices is typically V_{DD} larger than that of the

n-MOS device. Choice of an optimum substrate bias in such circuits will require further investigation.

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