A System Based on Capacitive Interfacing of CMOS With Post-Processed Thin-Film MEMS Resonators Employing Synchronous Readout for Parasitic Nulling

Liechao Huang, *Student Member, IEEE*, Warren Rieutort-Louis, *Student Member, IEEE*, Alexandra Gualdino, Laura Teagno, Yingzhe Hu, *Student Member, IEEE*, João Mouro, Josue Sanz-Robinson, James C. Sturm, *Fellow, IEEE*, Sigurd Wagner, *Fellow, IEEE*, Virginia Chu, *Senior Member, IEEE*, João Pedro Conde, and Naveen Verma, *Member, IEEE*

***Abstract*—Thin-film MEMS resonators fabricated at low temperatures can be processed on CMOS ICs, forming high-sensitivity transducers within complete sensing systems. A key focus for the MEMS devices is increasing the resonant frequency, enabling, among other benefits, operation at atmospheric pressure. However, at increased frequencies, parasitics associated with both the MEMS-CMOS interfaces and the MEMS device itself can severely degrade the detectability of the resonant peak. This work attempts to overcome these parasitics while providing isolation of the CMOS IC from potentially damaging sensing environments. To achieve this, an interfacing approach is proposed based on capacitive coupling across the CMOS IC passivation, and a detection approach is proposed based on synchronous readout. Results are presented from a prototype system, integrating a custom CMOS IC with MEMS bridge resonators. With the MEMS resonators fabricated in-house at 175°C on a separate substrate, readout results with multiple different resonators are obtained. In all cases, the IC enables detection with >20 dB SNR of resonant peaks that are only weakly detectable or undetectable directly using a vector-network analyzer (VNA).**

***Index Terms*—Amorphous silicon, ASIC, MEMS, non-contact interface, resonator sensor, synchronous readout, thin-film technology.**

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L. Huang, W. Rieutort-Louis, Y. Hu, J. Sanz-Robinson, J. C. Sturm, S. Wagner, and N. Verma are with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08540 USA (e-mail: liechaoh@princeton.edu).

A. Gualdino, L. Teagno, J. Mouro, and V. Chu are with the INESC Microsistemas e Nanotecnologias and IN-Institute of Nanoscience and Nanotechnology, 1000-029 Lisboa, Portugal.

J. P. Conde is with the INESC Microsistemas e Nanotecnologias and IN-Institute of Nanoscience and Nanotechnology, 1000-029 Lisboa, Portugal. He is also with the Department of Bioengineering, Instituto Superior Técnico, Universidade de Lisboa, Portugal.

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I. Introduction

MICRO-ELECTRO-MECHANICAL systems (MEMS) have resulted in sensors with extremely small form factors and very high sensitivities, enabling a range of sensing applications [1]–[3]. Resonant-frequency transducers are a representative example. For a mechanical resonator, the resonant frequency, as a function of mechanical parameters, can be represented as follows [1]:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{k}{m} - \frac{c^2}{2m^2}}. \quad (1)$$

Here, m is the mass of the resonator, while k (~ 200 N/m) and c (~ 3 μg/s) are the effective spring constant and damping coefficient, respectively, both of which are strongly related to environmental factors such as pressure and temperature, in addition to device structure. Micro/nano fabrication has made devices possible with very small masses ($\sim$10 ng) and high quality factors (Q), resulting in high sensitivity to mass changes and high selectivity of the resonant-frequency point. For instance, taking the derivative of (1), sensitivity to mass changes can be estimated:

$$\frac{\Delta f}{f_{res}} \approx \frac{\Delta m}{4\pi m}. \quad (2)$$

The ability to detect small shifts in resonant frequency depends on the the sharpness with which the frequency peak falls off (i.e., Q factor). For instance, with devices having quality factor of $\sim$1000 (which is routinely achieved [1]) and critical mass of $\sim$10 ng, frequency shifts corresponding to the -3 dB bandwidth are caused by a change in mass on the order of just picograms. Of course, sensing systems aiming to exploit this require readout electronics capable of detecting such shifts and sharp peaks in the resanant frequency.

Of particular interest is the integration of MEMS devices with CMOS ICs, to form complete systems for sensing. While monolithic MEMS represent the highest level of integration, strict fabrication requirements for both MEMS and CMOS limits compatibility, restricting the devices possible. On the other hand, post-processed MEMS, typically based on thin-film

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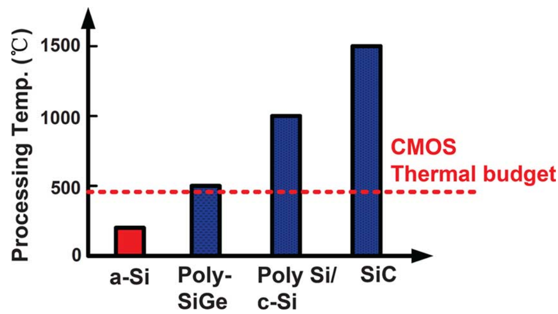


Fig. 1. Process temperatures of different materials for MEMS. SiC is purposely designed for high temperature sensing, Poly-Si/c-Si is mainly used for pre-CMOS or intra-CMOS micromachining, Poly-SiGe is one of today's main trends for post-CMOS integration, which just meets the thermal budget.

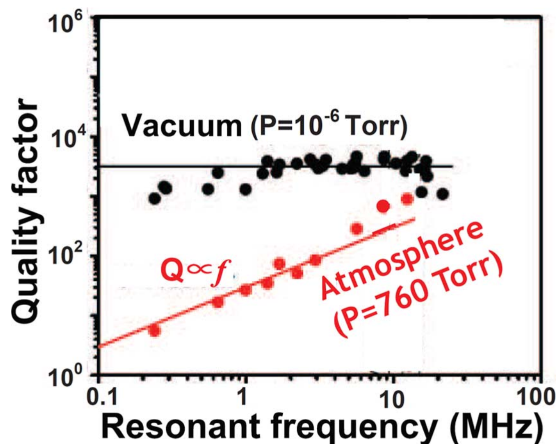


Fig. 2. Measured a-Si MEMS resonator's Q versus frequency under vacuum and atmosphere respectively, indicating a high frequency resonance at reduced vacuum.

processing after CMOS fabrication, presents broad possibilities. However, post processing must be limited to temperatures compatible with the fabricated CMOS devices [4]. Fig. 1 shows the typical processing temperatures for various materials used to fabricate thin-film MEMS [5]–[7]. CMOS temperature restrictions make amorphous silicon (a-Si) a potential choice for post-processed MEMS.

Despite the sensitivities and the prospects for integration, a general challenge that limits the application of MEMS resonant-frequency sensors is the need to operate devices under vacuum conditions. This restricts the interaction of the devices with the environment in which sensing is to be performed. To overcome this, a general trend has been to engineer devices with high resonant frequencies [8]. Experimental data, as in Fig. 2, shows that the need for vacuum conditions is mitigated at higher frequencies (10–100 MHz). Engineering the electro-mechanical parameters to achieve higher frequencies presents challenges with respect to MEMS fabrication since specialized structures and vibration modes are often required [3], but it also presents challenges with respect to CMOS integration and readout, due to elevated impact of electrical parasitics.

The focus of this paper is a CMOS integration strategy and readout architecture that aims to overcome the effects of these parasitics for post-processed a-Si thin-film MEMS resonators. In particular, two challenges are addressed:

1) **Interfacing.** Direct bonding of post-processed MEMS via an exposed bond pad has two adverse consequences. First, various bond pads all have substantial parasitics ($>$ 100fF) [9]. This shunts away the small currents generated by the MEMS resonator, making the resonant peak difficult to detect. Second, bond-pad openings expose CMOS to the sensing environment, which might be damaging. This work focuses on non-contact coupling between the CMOS and MEMS via capacitor plates patterned across the top-level passivation of CMOS IC.
2) **Readout.** Current due to parallel parasitic capacitances across the MEMS resonator, caused due to both the device structure and typical routing to the device electrodes, can dominate over the current through the resonator. This once again makes the resonant frequency peak difficult to detect. This work focuses on synchronous readout, wherein the phase response of the resonator current and the parasitic-capacitance current is used to accentuate the resonant peak.

The rest of the paper is organized as follows. Section II presents details of the a-Si MEMS bridge resonators we fabricate and use in this work, emphasizing the electrical characteristics in the context of the interfacing and readout challenges. Section III describes the capacitive non-contact interfacing used between the CMOS and MEMS devices. Section IV presents the readout circuit architecture and details. Section V presents system measurements, and finally Section VI concludes.

II. MEMS Fabrication and Challenges

This section starts by describing the fabrication process employed for the a-Si thin-film MEMS bridge resonators, summarizing the typical device parameters obtained. Then, it quantitatively illustrates the readout challenges faced as we increase the resonant frequency in the presence of parasitics.

A. MEMS Fabrication

The MEMS resonators used in this paper consist of bridge structures 25 μm wide and between 50-100 μm long, over a centered titanium-tungsten (TiW) gate electrode. All components of the resonator are fabricated by thin-film processing and surface micromachining on 0.8 cm $\times$ 0.8 cm glass substrates.

Fig. 3 illustrates the fabrication procedure. A 70 nm thick TiW layer is deposited on a clean glass substrate and the bridge/gate electrodes patterned by photolithography and reactive ion etching (RIE). A sacrificial aluminium layer, between 200 nm and 1 μm thick, is patterned on top of the gate electrode, followed by a 100 nm-thick layer of TiW. A 2 μm-thick structural layer of doped (n^+) amorphous silicon is subsequently deposited by PECVD at a maximum temperature of 175°C and patterned by RIE. The sacrificial layer is finally etched off, defining the air gap (d) under the bridge. While reducing the height of this gap is favourable for increasing the strength of the resonant behavior, heights less than 200nm are more challenging to fabricate with high yield and are more vulnerable to bridge collapse.

In order to achieve resonance, a DC bias and an AC stimulation are applied between the gate of the bridge and the bridge

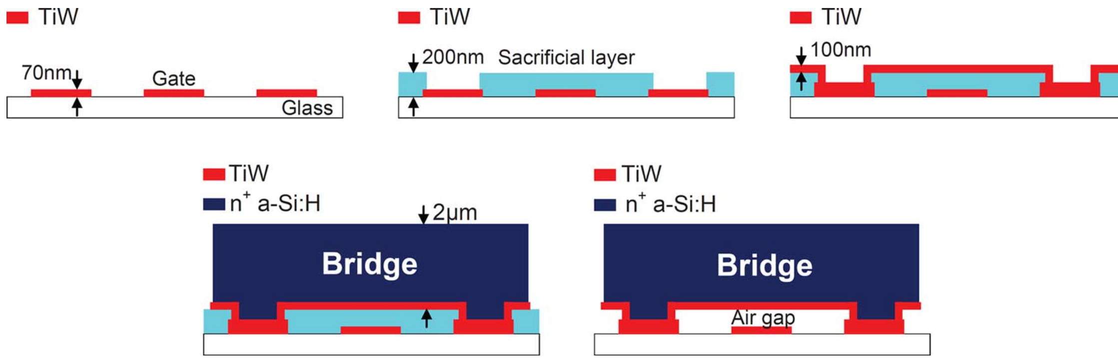


Fig. 3. Fabrication process of the a-Si MEMS bridge resonator.

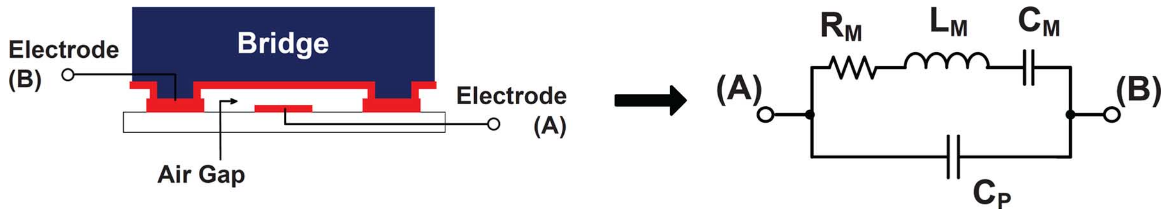


Fig. 4. The equivalent circuit model for MEMS resonator.

structure. Typical values for the AC voltage are 100–300 mV. Typical values for the DC voltage (V_g) range from 5–10 V for narrow gap bridges (e.g., 200 nm) to 20–30 V for wide gap bridges (e.g., 1 μm). This DC voltage directly impacts the electrical parameters of the resonator (as shown in Section II-B), with larger voltages typically enhancing the resonant response [1]. However, application of too large a DC voltage can cause excessive electrostatic attraction between the gate and bridge, resulting in the collapse of the MEMS bridges.

B. Readout Challenges

To quantify the challenges and specifiy the readout requirements faced at the frequencies of interest, we adopt a widely used electrical model for the bridge resonators, developed along with explanation of assumptions in [10]. Under the assumption that the strain response of the structure is linearly proportional to its displacement (which is valid for the displacements of ~10 nm seen in our structures) it can be shown, by applying Ohm's law and Newton's second law, that the equivalent circuit illustrated in Fig. 4 models the electromechanical motion of the one-dimensional damped harmonic resonator, under biasing (V_g) applied between the underlying gate electrode A and the bridge electrode B. The circuit comprises an equivalent series RLC network, representing mechanical motion through the motional parameters R_M, L_M, C_M, and a parallel parasitic capacitor C_P, representing electrostatic coupling between the gate and bridge electrodes. The series RLC implies that a resonant peak will occur in the transmission current when an AC voltage is applied across electrodes A and B; however, as we show below, the transmission current can be easily drowned out by a parasitic current through the capacitor C_P. To characterize this effect, we start by specifying the motional parameters, whose values are derived from the mechanical and electrical parameters of the device:

$$L_M = \frac{d^2 m}{{V_g}^2 {C_g}^2}, \quad C_M = \frac{{V_g}^2 {C_g}^2}{{\omega_0}^2 d^2 m}, \quad R_M = \frac{\omega_0 d^2 m}{{V_g}^2 {C_g}^2 Q}. \quad (3)$$

Here, m is the effective (lumped) resonator mass, d is the air gap between the bridge and the bottom electrode, ω_0 is the resonant angular frequency, and Q is the quality factor. Additionally, V_g is the applied bridge bias, and C_g is the intrinsic parallel-plate capacitor given by (4) (note, C_g is included in C_P, but is typically much smaller)

$$C_g = \varepsilon \frac{WL}{d}. \quad (4)$$

To consider the readout challenges brought on as bridges are designed to have higher resonant frequency, we start by extracting parameter values of the electrical model by measuring a typical fabricated bridge (width: 25 μm, length: 80 μm, thickness: 2 μm, gap: 0.2 μm). Fig. 5 shows the impedance between electrodes A and B obtained by a vector-network analyzer (VNA) through direct microprobing of the device. From this, the parameters of the electrical model can be extracted [10]. Corresponding values are provided in the right-hand table. The simulated transmission curves generated from the extracted values are also shown overlaying the measured curves, confirming good agreement. Several points are worth noting. First, though a large Q is achieved (electrically measured to be 362), R_M $(750\,\text{k}\Omega)$[1] is also large, implying that the current through the RLC network, even at resonance, is quite small. Second, the 90° baseline phase implies that the parasitic path is capacitive as predicted. As a side note, we see from the VNA sweeps that this prevents the network from achieving a phase of zero degrees, which would preclude the use of the resonator in typical oscillator topologies [11]. In particular, substantial C_P $(\sim 100$ fF) is obtained even from direct microprobing. We

[1] R_M's of 100 kΩ–1 MΩ are typically reported, though very aggressive geometries have led to lower values as in [11]

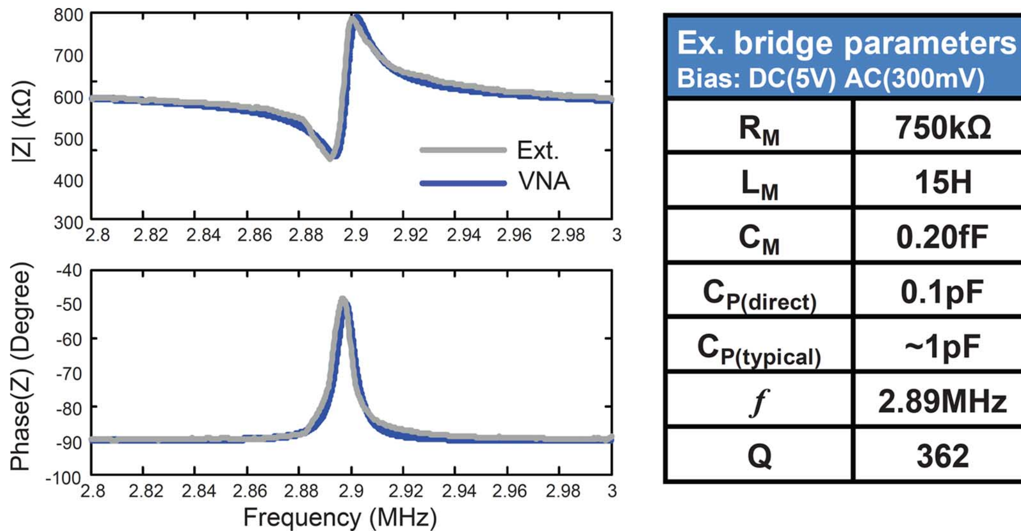


Fig. 5. a-Si MEMS resonator's resonant peak measured by direct microprobing the MEMS device by VNA and corresponding extracted model parameters.

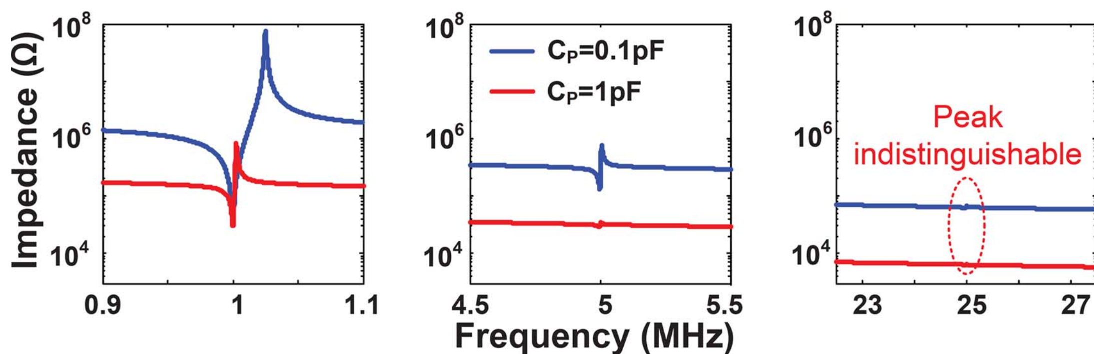


Fig. 6. Simulated resonator's peak with different feedthrough capacitor C_P and resonant frequencies.

treat this level of capacitance as being intrinsic to the device and referred to is as $C_{P(direct)}$ in Fig. 5. In fact, typical routing to the device electrodes is expected to make C_P even larger. The capacitance that results is referred to as $C_{P(typical)}$, and has been measured to be as high as $\sim$ 1 pF even in samples where some explicit attempts have been made to optimize the routing. Starting from the parameters for a typical device, we consider the implications of engineering devices for higher resonant frequencies. Assuming the Q is constant (as suggested in the data of Fig. 2), we assume scaling of L[1], [8], with values of 136 μm, 60 μm and 27 μm. Fig. 6 shows the expected impedances from simulation, assuming a C_P of both 100 fF and 1 pF. The resonant peak is increasingly indistinguishable, even for $C_P = 100$ fF. In Section IV, we describe the readout approach proposed wherein phase synchronization is employed to null the C_P current and accentuate the RLC current at resonance, thus restoring detectability of the peak.

III. CMOS-MEMS Interfacing

Interfacing MEMS with CMOS involves a number of important considerations. Currently, the dominant strategies employ system-in-package solutions, wherein the MEMS device is interfaced via an exposed bond pad. The problem with this is that the bond-pad capacitance can easily filter the small resonator currents. For example, taking the R_M extracted for the bridge considered above, a bond-pad capacitance of 500 fF–5 pF would result in a pole at $\sim$ 50 k–500 kHz, well below the resonant frequencies of interest. Even if the capacitance of the IC bonding structure is reduced, a critical problem that remains is the exposure of the CMOS chip to the sensing environment, which generally can be harsh and damaging. Current strategies for isolation employ tight barriers based on specialized materials [12], elevating assembly complexity. To address both the interfacing parasitics and isolation, this work focuses on non-contact interfacing across the chip passivation.

Non-contact interfaces can be implemented using either capacitive or inductive coupling. In considering inductive versus capacitive interfaces, we make the distinction between MEMS devices whose sensing response is (1) a change in an intrinsic capacitance C_{MEMS}, versus (2) a change in resonant frequency due to an intrinsic motoional RLC network. The attributes of each are summarized in Fig. 7. Inductive coupling (as proposed in [13]) is preferred for MEMS sensors based on measuring capacitance change, not resonator frequency change. For devices that provide sensing based on change in capacitance, the MEMS sensor and coupling inductor can form a resonant network, making capacitance change detectable as a shift in the resonant frequency. On the other hand, for devices that provide sensing based on a change in resonant frequency, C_P masks the impedance/conductance change due to the motional RLC.

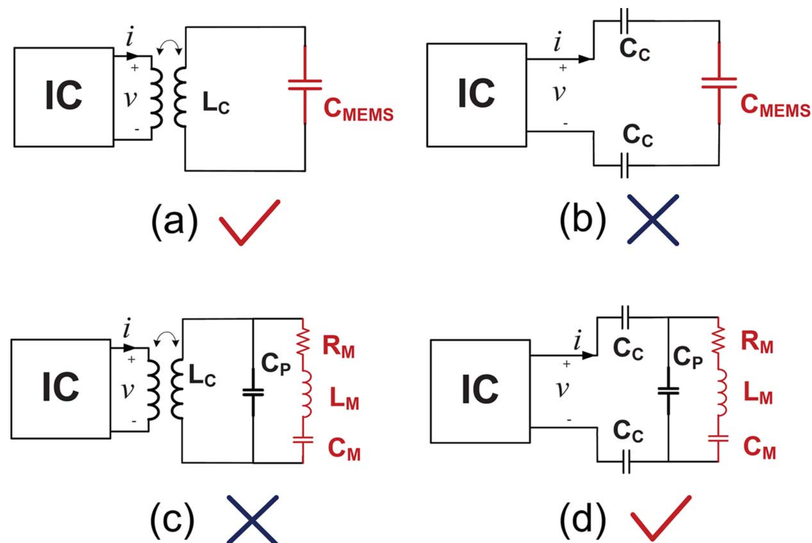


Fig. 7. Summary of different non-contact interfaces to MEMS sensors. Inductive interface is preferred when MEMS sensor is applied as a capacitor while capacitive interface is preferred when MEMS applied as a resonator.

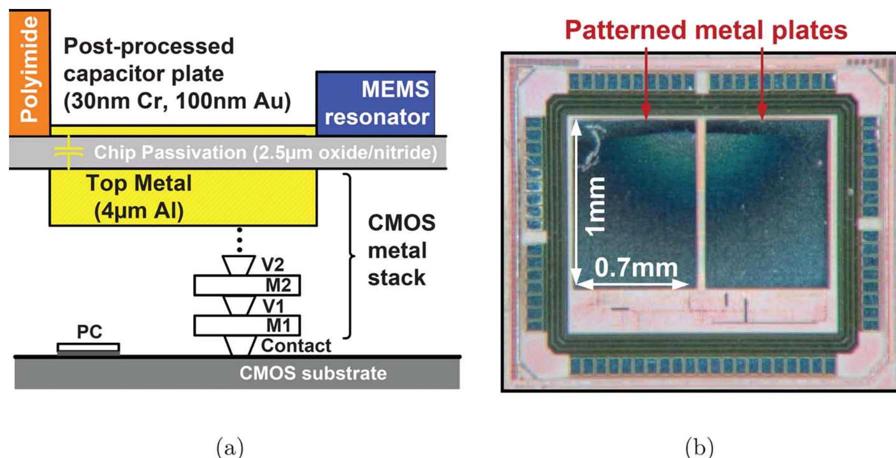


Fig. 8. (a) Cross-section view of the CMOS chip and its capacitive interface to MEMS. (b) Die photo with post-processed metal plate.

To cancel C_p, an interface inductor can be considered; however, tuning the inductor to a particular frequency is unviable (due to difficulty in precisely prediciting C_P) and inadequate (since sensing response causes shifts in the intrinsic resonant frequency).

On the other hand, capacitive coupling readily provides interfacing with the MEMS resonator. The key consideration is that the coupling capacitor should not degrade readout of the resonator current. Specifically, the capacitive interface should present series impedance well below R_M. Taking the R_M and resonant frequency from above as an example, 5 pF capacitors would be adequate and can be further reduced as the targeted resonant frequencies increase. Accordingly, Fig. 8(a) shows the capacitive interfacing employed in this work. The coupling capacitor is formed across the CMOS oxide/nitride passivation using the top metal layer of the CMOS process and a post-processed metal stack consisting of chrome (30 nm) and gold (100 nm). The post-processed metal plate is formed by first etching a layer of polyimide, and then a photoresist barrier is patterned to align with the bottom capacitor plates (formed from the CMOS top metal layer). Following this gold is evaporated and undesired metal regions (defined by the photoresist) are removed via a liftoff process. Fig. 8(b) shows the post-processed CMOS die with patterned capacitor plates; these are used to interface to the MEMS devices, which are fabricated on a separate glass substrate to facilitate testing with multiple resonators having various parameters. The 1 mm $\times$ 0.7 mm plates give a measured capacitance of 15 pF each, well beyond that required for interfacing to the targeted MEMS bridge resonators. Moreover the alignment resolution of the post processing is better than 5 μm, enabling robust formation of the interface for the plate sizes employed.

IV. CMOS Readout System

This section presents details of the CMOS system, which uses synchronous readout both to negate the effects of the MEMS parasitic capacitor C_P and to emphasize the resonant current of the MEMS RLC network. Fig. 9 shows the architecture. The principle of operation is as follows. A drive signal V_{SW} is applied to the MEMS resonator, and its frequency is swept to find

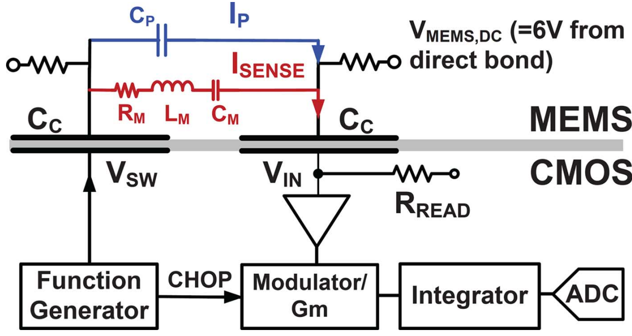
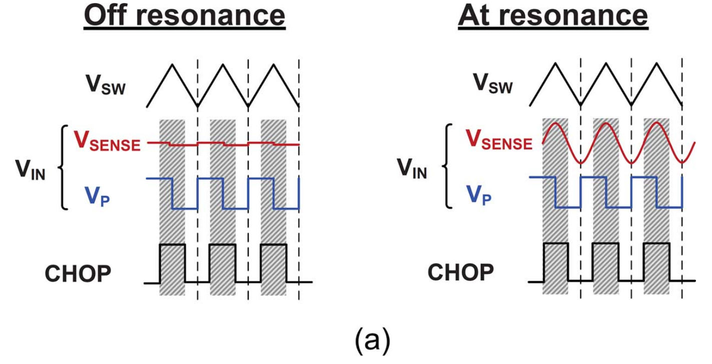


Fig. 9. Readout system block diagram.



	Off resonance		At resonance	
	Amp.	Phase	Amp.	Phase
I_P	*Constant*	*90°*	*Constant*	*90°*
I_{SENSE}	*Min.*	*90°*	*Max.*	*0°*

(b)

Fig. 10. Parasitic cancellation approach. (a) waveforms of the system signals for at resonance and off resonance. (b), Summary table for amplitude and phase of sensing signal (I_{SENSE}) and parasitic feedthrough signal (I_P) at resonance and off resonance.

the resonant point. V_{SW} is generated by an on-chip function generator and applied through the top-metal coupling capacitor. This results in readout currents I_P and I_{SENSE} through the MEMS C_P and the MEMS RLC, respectively. The readout currents are returned to the CMOS chip through the second top-metal coupling capacitor, and pass through the input resistor R_{READ} to generate a voltage V_{IN}. As long as the series impedance of the coupling capacitors ($C_C||C_C$) and R_{READ} is much lower than that of the MEMS C_P and RLC at the frequencies of interest, the phases of both I_P and I_{SENSE} are preserved with respect to V_{SW}. In particular, I_P is 90° out of phase with V_{SW}, while I_{SENSE} is either out of phase or in phase, depending on the resonance condition. Accordingly, V_{IN} is composed of voltages V_P and V_{SENSE}, respectively, with corresponding phases. Following amplification, the voltages are modulated within a transconductance stage, by a signal $CHOP$ that is in phase with V_{SW}. This has the effect shown in Fig. 10(a):

- **Off resonance**. Both I_P (set by C_P) and I_{SENSE} (set by C_M or L_M), are 90° out of phase with $CHOP$. Thus both are nulled regardless of their amplitudes.
- **At resonance.** I_P is once again out of phase with $CHOP$ and thus nulled. However, I_{SENSE} (set by R_M) is now both maximum in amplitude *and* in phase with $CHOP$. I_{SENSE} is thus modulated to a baseband signal.

These conditions are summarized in Fig. 10(b), indicating both the amplitude and phase with respect to the resonance condition. After modulation, the currents are integrated within an integrating ADC for digitized readout.

Analytically, the nulling of I_P can be modelled as follows. Consider the simplified circuit *at resonance*, shown in Fig. 11 (wherein the coupling capacitors have been grouped together into $C_C/2$). For simplicity, we consider V_{SW} and $CHOP$ to be sinusoids, $V_{IN}\sin(\omega t)$ and $V_{CH}\sin(\omega t)$, respectively. We seek to find the ratio between I_P and I_{SENSE} both before and after modulation. With the applied V_{SW}, the voltage generated across the MEMS device is $V_X = V'\sin(\omega t + \phi)$, with some relative phase ϕ. Thus, at resonance, I_P and I_{SENSE} are given as follows:

$$I_{SENSE} = \frac{V'}{R_M}\sin(\omega t + \phi) \tag{5}$$

$$I_P = V'\omega C_P \sin(\omega t + \phi). \tag{6}$$

While these currents reflect values at resonance, we note that off resonance I_P will remain roughly the same and I_{SENSE} will be comparatively be much smaller. The reason is that the overall impedance of the MEMS resonator is dominated by $1/(\omega C_P)$ at the frequencies of interest (i.e., compared to ωL_M or $1/(\omega C_M)$ off resonance and R_M at resonance). Thus, V_X remains roughly constant, and I_{SENSE}/I_P can be used to estimate the height of the resonant peak. Before modulation, the height is given as follows:

$$\frac{I_{SENSE}}{I_P} = \frac{1}{R_M\omega C_P}. \tag{7}$$

Large R_M, high target frequency, and typical values for C_P make this ratio small, degrading the ability to detect resonant peaks. However, after modulation by $CHOP = V_{CH}\sin(\omega t)$, the following currents are obtained:

$$I_{SENSE,mod} = \frac{V'V_{CH}}{R_M}\cos(\phi) \tag{8}$$

$$I_{P,mod} = V'V_{CH}\omega C_P \sin(\phi). \tag{9}$$

These result in the following ratio:

$$\frac{I_{SENSE,mod}}{I_{P,mod}} = \frac{1}{R_M\omega C_P \tan(\phi)}. \tag{10}$$

From the circuit in Fig. 11, $\tan(\phi)$ can be derived, giving the following value:

$$\tan(\phi) = \frac{\dfrac{\omega R_{READ}C_C}{2} - \dfrac{1}{\omega R_M C_P}}{\dfrac{C_C}{2C_P} + 1}. \tag{11}$$

For the circuit values chosen, $\tan(\phi)$ can be made very small, enhancing the ratio in (10). In particular, C_C is chosen to be larger than C_P and R_{READ} is chosen to be *much* smaller than

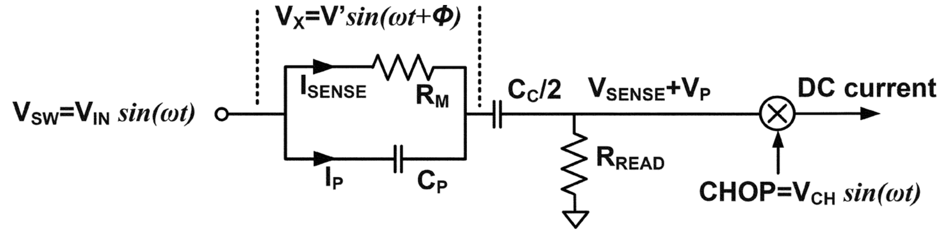


Fig. 11. An analytic model for proposed parasitic cancellation approach.

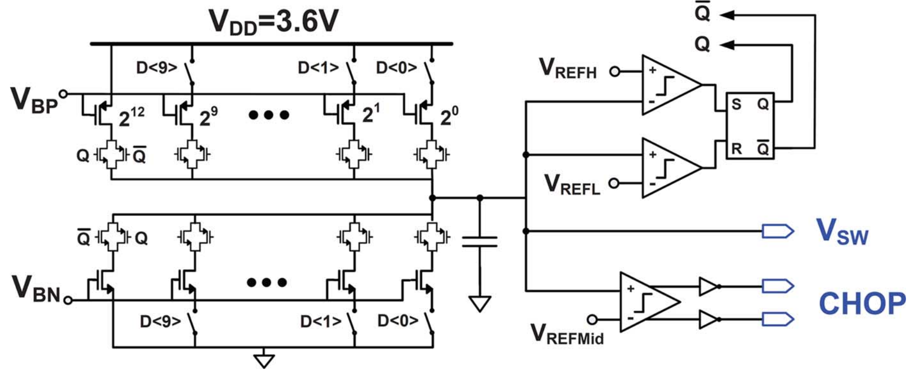


Fig. 12. Schematic of the function generator.

R_M. This drives the numerator to zero and makes the denominator larger than unity. As an example, employing the values used in this design ($R_M = 750$ kΩ, $R_{READ} = 100$ Ω, $C_C = 15$ pF and $C_P = 1$ pF) $\tan(\phi) = -9\text{e}-3$ at the typical resonant frequency of $f = 2.89$ MHz (as measured in Fig. 5). Thus, the observability of resonant peak is substantially enhanced due to attenuation of the quadrature-phase signals.

In the system, Fig. 9 shows that a 6 V DC bias is applied to the MEMS resonator, required to achieve adequate resonant response (high Q). This is provided from off chip through large biasing resistors ($\sim$ 10 MΩ) via direct routing and bonding. Thus physical isolation of the CMOS circuits is maintained, and readout of I_{SENSE} is not substantially affected, since the biasing resistors are much larger than both R_M and R_{READ}. We also point out that in an eventual system, power to the CMOS IC can be provided wirelessly to maintaining physical isolation.

The following subsections describe the circuit blocks employed in the readout system.

A. Function Generator

The function generator, responsible for generating V_{SW} and $CHOP$, is a critical block in the readout system. It must have adequate frequency-sweep resolution to capture narrow resonant peaks, sufficient frequency-sweep range to accommodate resonator frequency shifts in sensing applications, and low phase noise to maintain the sensitivity with which resonant peaks can be detected. At the frequencies of interest, on-chip LC oscillators are not viable. Thus the digitally-controlled relaxation oscillator shown in Fig. 12 is employed. This generates a triangle wave V_{SW}, which is filtered to a sinusoid by the high-Q RLC branch of the MEMS resonator and transformed to a square wave by the parasitic C_P branch. The $CHOP$ signal is derived through a comparator applied to the generated triangle wave.

Ten bit digital control $(D{<}9{:}0{>})$ is provided through switched current sources in feedback, which increase the oscillation frequency with respect to a base frequency. To enable testing with a wide range of MEMS devices, off-chip biasing (V_{BP}/V_{BN}) is used both to set the base frequency and the frequency step of the digital control. Transistor values are set such that the digital control gives a total sweep range that is one-quarter of the base frequency enabling coverage over a large frequency-shift range for sensing. With respect to sensing resolution, this results in a nominal frequency resolution of 1/4096 with respect to the chosen base frequency. Given resonant peaks with Q of $\sim$1000, this resolution yields 4–5 samples within the -3 dB bandwidth, to ensure robust capture. The plot in Fig. 13 shows the measured frequency versus DCO code.

The phase noise of a relaxation oscillator has been analyzed in detail in [14]. Generally, two noise sources are of concern: (1) comparator noise affecting the feedback signals $Q/\overline{Q}$; and (2) current-source noise appearing at the comparator input. The impacts of these sources on the oscillator's frequency resolution are given below:

$$\left(\frac{\sigma_{\Delta f_{OSC}}}{f_{OSC}}\right)_{vn} = \alpha\frac{\sqrt{S_{vn}B_n}}{V_H - V_L} \tag{12}$$

$$\left(\frac{\sigma_{\Delta f_{OSC}}}{f_{OSC}}\right)_{in} = \frac{\sqrt{\frac{S_{in}f_{OSC}}{2}}}{I_{charge}}. \tag{13}$$

S_{vn} is the power-spectral density (PSD) of the comparator's input-referred noise, B_n is the comparator's noise bandwidth, and S_{in} is the PSD of the current-source noise. Within the readout system, this noise is effectively averaged during integration of the modulated currents. Thus, integration over N

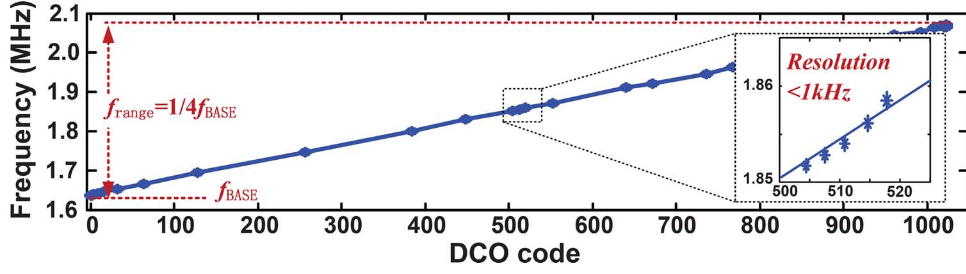


Fig. 13. Measured frequency of the function generator versus DCO code, showing a wide sweep range with high resolution.

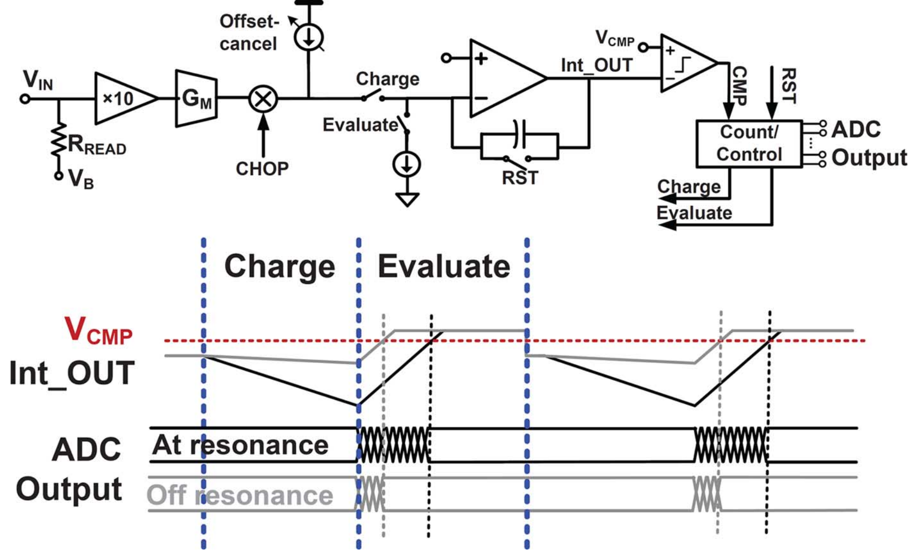


Fig. 14. Block diagram of the readout instrumentation and timing diagram.

clock cycles (via the dual-slope ADC described below) results in reduced noise according to

$$(\frac{\sigma_{\Delta f_{OSC}}}{f_{OSC}})_{effective} = (\alpha\frac{\sqrt{S_{vn}B_n}}{V_H - V_L} + \frac{\sqrt{\frac{S_{in}f_{OSC}}{2}}}{I_{charge}})\frac{1}{\sqrt{N}}. \quad (14)$$

From (14), we see that two tradeoffs arise when enhancing the frequency resolution of the function generator:

1) Increasing the swing of the triangle wave $V_H - V_L$ (by increasing the power supply) or increasing the charge current of the current source leads to higher power consumption.
2) Increasing the integration cycles N reduces the readout speed.

In this work, we maximize the swing of the triangle wave by using a 3.6 V V_{DD} to power the function generator, and we employ a large current ($\sim$ 1 mA) for the base current sources. As a result, the function generator's power consumption dominates the system.

B. Modulator and Dual-Slope ADC

Fig. 14 shows the circuit block diagram and timing waveforms of the modulator and dual-slope ADC. The AC currents from the MEMS resonator are converted to a voltage through the resistor R_{READ} and amplified by a gain stage $(10\times)$. The resulting voltage is fed to a transconductor (G_M stage) with an output modulator. The modulated signals are then integrated by an op-amp with capacitor feedback. Together with V_{SW}, which induces the AC currents, this forms a synchronous $G_M - C$ integrator. As mentioned previously, off resonance, the modulation substantially attenuates the currents from both the C_P and RLC branches of the MEMS resonator while at resonance, the current from the RLC branch is preserved. After integrating the modulated MEMS current, a constant current is applied to the integration capacitor, and analog-to-digital conversion is performed at the 11-b level by counting the discharge time.

1) Input Amplifier: Fig. 15 shows the circuit of the input amplifier. The small R_{READ} $(100\ \Omega)$ and large C_C (15 pF) are chosen to preserve the phase of the currents (I_P and I_{SENSE}) from the MEMS resonator to ensure the correct operation during synchronous readout. In particular, to maintain the current phase with respect to V_{SW}, R_{READ} should be smaller than R_M and C_C should be larger than C_P. The amplifier input capacitance C_{in} could also affect the phase. Despite substantial C_{in} ($\sim$4 pF), due to a transistor sizing for large transconductance (and thus reduced input-referred noise), the phase impact is negligible, once again, thanks to small-valued R_{READ}, which thus sets the input impedance. The amplifier is implemented as a common-source stage loaded by a diode-connected PMOS. In addition to the function-generator phase noise, the

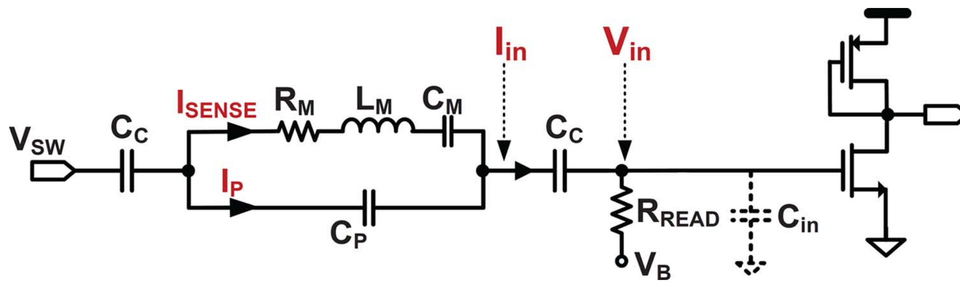


Fig. 15. Schematic of the input amplifier.

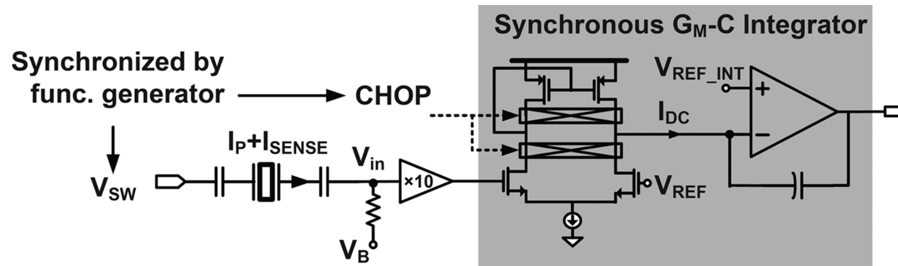


Fig. 16. Schematic of the synchronous G_M-C integrator.

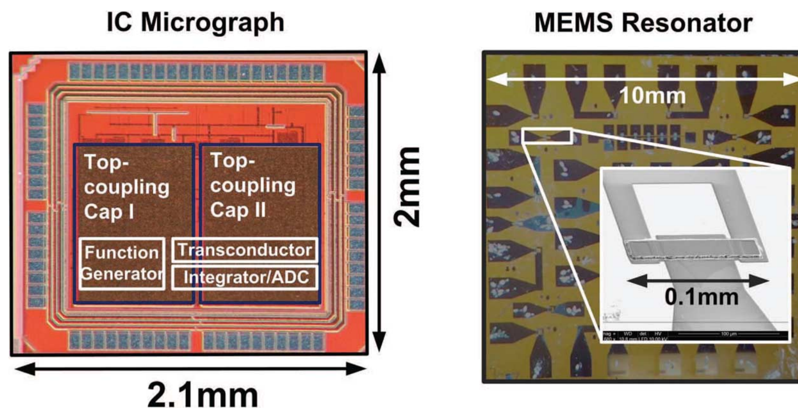


Fig. 17. Die photo of CMOS readout chip and MEMS resonator.

voltage noise of the input stage limits the readout sensitivity. The input-referred noise (including contributions from the subsequent integration stage) is measured to be 290 nV_{rms}.

2) Synchronous G_M-C Integrator: Fig. 16 shows the synchronous G_M-C integrator. The G_M stage provides a transconductance of 600 μA/V and implements signal modulation. The integrator is implemented as an op-amp with a feedback capacitor. The op-amp is a two-stage design with Miller compensation. The integration capacitor is chosen to be 500 pF, with an area of 0.5 mm $\times$ 1.4 mm, to accommodate longer integration times, motivated by the noise considerations mentioned previously. As mentioned previously, the function generator employs a relaxation oscillator, providing a triangle wave (rather than a sinusoid). Thus, current through the C_P branch of the MEMS resonator is transformed into a square wave, exhibiting positive and negative steps. Adequate rejection of the harmonics without distorting the signal amplitude would be challenging, requiring several stages of filtering. Instead, the transconductor and integrator are designed to preserve the resulting square wave with a step response having $\sim$4 ns of settling time. This ensures nulling of the C_P current, with negligible effect on the overall power consumption (which is dominated by the function generator).

V. System Measurements

Fig. 17 shows the die photo of the CMOS chip and a separate sample with multiple MEMS bridge resonators. The CMOS chip is fabricated in an IBM 130 nm technology while the MEMS sample is fabricated in house at 175°C on a glass substrate. The active area of the CMOS circuits is 0.4 mm $\times$ 1 mm. The use of a separate sample for the MEMS resonators enables testing with various different bridges, as described below. To interface the CMOS chip to the MEMS resonators, the non-contact strategy described Section III is used. With an area of 1 mm $\times$ 0.7 mm, each of the coupling capacitors is measured to have a value of 15 pF.

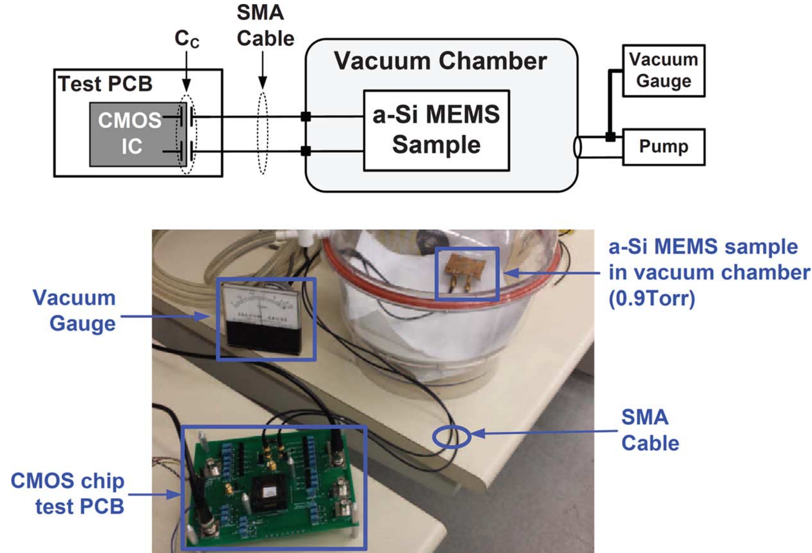


Fig. 18. Test setup for the CMOS-MEMS readout system.

Fig. 18 illustrates the test setup used to acquire the measurement results presented. The MEMS sample is placed in a vacuum chamber with a pressure of 0.9 Torr. The CMOS IC (on a custom PCB) is connected to the MEMS sample via the SMA cables shown. The cables introduce additional parasitics ($\sim$ 100 pF to ground and $\sim$ 100 fF in parallel), exacerbating the adverse effects that the proposed interfacing and readout architecture aim to overcome. Thus, the measurements reflect highly conservative conditions.

To evaluate the synchronous readout approach, we first isolate the output response with respect to the input signal phase. The approach taken is illustrated in Fig. 19(a). A sinusoidal wave of amplitude 200 mV and a digital $CHOP$ signal are generated using a bench-top function generator (Tektronix AFG3102). The phase of the two signals is then swept, giving the ADC readout with code-RMS error bars shown in Fig. 19(b). As shown, attenuation of out-of-phase signals is achieved.

Next, to evaluate readout of the resonant peaks associated with different MEMS devices, we first characterize the MEMS devices. This is done using a VNA, both through direct microprobing of the resonators (to minimize the effects of parasitics) and through typical routing on the sample. Then, we perform readout using the CMOS IC. Fig. 20 shows measurement results from four different MEMS resonators. On the left, the impedance magnitude obtained from VNA measurements is shown for direct probing (dashed curves) and for typical routing (solid curves), which yields a parallel capacitance C_P of $\sim$1 pF. In both cases, the resonant peak is only weakly measurable. On the right, digitized readout from the IC is shown along with code-RMS error bars. Clear peaks are observed with an SNR greater than 20 dB in all cases. For comparison with the VNA measurements, peak observability is defined as the ratio of the peak height to the baseline as marked in Fig. 20. The bar graph in Fig. 21 shows that, compared with both direct probing and typical routing, the proposed readout approach is able to greatly

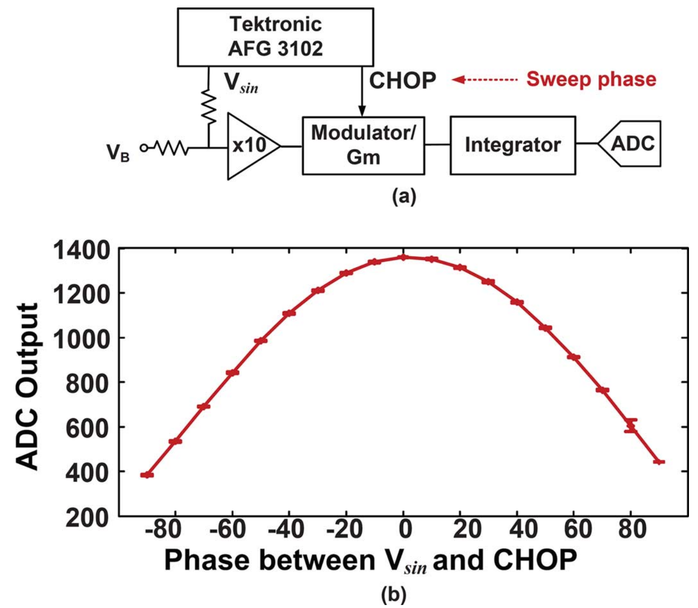


Fig. 19. Isolated test for signal cancellation based on phase.

improve the detectability of peaks (despite the additional parasitics introduced by the measurement setup).

To demonstrate an application, we employ the readout system for ambient environmental-pressure sensing, as suggested in [1]. Pressure sensing has been achieved through a variety of approaches, perhaps mostly commonly capacitance response due to displacement of plates due to pressure (e.g., [15]). References [16] and [17] present devices specially engineered to generate response under reduced pressures. However, to the best knowledge of the authors, integrated systems for low pressure sensing based on resonant-frequency response of MEMS devices have not been reported. In this work, we measured the resonant frequency under various pressures using both the VNA (direct probing) and the CMOS IC. The resonant frequencies observed

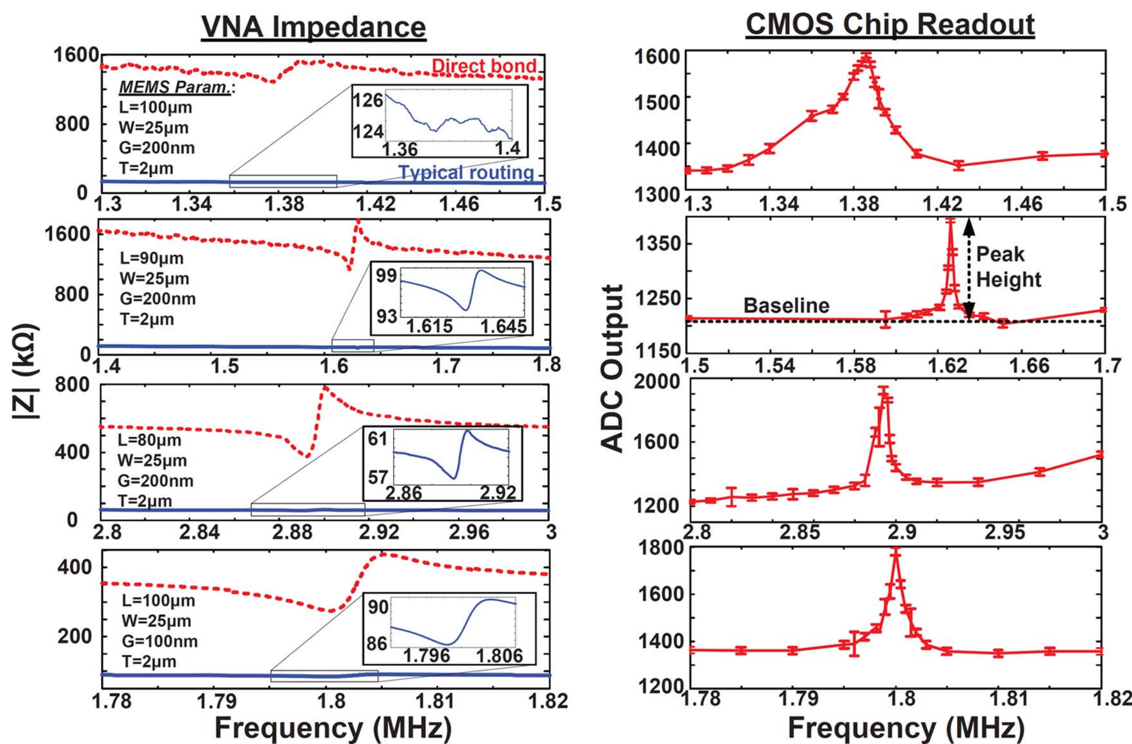


Fig. 20. VNA measurement and chip readout for four different MEMS bridges.

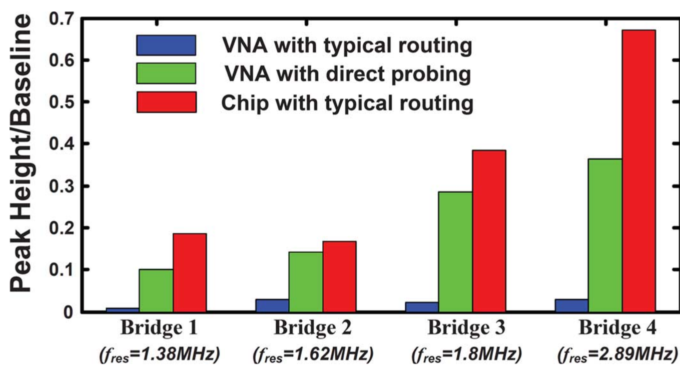


Fig. 21. Bargraph for resonant peak's detectability comparison among different readout approaches.

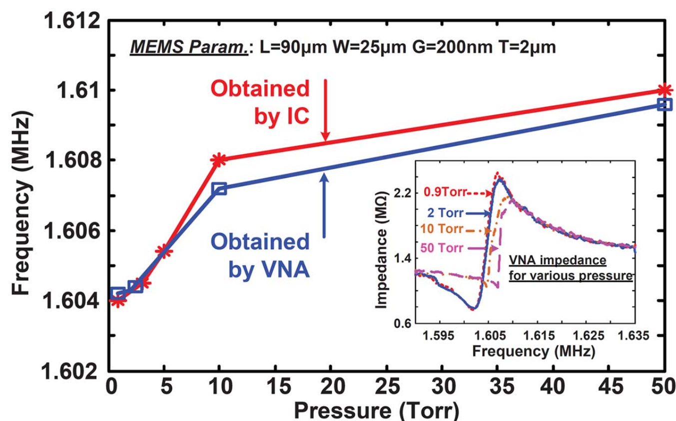


Fig. 22. Ambient environmental-pressure sensing as an application demonstration.

TABLE I
PERFORMANCE SUMMARY OF THE SYSTEM

CMOS Readout IC		
Power Consumption	Function Generator	2mA@3.6V
	G_m-C and ADC	700μA@1.2V
Resonator Frequency Range		1-4MHz
Frequency Resolution		<1kHz@2MHz
Input Voltage Noise*		$0.29\mu V_{rms}$
Detectable R_M (@Cp=1pF)		0.3-1.2MΩ
Readout Rate (2MHz Resonator)		500Hz
SNR		>20dB
MEMS Resonators (biased at 6V DC)		
Quality Factor		300~1000
Frequency Range		1.3-2.89MHz

*Obtained from distribution of ADC output code with highly stable inputs

are shown in Fig. 22. Good agreement is achieved, indicating proper peak detection by the IC with much greater SNR. Regarding application, we would like to point out that variation in the MEMS will indeed alter the absolute resonant frequency with respect to the pressure, thus an one-sample calibration is needed. Under our in-house manufacture condition, a 100 μm long, 1 μm thick bridge will present a shift of $\sim$0.08 MHz. The main parameter that affects the resonance frequency in our samples is the thickness of the structural layer. Commercial deposition systems will definitely be more homogeneous and this variation can be reduced. Finally, Table I provides a performance summary of the system.

VI. Conclusions

This paper focuses on an integration and readout strategy for thin-film MEMS resonators post processed on CMOS die. An important trend in the design of MEMS resonators is increasing the resonant frequency. Among other benefits, this mitigates the need for vacuum pressures, opening possibilities for a range of applications. However, higher frequencies exacerbate the effects of parasitics, particularly interface capacitances and parallel feed-through capacitances between the MEMS device electrodes. Considering the typical device parameters that can be achieved, these parasitics can make resonant behaviors undetectable at the target frequencies. To address the interface capacitances, this paper proposes the use of capacitive coupling across the chip-top passivation (formed using the CMOS top-layer metal and a metal plate deposited on the CMOS die). To address the parallel feed-through capacitances, this paper proposes a synchronous readout architecture, whereby the phase response is exploited to accentuate the resonant behavior. A CMOS prototype, fabricated in a 130 nm technology, is integrated with thin-film amorphous-silicon MEMS bridge resonators fabricated in-house on glass, enabling testing and characterization with multiple devices. While resonator peaks are only weakly detectable or undetectable electronically using a VNA, the prototype system enables readout of peaks with greater than 20 dB SNR in all cases.

Acknowledgment

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References

[1] J. Gaspar, V. Chu, and J. P. Conde, "Electrostatically actuated thin-film amorphous silicon microbridge resonators," *J. Appl. Phys.*, vol. 97, no. 9, pp. 094501–094501–11, Sep. 2005.

[2] N. Maluf and K. Williams, *An Introduction to Microelectromechanical Systems Engineering*. Boston, MA, USA: Artech House, 2004.

[3] G. Piazza, "MEMS resonators for frequency control and sensing applications," 2011 [Online]. Available: www.ifcs-eftf2011.org/sites/ifcs-eftf2011.org/files/editor-files/Slides_Piazza.pdf

[4] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T. King, "Thermal budget limits of quarter-micrometer foundry CMOS for post-processing MEMS devices," *IEEE Trans. Electron Dev.*, vol. 52, no. 9, pp. 2081–2086, Sep. 2005.

[5] A. Witvrouw, "The road to flexible MEMS integration," in *MRS Symp. Proc. 2008*, 2008, vol. 1075, pp. 1075–J05–01.

[6] M. Mehregany and C. A. Zorman, "SiC MEMS: opportunities and challenges for applications in harsh environments," *Thin Solid Films*, vol. 355–356, no. 1, pp. 518–524, Nov. 1999.

[7] S. Pourkamali, A. Hashimura, R. Abdolvand, G. K. Ho, A. Erbil, and F. Ayazi, "High-Q single crystal silicon HARPSS capacitive beam resonators with self-aligned sub-100-nm transduction gaps," *J. Microelectromechanical Syst.*, vol. 12, no. 4, pp. 487–496, Aug. 2003.

[8] A. Gualdino, V. Chu, and J. P. Conde, "Thin film amorphous silicon bulk-mode disk resonators fabricated on glass substrates," in *MRS Symp. Proc. 2011*, 2011, vol. 1299.

[9] G. B. Kromann, "Thermal modelling and experimental characteriztion of the C4/surface-mount-array interconnect technologies," in *Proc. 44th Electron. Components and Technol. Conf.*, 1994.

[10] P. A. Truitt, J. B. Hertzberg, C. C. Huang, K. L. Ekinci, and K. C. Schwab, "Efficient and sensitive capacitive readout of nanomechanical resonator arrays," *Nano Lett.*, vol. 7, no. 1, 2006.

[11] Y. Lin, S. Lee, S. Li, Y. Xie, Z. Ren, and C. T.-C. Nguyen, "Series-resonant VHF micromechanical resonator reference oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2477–2491, Dec. 2004.

[12] C. P. Wong, "High-performance silicone gel as integrated-circuit-device chip protection," *Polymeric Materials for Electronics Packaging and Interconnection*, vol. 407, pp. 220–229, Sep. 1989.

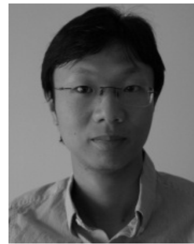
[13] M. Rocznik, F. Henrici, and R. Has, "ASIC for a resonant wireless pressure-sensing system for harsh environments achieving ± 2 % error between -40 and $150°$C using Q-based temperature compensation," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2012, pp. 202–203.

[14] S. Gierkink and E. V. Tuijl, "A coupled sawtooth oscillator combining low jitter with high control linearity," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 702–710, Jun. 2002.

[15] W. P. Chan *et al.*, "A monolithically integrated pressure/oxygen/temperature sensing soc for multimodality intracranial neuromonitoring," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2449–2461, Nov. 2014.

[16] N. Minh-Dung, H. Takahashi, T. Uchiyama, K. Matsumoto, and I. Shimoyama, "A barometric pressure sensor based on the air-gap scale effect in a cantilever," *Appl. Physics Lett.*, no. 130, pp. 143505–1–143505–4, Oct. 2013.

[17] X. Liu, Y. Zhu, M. W. Nomani, X. Wen, T. Hsia, and G. Koley, "A highly sensitive pressure sensor using a au-patterned polydimethylsiloxane membrane for biosensing applications," *J. Micromech. Microeng.*, vol. 23, no. 2, 2013.



Liechao Huang (S'12) received the B.S. degree in microelectronics from Fudan University, Shanghai, China, in 2010 and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012, where he is currently pursuing the Ph.D. degree.

His research interests include thin-film circuit design for power, radio and sensing interfaces, CMOS analog and mixed signal design for sensing interfaces and power management and hybrid system design combining thin-film circuits and CMOS ICs.

Mr. Huang is the recipient of a Princeton Fellowship and Gordon Wu award at Princeton University.

Warren S. A. Rieutort-Louis (S'12) received the B.A. (Hons.) and M.Eng. degrees in electrical and information engineering from Trinity College, Cambridge University, Cambridge, U.K., in 2009 and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012. He is currently pursuing the Ph.D. degree at Princeton University, where his research interests include thin-film materials, processes, devices and circuits for large-area electronic systems, as well as the development of hybrid thin-film/CMOS systems.

Mr. Rieutort-Louis is the recipient of an IBM PhD Fellowship, the Andlinger Center Maeder Fellowship in Energy and the Environment, the Princeton Harold W. Dodds Graduate Honorific Fellowship, and is a Graduate Teaching Fellow in the Princeton McGraw Center for Teaching and Learning.

Alexandra Gualdino received the Licenciatura degree in technological physics engineering from Instituto Superior Técnico, Lisbon, Portugal, in 2004. After one year working in academic research projects and venturing into the development of new consumer products for the paper industry for four years, she joined INESC-MN to research on the development of low-temperature thin-film microelectromechanical resonators. She received the Ph.D. degree from the Department of Materials Engineering of the Instituto Superior Técnico, Lisbon, Portugal, in 2014.

She is currently working in the Failure Analysis group at Pixtronix, a subsidiary of Qualcomm, developing a low-power display technology based on MEMS micro shutters.

Laura Teagno received the Master's degree in electronic engineering from the Polytechnic of Turin, Italy, in 2014. Her thesis topic was related to the research of sub-micron gaps thin-film amorphous silicon microelectromechanical resonators and was developed at INESC Microsystems and Nanotechnologies (INESC-MN), in Lisbon, in particular with the collaboration of the Thin-film MEMS group.

She is currently working at INESC-MN on the electronic detection of microelectromechanical resonators.

Yingzhe Hu (S'12) received the B.S. degrees in both physics and microelectronics from Peking University, Beijing, China, in 2009, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2011, where he is currently working towards the Ph.D. degree.

His research interests include thin-film circuit and CMOS IC hybrid sensing system design and analog and mixed-signal design for sensing applications.

Mr. Hu is the recipient of a 2013 Qualcomm Innovation Fellowship and Gordon Wu award at Princeton University.

João Mouro received the Master's degree in chemical engineering from the Instituto Superior Técnico, Lisbon, Portugal, in 2010. He is currently pursuing the Ph.D. degree in technological physics engineering at the Instituto Superior Técnico and is affiliated with the INESC-MN Research Center. His Ph.D. dissertation is on fabrication, characterization, modeling, and application of thin-film NEMS/MEMS. His current interests include design, fabrication, and modeling of thin-film MEMS resonators.

Josue Sanz-Robinson received the B.Eng. degree in electrical engineering (Hons.) from McGill University, Montreal, Canada, in 2010 and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2012. He is currently working towards the Ph.D. degree in electrical engineering at Princeton University. His research focuses on amorphous/nanocrystalline silicon rectifying diodes and sensors for flexible large-area electronic systems.

Mr. Sanz-Robinson is the recipient of a 2013 Qualcomm Innovation Fellowship.

James C. Sturm (S'81–M'85–SM'95–F'01) received the B.S.E. degree in electrical engineering and engineering physics from Princeton University, Princeton, NJ, USA, and the M.S.E.E. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 1981 and 1985, respectively.

He was with Intel Corporation as a Microprocessor Design Engineer as well as with Siemens, Munich, Germany. He has been with the Faculty of Princeton University since 1986, where he is currently a Professor of electrical engineering and PRISM Director. In 1994–1995, he was a von Humboldt Fellow at the Institüt Für Halbleitertechnik, University of Stuttgart, Germany. He has worked in the fields of silicon-based heterojunctions, 3-D integration, silicon-on-insulator, optical interconnects, TFT's, and organic light-emitting diodes. His current research interests include silicon-germanium–carbon and related heterojunctions on silicon, SOI, and 3-D integration, large-area electronics, flat-panel displays, organic semiconductors, and the nanotechnology-biology interface.

Prof. Sturm is a member of the American Physical Society and the Materials Research Society. Formerly, he was a National Science Foundation Presidential Young Investigator. He was the recipient of ten awards for teaching excellence from both Princeton University and the Keck Foundation and was the recipient of the President's Distinguished Teaching Award at Princeton in 2004. In 1996 and 1997 he was the Technical Program Chair and General Chair of the IEEE Device Research Conference, for which he is now a charter trustee. He served on the organizing committee of IEDM (1988–1992 and 1997–1999), having chaired both the Solid-State Device and Detectors/Sensors/Displays committees. In 2005, he was named the William and Edna Macaleer Professor of Engineering and Applied Science. He also has been a symposium organizer for the Materials Research Society and on the SOS/SOI, EMC, and several other conference committees. He was the organizing Chair for ISTDM 2006.

Sigurd Wagner (SM'78–F'00) received the Ph.D. degree from the University of Vienna, Vienna, Austria, in 1968.

Following a postdoctoral fellowship at Ohio State University, he worked from 1970 to 1978 with the Bell Telephone Laboratories on silicon memory and chalcopyrite semiconductor solar cells. From 1978 to 1980 he organized the Photovoltaic Research Branch of the Solar Energy Research Institute (now NREL) in Golden, CO, USA, as its founding Chief. Since 1980 he has been Professor of electrical engineering at Princeton. He introduces new electronic materials for flexible, conformably shaped and stretchable large-area displays, electronic wallpaper, electrotextiles, and electronic skin. His work ranges from the development of materials and flexible structures with fundamentally new functions to the design and fabrication of opto-electronic cells and, in collaboration with colleagues, their integration and application in systems.

Dr. Wagner is a Fellow of the American Physical Society, a corresponding member of the Austrian Academy of Science, was a Humboldt Senior Fellow in the Physics Department of the University of Konstanz, Germany, and has had research leaves at the Electrotechnical Laboratory in Ibaraki, Japan, at INESC Microsistemas e Nanotecnologias in Lisbon, Portugal, and at the Institute of Semiconductor and Solid State Physics of the University of Linz, Austria. He received the Nevill Mott Prize "for his groundbreaking research, both fundamental and applied, on amorphous semiconductors as well as chalcopyrites" in 2009, and in 2014 an ITC 10th Anniversary Prize "for his pioneering research on flexible and stretchable large-area electronics and comprehensive study on the mechanical behavior of the same, which will be applied to various products in the near future."

Virginia Chu (M'96–SM'08) received the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 1989.

Following her degree, she was a postdoctoral fellow at LPICM, Ecole Polytechnique, Palaiseau, France. Since 1990, she has been part of the Research Staff of INESC MN where she is a co-Director and co-responsible of the MEMS and BioMEMS research group. Her present research interests include thin film microelectromechanical systems (MEMS) for sensors and actuators, large area electronics and integration of thin film technology to biological applications.

João Pedro Conde received the Ph.D. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 1989. His thesis topic involved the study of the optoelectronic properties of amorphous silicon-silicon germanium multilayers.

Between 1989 and 1990 he was an IBM postdoctoral fellow at Yorktown Heights, NY, USA, where he developed a low-temperature process for the deposition of amorphous silicon, for which a patent was awarded. Since 1990 he has been at the Instituto Superior Tecnico, Lisbon, Portugal, where he is

presently a full Professor in the Department of Bioengineering. He is co-responsible for the Thin Film MEMS and BioMEMS research group of INESC Microsystems and Nanotechnologies. His current research interests include novel thin film devices such as thin film MEMS and sensors, low-temperature deposition of thin film semiconductors and electronic devices and micro- and nanotechnologies applied to Lab-on-a-Chip devices.

Naveen Verma (S'03–M'09) received the B.A.Sc. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2005 and 2009, respectively.

He is currently an Associate Professor of electrical engineering at Princeton University, Princeton, NJ, USA, where he has been since 2009. His research focuses on advanced sensing systems, including low-voltage digital logic and SRAMs, low-noise analog instrumentation and data-conversion, large-area sensing systems based on flexible electronics, and low-energy algorithms for embedded inference, especially for medical applications.

Prof. Verma was a recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, 2008 ISSCC Jack Kilby Paper Award, 2012 Alfred Rheinstein Junior Faculty Award, 2013 NSF CAREER Award, 2013 Intel Early Career Award, 2013 Walter C. Johnson Prize for Teaching Excellence, 2013 VLSI Symposium Best Student Paper Award, and 2014 AFOSR Young Investigator Award.