Screening of remote charge scattering sites from the oxide/silicon interface of strained Si two-dimensional electron gases by an intermediate tunable shielding electron layer

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(Received 17 April 2014; accepted 9 June 2014; published online 20 June 2014)

We report the strong screening of the remote charge scattering sites from the oxide/semiconductor interface of buried enhancement-mode undoped Si two-dimensional electron gases (2DEGs), by introducing a tunable shielding electron layer between the 2DEG and the scattering sites. When a high density of electrons in the buried silicon quantum well exists, the tunneling of electrons from the buried layer to the surface quantum well can lead to the formation of a nearly immobile surface electron layer. The screening of the remote charges at the interface by this newly formed surface electron layer results in an increase in the mobility of the buried 2DEG. Furthermore, a significant decrease in the minimum mobile electron density of the 2DEG occurs as well. Together, these effects can reduce the increased detrimental effect of interface charges as the setback distance for the 2DEG to the surface is reduced for improved lateral confinement by top gates. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4884650]

The silicon-based material system is attractive for the implementation of single-electron quantum dot (QD) devices for quantum computing applications, owing to the longer spin coherence time of electrons in silicon compared to that in III–V compounds.[1,2] Current research interests are focused on enhancement-mode quantum devices in undoped silicon two-dimensional electron gases (2DEGs) due to the absence of ionized dopants, which are possible sources of disorder and potential fluctuations in Si 2DEGs.[3–5] In an enhancement-mode structure, a strained-silicon quantum well (QW) which confines a 2DEG is buried below the surface to reduce the scattering from remote charges from the semiconductor surface. Therefore, a thick SiGe setback layer which separates the 2DEG away from the surface can lead to high electron mobility (μ) and low minimum two-dimensional electron density (n_{2D}).[6,7]

However, to pattern an undoped 2DEG into a QD, a thin SiGe setback layer is preferred to enable patterned top gates to precisely define the lateral extension of the 2DEG, which degrades the 2DEG transport properties. In this Letter, we present an improvement in 2DEG properties (higher mobility and lower minimum n_{2D}) in samples with thin SiGe setback layers (<40 nm) by introducing a tunable shielding electron layer near the surface. We believe that, at a critical electrical field, tunneling of electrons from the buried silicon QW to the surface triggers the formation of a barely mobile electron layer near the silicon surface. This surface electron layer can effectively screen the remote charge scattering sites, and thus dramatically improve both mobility and minimum n_{2D}.

The undoped Si/SiGe heterostructures in this study (Fig. 1) were grown by rapid thermal chemical vapor deposition (RTCVD) on top of a starting structure that consists of a relaxed $Si_{0.72}Ge_{0.28}$ buffer layer, which, in turn, was on top of a graded SiGe layer on a silicon (100) substrate. After growing another $Si_{0.72}Ge_{0.28}$ relaxed buffer layer (90 to 165-nm) on the top of this starting structure, an 11-nm strained silicon quantum well (buried QW) was then grown to hold the 2DEGs. Subsequently, a thin undoped $Si_{0.72}Ge_{0.28}$ setback layer (14, 20, or 40-nm) was grown, followed by a 4-nm strained silicon cap layer (surface QW) growth (5-nm for the 14-nm setback sample). The thin surface silicon layer is grown because we and others have found that a Si/insulator interface electrically behaves better than SiGe/insulator interface. The actual layer thicknesses may differ by +/−20%. To contact the buried 2DEG, phosphorus was first implanted in contact regions, followed by annealing at 600 °C. A 90-nm aluminum oxide layer was then deposited by atomic layer deposition as a gate insulator between contacts and the gate.

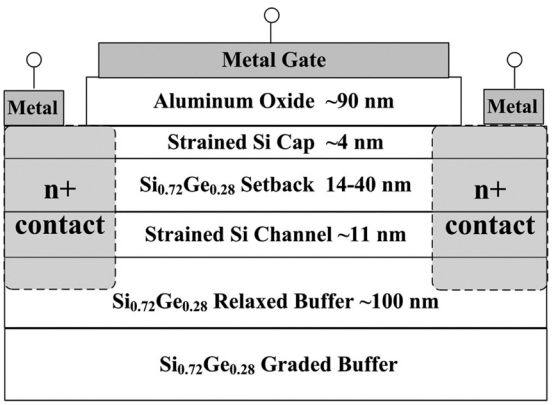

FIG. 1. The layer structure of a typical enhancement-mode undoped silicon 2DEG.

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A chrome/gold stack was finally evaporated on a sample to form both a Hall-bar-shaped gate and metal contacts on the implanted regions.

Hall measurements on the enhancement-mode silicon 2DEGs were all conducted at liquid helium temperature (4.2 K) with a magnetic field up to 2 T. The current source into the Hall bar is AC modulated with a low frequency (11 Hz). Four clear stages of the Hall electron density ($n_{2D,Hall}$) were observed in all samples as the gate voltage was ramped up. Fig. 2 shows data for the 14-nm SiGe setback sample as a characteristic example. When the gate voltage is above zero, but below a threshold voltage (V_T), which is ~2.9 V, the n_{2D} induced in the buried QW is low, leading to insulating behavior (referred to as Stage I) due to disorder and potential fluctuations, primarily from remote charges at the oxide/silicon interface.[8–11] Once the gate voltage supports an electron density above the critical density for the metal-insulator transition (MIT),[12] $3.5 \times 10^{11}\,cm^{-2}$ in this sample, electrons start to flow from the contacts into the buried QW to form a 2DEG (stage II). The experimental capacitance extracted from the linear dependence of the Hall electron density on gate voltages from 2.9 to 3.5 V in stage II is close to the expected value (~90%) based on a parallel-plate capacitor between the 2DEG and the gate (By $n_{2D,Hall}$ and μ_{Hall} in this paper, we mean those extracted from the measurements assuming a single transport layer, in this case, the buried silicon quantum well.).

With further increase in the positive gate bias, a sharp collapse of $n_{2D,Hall}$ was clearly observed in all samples when $n_{2D,Hall}$ reached $\sim 6.0 \times 10^{11}\,cm^{-2}$, dropping to $2.2 \times 10^{11}\,cm^{-2}$, much lower than the density originally required to initiate conduction. This new range is referred to as Stage III. With a 3–4 V further increase of gate voltage, $n_{2D,Hall}$ then increased only marginally ($<0.3 \times 10^{11}\,cm^{-2}$), while a simple $C \cdot \Delta V_G$ calculation would predict an increase of $n_{2D,Hall}$ of $\sim 10^{12}\,cm^{-2}$. In addition to the reduction in minimum n_{2D} in the sharp transition from stage II to stage III, the electron mobility is also dramatically enhanced (Fig. 5). Explaining these effects is the focus of this Letter; we hypothesize the effects are due to the formation of a tunable shielding electron layer at the semiconductor surface which screens the buried 2DEG from the scattering from remote charges at the oxide/silicon interface.

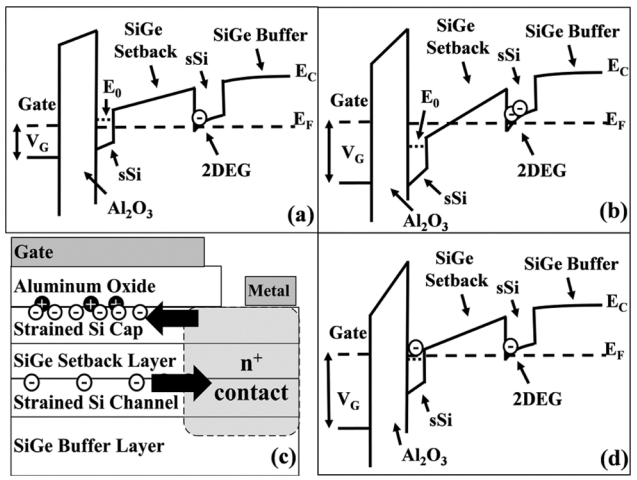

FIG. 3. Step-by-step description for the feedback process that brings the surface electron layer from non-thermal equilibrium to thermal equilibrium. (a) With a small gate bias, electrons accumulate in the buried QW first. (b) Even with a large gate bias, no electrons populate the surface QW due to a high critical density for MIT in that layer. (c) At higher gate voltage, electron tunneling from the buried QW towards the surface (not shown in Fig. 3(c)) raises the density above the metal insulator transition point, leading to a current flowing from the contacts into the surface layer. By Gauss's law, the buried electron density must be reduced as the surface density increases at a fixed gate voltage. (d) Electrons exist at both the surface and the buried QW, with the same Fermi level in both layers.

Since the buried QW (11 nm) is thicker than the surface QW (4–5 nm) in our structures, at flatband, the ground state (E_0) of surface silicon lies higher than the one in the buried QW. Therefore, as the gate voltage increases, E_0 of the buried QW drops to the Fermi level (E_F), defined by the contacts, before that for the surface layer, leading to the population of a buried 2DEG (Fig. 3(a)). As the gate voltage increases to induce higher density of mobile electrons in the buried QW, eventually E_0 of the surface QW will fall below E_F, so that electrons in the surface QW would be expected. With this assumption of thermal equilibrium with the contacts (both densities represented by a single Fermi level), once the surface electron layer forms (blue solid line in Fig. 4), a further increase in the gate voltage will lead to an increase only in the surface electron density ($n_{surface,Eq}$), and the electron density in the buried QW ($n_{buried,Eq}$) will

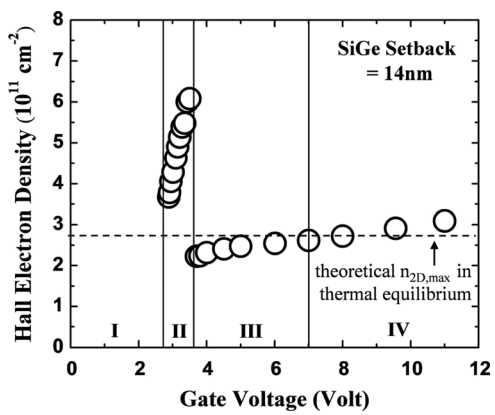

FIG. 2. Four-stage behavior in Hall electron density observed in all three samples (Data here are from the sample with 14-nm SiGe setback). The dashed line shows the theoretical $n_{2D,max}$ from the SCSP simulation.

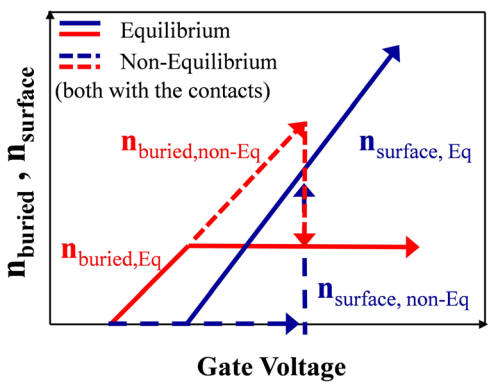

FIG. 4. The comparison of buried electron density (n_{buried}, red) and surface electron density ($n_{surface}$, blue) with increasing gate voltages in both thermal equilibrium with the contacts between two 2DEGs and non-thermal equilibrium. A sudden collapse in n_{buried} as the gate voltage increases and the corresponding increase in $n_{surface}$ bring the system back to thermal equilibrium.

remain fixed to first order (red solid line), because surface electrons will screen out the electrical field from the gate. However, the close proximity of many scattering charges at the oxide/silicon interface leads to a high critical density for the MIT of the surface layer. Thus, when $n_{surface,Eq}$ would be expected to be at a low value, it is impossible for electrons to flow laterally from the contacts into the surface QW. Furthermore, the low vertical electric field prevents electrons from tunneling from the buried QW to the surface layer. Thus, a surface layer cannot form, and the surface layer is not in thermal equilibrium with the contacts, with its ground state E_0 substantially below the contact Fermi level (Fig. 3(b)).[13] Therefore, as the gate voltage is raised, more electrons continue to accumulate in the buried QW, with the system continuing to exhibit Stage II behavior (dotted lines in Fig. 4) in a non-equilbrium condition.

We propose the sharp collapse in $n_{2D,Hall}$ with a further increase in gate voltage is triggered by electron tunneling, which initiates a positive feedback process. At an electron density of $6 \times 10^{11}\,cm^{-2}$ in all samples, corresponding to a critical electric field of $\sim 10^5$ V/cm if spurious charges are ignored, electrons begin to significantly tunnel through the thin SiGe setback layer into the surface. The surface density then reaches a point where some slow conduction laterally from the contacts into the surface layer occurs. This initial increase in density feeds back to cause an further increase in conductivity and thus more lateral flow, leading to the formation of a surface electron layer at its expected equilibrium density (Fig. 3(c)). As the surface layer forms at a fixed gate voltage, electrons must also flow out of the buried QW to obey Gauss's law (Fig. 3(d)). The simultaneous increase in $n_{surface,non-Eq}$ (blue dashed line in Fig. 4) and decrease in $n_{buried,non-Eq}$ (red dashed line in Fig. 4) brings the whole system back to thermal equilibrium (Stage III). Note that the time scale for the density collapse, namely the time scale for electrons to flow into the surface layer, could be on the order of 5 min—this is the approximate time between Hall measurements at each gate voltage. Beyond this point, in equilibrium, with more gate voltage, we expect an increase mostly in the surface density. Furthermore, if the surface mobility (and thus conductivity) was several orders of magnitude below that of the buried layer, a single-layer interpretation of the Hall measurements ($n_{2D,Hall}$ and μ_{Hall}) would continue to represent the properties of the buried layer.

To build confidence in our model, a self-consistent Schrodinger-Poisson (SCSP) simulation[14] was utilized to calculate the theoretical maximum n_{2D} in the buried quantum well at thermal equilibrium, which is the constant value that the red solid line in Fig. 4 represents at high gate voltage. For samples with 14-nm, 20-nm, and 40-nm SiGe setbacks, these values are $2.7 \times 10^{11}\,cm^{-2}$, $2.9 \times 10^{11}\,cm^{-2}$, and $1.9 \times 10^{11}\,cm^{-2}$, respectively. The $n_{2D,Hall}$ values (representing the buried layer) measured near the end of stage II ($\sim 6.0 \times 10^{11}\,cm^{-2}$) were much higher than these values, implying that the surface layer was indeed not in equilibrium at the end of Stage II when the collapse occurs. Furthermore, note the experimental values just after the stage II/stage III (equilibrium/non-equilibrium) transition were $2.5 \times 10^{11}\,cm^{-2}$, $2.4 \times 10^{11}\,cm^{-2}$, and $1.7 \times 10^{11}\,cm^{-2}$ for three samples, respectively, all in close agreement with the predictions (Fig. 5). Both results support our model that the Stage II/III collapse is a switch of the surface layer from non-equilibrium to equilibrium.

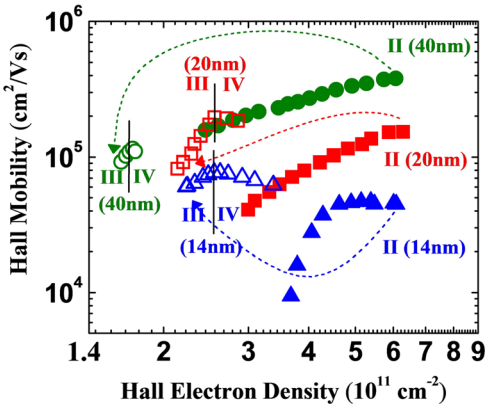

FIG. 5. The dependence of Hall mobility on Hall electron density measured at 4.2 K for all three samples with different stages labeled. The gate voltage steps for data points at stage II and stage III/IV are 0.03–0.15 Volt/0.1–2 Volt, respectively, for all three samples. The measurement sequence is indicated by dashed lines (from stage II to stage III).

We now discuss the transport properties, and show the dependence of the Hall mobility on the Hall electron density (Fig. 5). For each sample, two sets of point are shown: closed symbols before the transition and open symbols after it. With no surface layer in Stage II, the mobility of each sample increases with density due to the usual self-screening. Because the mobility at a given density increased (and the minimum density decreased) as the separation between the semiconductor/insulator interface and the buried 2DEG increased, it seems clear that the main scattering sites are at the surface (or inside the insulator).[15] When the system switches back to thermal equilibrium, the new intermediate electron layer near the surface separates the buried 2DEG and the scattering sites, resulting in a strong screening effect on both the minimum n_{2D} and electron mobility of the buried layer. In all samples, after the transition, the samples now conduct well at densities only 60%–70% of their previous minimum densities (Fig. 6(a)). Note the small range of Hall electron densities in Stage III despite an increase of gate voltage of several volts; this is because the new charges go mostly into the surface layer and not the buried layer. Beyond the density reduction, the screening effect enhances the electron mobility of the buried layer as well (Fig. 5). In stage II, the highest electron mobility obtained from samples with 14-nm, 20-nm, and 40-nm SiGe setbacks are 47 000 cm^2/Vs, 153 000 cm^2/Vs, and 381 000 cm^2/Vs at high

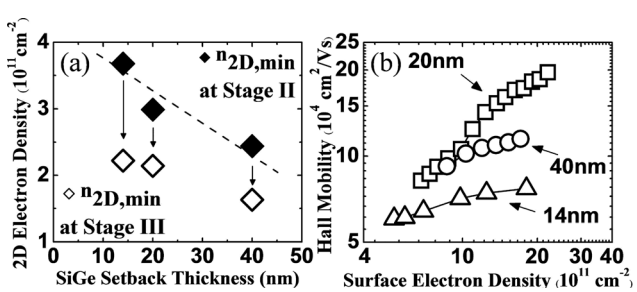

FIG. 6. (a) The reduction in minimum n_{2D} due to the screening effect by the surface electron layer. (b) The increasing surface electron density screens the scattering from remote charges to enhance the buried electron mobility.

densities ($\sim 6.0 \times 10^{11}\,cm^{-2}$), respectively, with the 20-nm setback sample requiring a density of $\sim 5 \times 10^{11}\,cm^{-2}$ to reach a mobility of 100 000 cm^2/Vs. After the transition, both the 14-nm and 20-nm setback samples achieve a mobility at or near $100\,000\,cm^2/Vs$ at a density of only $\sim 2.3 \times 10^{11}\,cm^{-2}$, and the 40-nm setback sample achieves this benchmark at a density of only $1.6 \times 10^{11}\,cm^{-2}$. The 20-nm setback sample reaches $196\,000\,cm^2/Vs$ at only $2.6 \times 10^{11}\,cm^{-2}$. These densities are well below the metal-insulator transition level for each of the three samples before the transition. To emphasize the importance of surface electron layer on the mobility enhancement in stage III, the relation between $n_{surface}$ and Hall mobility for all three samples are shown in Fig. 6(b). Here, the tunable $n_{surface}$ was calculated by starting with the change in electron density in the buried layer at the collapse voltage (adjusted for the slightly different gate capacitance), and then scaling the value up by $C_{ox} \cdot \Delta V_G$ from that point. In stage III, the increase in gate voltage (2–3 Volts) results in a considerable increase in the $n_{surface}$ from around $4.0 \times 10^{11}\,cm^{-2}$ to over $1.0 \times 10^{12}\,cm^{-2}$, but only a marginal increase in n_{buried} ($<1.0 \times 10^{11}\,cm^{-2}$). This increases our confidence in attributing the enhancement in buried layer mobility to the strong screening by the surface electron layer.

Finally, we note that if we keep ramping up the bias in the equilibrium mode, a decrease in Hall mobility is eventually seen in all samples (Stage IV in Fig. 5). The increasing surface electron density leads to higher surface electron mobility, so that eventually the conductance in the surface layer becomes significant compared to that in the buried electron layer. Through a parallel conduction model, the decreasing measured total Hall mobility with increasing electron density (Fig. 5) in stage IV reflects the existence of two parallel conduction paths with a lower mobility of the surface (because it is adjacent to the scattering sites) compared to that in the buried QW.[16]

To summarize, we observed a rapid collapse in the density of a buried Si 2DEG in an enhancement-mode structure above a critical gate voltage. A large improvement in the 2DEG transport properties, including a significant reduction in minimum n_{2D} and enhancement of electron mobility, was achieved simultaneously. The process is attributed to the formation of an intermediate electron layer near the surface which screens the buried layer from the remote charges at the oxide/silicon interface. This screening effect may mitigate concerns about remote charges in a shallow two-dimensional electron system and may provide a better platform for the realization of single-electron quantum devices in the silicon-based material system.

This work at Princeton University was sponsored by United States Department of Defense through DARPA, and by the NSF MRSEC program (DMR-0819860). The views and conclusions contained in this document are those of the authors and should not be interpreted as representing the official policies, either expressly or implied, of the U.S. Government. We also thank D. C. Tsui for helpful discussions and Amberwave Semiconductor for supplying the relaxed $Si_{0.72}Ge_{0.28}$ buffers.

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