Effect of Low-Temperature TFT Processing on Power Delivery from Thin-Film Power Electronics on Flexible Substrates

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Abstract

We have recently shown thin-film systems combining energy-harvesting devices possible in large-area electronics with embedded power electronics based on thin-film transistors (TFTs), creating complete powering systems. Power inverters are built to perform DC to AC conversion from large thin-film solar cells, enabling substantial wireless power delivery to mobile load devices or to other physical “planes” (layers) in a large-scale thin-film system. To realize non-rigid planes, we use low-temperature amorphous-silicon (a-Si) processing for TFTs in the power circuits [1]. We previously illustrated how TFT characteristics (e.g. ft) impact performance of these systems; in this paper we show how provision of output power is affected by stability of TFTs in the thin-film circuits and how degradation can be mitigated.

Results are presented for a TFT LC-oscillator-based inverter [1,2], drawing DC power from an a-Si solar module (Vop≈35V) and transmitting this through near-field inductive coupling to load devices. The oscillator is two cross-coupled, SiNx-passivated, back-channel-etched TFTs (W/L=3600/6μm) with planar Cu inductors (10cm^2, L=150 μH, R=35Ω) forming tanks at TFT drains; the inductors resonate with the TFT capacitances (Ct≈30pF) enabling wireless power transfer(>20mW). We fabricate our inverters on free-standing 50 μm polyimide at process temperatures <180C.

We show that output power decrease over time results from TFT instability, caused by threshold-voltage shift. For Vop<35V and a SiNx TFT dielectric, this is from moderate gate field (on average <10^6 V/cm) Vt shift [3] of oscillator TFTs of the form t^β with β=0.40 (previously associated with defect creation at the a-Si-dielectric interface). The oscillator stress conditions are complex, as large AC swings at TFT drain/gate nodes result in devices moving between linear/saturation regimes, with biasing voltages oscillating about a non-zero average, Vop. DC stressing in 3 regimes (Vds>Vgs, Vds<Vgs and Vds=Vgs) suggests Vt shift mainly occurs while TFTs are in saturation. After 3 hours, average oscillator current drops by 25% resulting in 17% decrease in power delivery from reduced TFT gm, lowering oscillator voltage swing.

This gm reduction also affects the oscillator’s required positive feedback condition, (gm/Ct)x(L/R)>1 [2]. We show that large L/R ratio inductors, achievable by large-area patterning, make the power-inverter less sensitive to long-term TFT drift. Raising gate nitride deposition temperature can improve the dielectric-channel interface, reduce Vt shift [3] and maintain gm. At higher temperatures, however, larger misalignments result between device layers, requiring larger source/drain overlaps to maintain successful operation (hence larger Ct). We show experimental data for this tradeoff, noting that larger Ct affects the positive feedback condition, output power and power-transfer efficiency.

1. Rieutort-Louis et al. IEDM 2012

2. Hu et al. CICC 2012

3. Kattamis et al. EDL 2007