Amorphous Silicon: The other Silicon

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1. Abstract

While crystalline silicon FET's are the key enablers for the integrated circuit field, amorphous silicon thin film transistors are the key semiconductor of the large-area electronics field, also known as "macroelectronics."   This talk reviews the basic properties of amorphous silicon, and then outlines research trends, driven in large part by new applications. These trends include increased performance, increased stability for analog and high duty cycle applications, flexible substrates for products with new form factors, printing for cost reduction, and crystalline silicon-amorphous silicon interfaces for high performance solar cells.

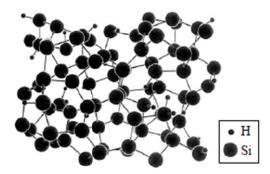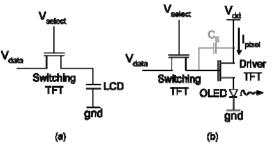## 2. Introduction to Amorphous Silicon

Fig. 1. *Structure of hydrogenated amorphous silicon [2].*

Amorphous silicon (a-Si) was first intensively investigated in the 1970's [1]. a-Si is used in devices typically deposited by plasma-enhanced chemical vapor deposition from silane at ~300 $^{\circ}$C. Although a-Si has no long range order like a crystal, in device-grade a-Si *most* silicon atoms still have bonds to four neighboring silicon atoms (Fig. 1).   Surprisingly, these bonds have a bond length and an angle between bonds *close to* those in crystalline silicon, despite the lack of long range order. The words "most" and "close to" are important. About 10% of the silicon orbitals do not form bonds with other silicon atoms, but nearly all of these form bonds to atomic hydrogen, which reduces the density of residual dangling bonds and states in the band gap to ~10^{16} cm^{-3}. Because the material contains on the order of ~10% hydrogen, it is often referred to as "hydrogenated amorphous silicon," a-Si:H.   Second, because the bond lengths and angles are not all ideal, many of the bonds are strained. As a result, the edges of the conduction and valence band are not sharp, and the states at the edges of the conduction and valence bands closest to midgap are not conventional conducting states, but rather localized states.
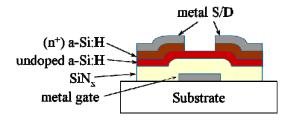
3. TFT and AMLCD Application

Fig. 2. *Pixel circuits for (a) active matrix liquid crystal display and (b) active matrix organic light emitting diode (AMOLED) display.*

The main driver of amorphous silicon to date has been its role as the switch to control pixel addressing in Active Matrix Liquid Crystal displays (Fig. 2(a)). The rows in the display (select lines) are scanned sequentially while the data for each pixel in a row is provided by the vertical data columns.

In contrast to VLSI devices, the TFT is constructed with the gate on the bottom, as the PECVD SiN$_x$/a-Si:H interface with the gate insulator on the bottom has better

interface properties in general than the device on top for PECVD processes in the 300 ^{o}C range. In the conventional structure the source/drains are not self-aligned to the gate (Fig. 3). The glass substrate combined with the TFT's and row and column metal lines is known as the "backplane" of the display. Due to its relative process complexity compared to that of the liquid crystal, the backplane is a dominant component of the cost of displays. Typical TFT channel lengths are several microns, not scaled shorter in practice by the need to keep process costs low. The typical n-channel field-effect mobility is 0.5 - 1.0 cm^2/Vs, which is sufficient for TFT use as a switch to charge the liquid crystal capacitor.

Fig. 3. *Typical a-Si:H TFT cross section. For AMLCD production, the substrate is glass.*

As the AMLCDs have come to dominate the flat panel display market, the size of the industry has grown to ~$75B/yr, roughly 1/3 the size of the conventional semiconductor/integrated circuit industry (Fig. 4). Future growth will depend in large part on technical innovation with respect to the backplane, TFT's, and the properties of the a-Si:H itself. Future directions of innovation include higher performance and stability, flexible substrates, printing for lower cost, and heterojunctions with crystalline silicon.
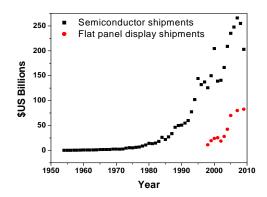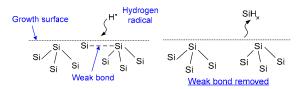

Fig. 4. *Annual market size of flat panel display and conventional semiconductor/IC industries [3].*

4. Performance and Stability

In most displays to date, the scanner circuits for the row and column lines are off-chip (conventional IC's),

requiring many wire connections to be made between external driving circuitry and the display. Integrating such circuits onto the display [4] can reduce cost. While possible in some cases, this is difficult because of the low n-channel mobility. Because of the large number of non-conducting "tail" states above the valence band edge of a-Si:H, the hole mobility is only ~0.01 cm^2/Vs, making CMOS impractical. Furthermore, the low-temperature gate dielectric traps carriers, and the a-Si itself degrades with time, so that threshold voltages increase rapidly. These can be tolerated in the AMLCD circuit of Fig. 2(a), because the TFT operates only in digital mode and is on for only 0.1% duty cycle.

One approach towards increased performance, while retaining the production advantages of a ~300 ^{o}C maximum process temperature, is to add hydrogen to the a-Si:H deposition. Schematically, atomic H can break weak Si-Si bonds (Fig. 5). Weakly-bonded Si can then combine with H to form volatile SiH$_x$ – in this way "weak-tissue" can be dynamically removed from the solid *in situ* during the PECVD process.
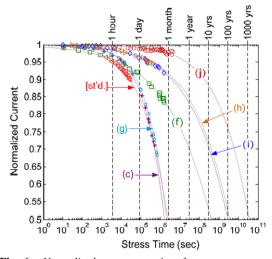

Fig. 5. *Simplified schematic description of how the addition of hydrogen to the PECVD process can improve the quality of a-Si:H.*

By adjusting the PECVD process, it is then possible that as the film grows, nano-sized nuclei of crystalline silicon may form within the amorphous matrix, or that vapour-phase epitaxial growth occurs on top of the crystalline nuclei to form "nanocrystalline" silicon [5,6]. Because the nanocrystalline material is on the top of the film, to take advantage of its higher mobility, top-gate structures are required. N-channel mobilities in excess of 100 cm^2/Vs have been reported [7] along with high p-channel mobilities [8].

Top gate structures are still limited by two issues – the a-Si:H/insulator interface is poor and the deposited SiO$_x$ insulator (commonly used on top gate devices) is leaky for the low deposition temperatures. Further, integration of the top-gate structure into a production process is difficult in practice without the ability to use ion shower/annealing technology for doping n$^+$ or p$^+$ regions, because of the low process temperature. Therefore it is attractive to look at new insulators for bottom-gate processes. For example, a novel insulator has been formed using PECVD from a mixture of hexamethyl disiloxane (HMDSO) and oxygen at room temperature. The material is a hybrid between SiO$_2$ and plasma-polymerized HMDSO. With the novel insulator

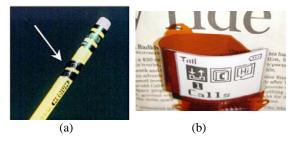and the conventional a-Si:H process of Fig. 3, n-channel mobilities of ~ 2 cm^2/Vs have been reported [9].

Organic LED's are an emerging display technology, but they require a driver transistor to supply current. This driver must operate in DC, and because it translates the programming voltage to the LED current, it operates in analog mode, requiring exceptional threshold stability. Under gate biases relevant for driving OLED's, the drive current of a typical a-Si:H TFT would degrade by 50% (leading to a 50% brightness reduction) in only 1 month in DC operation. The dominant mechanism for the degradation is the formation of defects in the a-Si (breaking of weak Si-Si bonds) and subsequent trapping of electrons in defects, which raises the threshold voltage. This process is actually driven by the electrons in the channel itself. Using PECVD processes based on the mechanism of Fig. 5, the extrapolated TFT DC lifetime has been increased by 10^4 to 1000 years [10, 11]. While further work is needed to enable accelerated tests, such a dramatic improvement in stability could also be important for digital scanning circuits.

Fig. 6. *Normalized current vs. time for room temperature operation of a-Si:H TFT's under ~7.5V gate bias, normalized to its initial value, for a "standard" and experimental processes with improved a-Si:H and improved SiN$_x$. Process conditions are described in Ref.'s 10 and 11.*

5. Flexibility and Deformability

Future products such as flexible displays, wearable electronics embedded with sensors, and unbreakable "electronic sensor wallpaper" requires that the glass substrates be replaced with plastic or even metal foil substrates. For cost reasons, it is desirable that the TFT's be fabricated directly on the thin foils, in contrast to first fabricated on rigid substrates and then transferred to flexible substrates. To first order, as long as the substrates are thin, the strain induced in the TFT's when the structured are cylindrically deformed (e.g. rolled) is small. Because the TFT's can withstand a

strain on the order of ~0.5% before mechanical failure, radii of a few mm can be achieved (Fig. 7(a)).

(a) (b)

Fig. 7. *(a) a-Si:H TFT on steel foil substrate cylindrically deformed around a pencil [12], and (b) active matrix electrophoretic ink display demo using a-Si:H TFT's on a steel foil backplane[13].*

Besides mechanical issues of bending, plastic foils pose process challenges – the common clear plastic polyethylene napthalate (PEN) has a maximum process temperature of ~200 ^{o}C, and is prone to dimensional changes during processing. In practice the low temperature is more of a problem for the dielectric quality than the a-Si:H itself. There is much innovative work in progress, and flexible products may be on the market in the near future, perhaps similar to the active matrix electrophoretic ink (E-ink) demonstration of Fig. 7(b).

6. Cost Reduction and Printing

VLSI technology has reduced the cost per transistor over time by scaling down the feature sizes. For applications, smaller is generally better. In contrast, for "large-area" electronics, such as flat panel displays, solar cells, etc., the large area is a key feature of the product, and shrinking is not allowed. Therefore cost per unit area has become a key metric, rather than cost per transistor. The reduction of cost/area to date has been accomplished largely by scaling up the size of the glass substrates -- in advanced production glass plates ~3m x 3m are used. However, the process still resembles a typical "IC-like" process with photolithography, optical exposure, etching, etc.

One technology option for future cost reduction are "printing-like" steps which eliminate photolithography. For example, one can first deposit the entire device/interconnect stack, followed by a soft polymer which can be "imprinted" using a multi-level mold (Fig. 8). By an appropriate subsequent set of process steps, the different levels in the resist can each be used to define a different level in the device structure.

This approach has the great advantage that if the substrate changes dimension during the fabrication steps, the different device layers remain in registration because they were defined from a single imprint step. This would not be the case of course if each layer
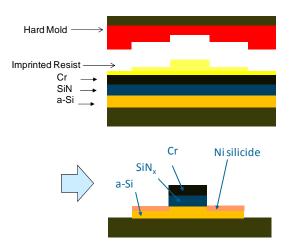
Fig. 8. *Self-aligned imprint lithography (SAIL) approach towards fabricating a top-gate a-Si TFT, based on a single imprint step to define the pattern of all layers [16].*

required its own lithography step and alignment. Thus the process has been named "Self-Aligned Imprint Lithography" (SAIL) [14]. SAIL has been demonstrated on a roll to roll (R2R) basis for bottom gate a-Si TFT's [15] and a small scale level for top gate TFT's [16]. The top gate TFT structure includes the use of novel metal source drains which are self-aligned to the gate [17], allowing one to avoid the need for n$^+$ layers.

7. Photovoltaics: x-Si/a-Si heterojunctions

Solar cells made from p-n junctions in a-Si:H and a-SiGe:H have been in production for some time, but their power efficiency in production has been limited to the 7% range. On the other hand, crystalline silicon (x-Si) solar cells can reach efficiencies of ~25%, but require high temperature diffusion steps, which could be a major cost component. a-Si:H has a bandgap of ~1.8 eV, substantially larger than the 1.1 eV of crystalline silicon. Thus one can consider replacing the diffused p-n junctions in crystalline silicon with a deposited a-Si:H heterojunction contact to the crystalline silicon. The absorption occurs in the crystalline silicon, and the large a-Si:H bandgaps can help reduce the minority carrier recombination at contacts, increasing the open circuit voltage. While the idea of a heterojunction is straightforward, in practice it requires careful attention to the interface, so that a low density of recombination sites on the crystalline silicon surface is achieved [18]. Recently, this approach of x-Si/a-Si heterojunctions has been used to create hybrid Heterojunction with Intrinsic Thin layer (HIT) a-Si:H/x-Si solar cells with remarkable efficiencies of ~23% [19].

8. Conclusion

TFT's with the semiconductor hydrogenated amorphous silicon have been the key electronic technology enabling the rapid growth of flat panel electronics. Advances in material and interface characteristics, process innovation and device structures, flexibility, and cost reduction will enable new applications from photovoltaics to wearable electronics and structural health monitors. It is not unreasonable to think that in another generation the market size for "macroelectronics" could be larger than that for conventional microelectronics.

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