Amorphous Silicon Thin-Film Transistors with DC Saturation Current Half-Life of More than 100 Years

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Abstract

We report amorphous silicon thin film transistors (a-Si TFT's) with an extrapolated DC saturation current half-life of more than 100 years, an improvement of over 1000 times compared to the previous art (1-4). This TFT half-life is higher than the luminance half-life of high-quality green phosphorescent OLED's, showing that the TFT's are promising for driving OLED's in active-matrix OLED displays.

Introduction

Commercial introduction of active-matrix OLED (AMOLED) displays requires low-cost and highly stable TFT's for driving OLED's. Amorphous Silicon (a-Si) technology is currently in widespread production of TFT backplanes for active-matrix LCD's and is a cost-effective technology which may be transferred to flexible plastic substrates (5). In AMLCD's, the TFT is used as a digital switch driven with duty cycles of only ~0.1%, making the circuit fairly insensitive to the conventionally large threshold voltage shifts of a-Si TFT's. In contrast, the driver TFT in an AMOLED pixel operates in DC, so that the OLED current depends directly and continuously on the TFT threshold voltage (5). An increase in the threshold voltage of the driver TFT's over time reduces the OLED drive current and therefore decreases the brightness of the pixel. The OLED half-life is conventionally defined as the time for the OLED luminance to drop to 50% of its initial value under constant current bias and is currently ~250,000 hours (~30 years) for high quality green phosphorescent OLED's (6). Defining the DC saturation current half-life of the TFT as the time for the TFT drain current to fall by 50% under DC voltage bias in saturation, the half-life of typical a-Si TFT's is lower than ~1 month (7), far lower than that of the OLED's. Thus conventional thinking has been that a-Si TFT's were too unstable for AMOLED displays and thus more expensive poly-Si technology was required.

Experimental Procedure

A. Sample Preparation

Standard a-Si TFT's were fabricated with either back-channel etched (BCE) or back-channel passivated (BCP) structures (Fig. 1). The BCP structure passivates the back-side of the TFT channel "in situ" at the cost of an extra mask step. The gate nitride and a-Si were grown in a standard PECVD growth system. The gate nitride was grown from a mixture of silane and ammonia at a chamber pressure of 500mtorr and plasma power density of 17mW/cm^2 and at temperatures from 200 to 350°C. Amorphous Si was grown either from pure silane ("standard" a-Si) at 500mtorr or a mixture of silane and hydrogen ("improved" a-Si) at 900mtorr, both at a plasma power density of 17mW/cm^2. The a-Si growth temperature was 200°C for TFT's with the gate nitride grown at 200°C, and 250°C for the gate nitride grown at 250°C and above. For BCP devices, the passivation nitride was grown at 250°C under the same conditions as the gate nitride.

B. Stress Measurements

Measurements at high gate stress fields (10^6 V/cm or above, i.e. gate voltages of 30V or above on the 300nm-thick gate nitride) were performed by grounding the drain and source of the TFT and applying a voltage to the gate. The threshold voltage shift was found from the difference of the threshold voltages extracted from the TFT characteristics before and after applying the stress. Low-field measurements (gate stress fields of 2×10^5 V/cm or below, corresponding to gate voltages of 7.5V or below) were performed by biasing the TFT's in saturation at constant gate voltages (and drain voltages of 12V). The threshold voltage shift was calculated by measuring the drop in the saturation current over time assuming negligible shift in TFT mobility (as verified experimentally and known from previous work (1-4)). This type of low-field measurement is consistent with the realistic TFT operating conditions in AMOLED pixels and also allows us to measure

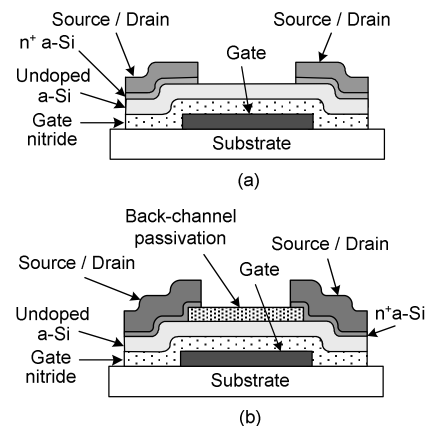

Fig. 1. Schematic cross-section of (a) back-channel etched (BCE) and (b) back-channel passivated (BCP) standard TFT structures.

smaller threshold voltage shifts which could not be extracted accurately from the small drift in TFT characteristics.

Results and Discussion

A. Degradation Mechanisms

Mechanisms responsible for the threshold voltage shift in a-Si TFT's are (i) the trapping of electrons in the gate nitride and (ii) creation of defects in a-Si at or near the a-Si/nitride interface (1). In the first mechanism, channel electrons tunnel into the empty trap states in the nitride (Fig. 2a) resulting in a logarithmic shift of the threshold voltage (1, 2) (Eqn. in Fig. 2a). In the second mechanism, weak Si-Si bonds break in the presence of excess electrons and create negatively charged dangling bonds (Fig. 2b). This process results in a stretched exponential shift of the threshold voltage which may be approximated by a power law at relatively short stress times (compared to a time scale of the order of 1 year) (1-3, 8) (Eqn. in Fig. 2b).

The threshold voltage shifts of a-Si TFT's with gate nitrides grown at different temperatures and standard a-Si channel material are plotted vs. time in Fig. 3 for different gate stress fields. At very high gate stress fields (3×10^6V/cm i.e. 90V on the gate) the extracted value of 1.2 for the λ parameter of the logarithmic charge trapping model (Fig. 2a) is close to the theoretical value of ~1 expected from the classical model of electron tunneling into the insulator traps (9) as noted in (1, 2). The improvement of high-field TFT stability achieved by increasing the gate nitride growth temperature results from a higher nitride quality and therefore less electron trapping (10).

At low stress fields (2×10^5V/cm i.e. 7.5V on the gate) the extracted value of 4.8 for the λ parameter of the logarithmic charge trapping model (Fig. 2a) is much larger than accepted for electron trapping in the insulator. This shows that at low gate stress fields, the threshold voltage shift is faster than can be explained by trapping in the gate nitride. However, the

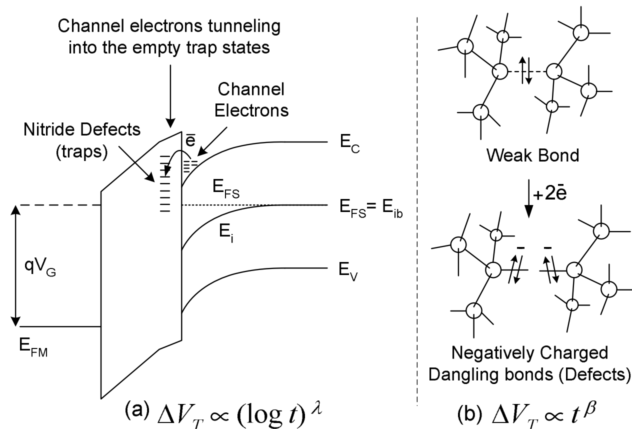

Fig. 2. Instability mechanisms in a-Si TFTs (a) charge trapping in gate SiN_x and (b) defect creation in a-Si near the a-Si/SiN_x interface.

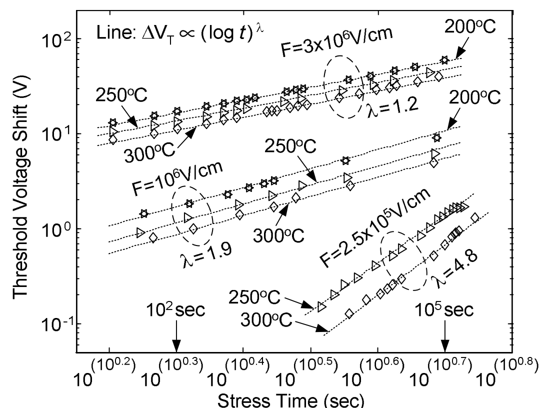

Fig. 3. Time dependence of the threshold voltage shift at different gate stress fields for a-Si TFT's fabricated with different gate nitride deposition temperatures and linear fits based on the logarithmic time dependence (Fig. 2a). All TFT's have BCE structures and standard a-Si channels.

low-field data precisely fits a power law model (Eqn. in Fig. 2b) with β=0.44, consistent with the literature (1-4, 8) indicating that creation of defects in a-Si at or near the interface is the dominant instability mechanism at low fields (Fig. 4). Interestingly, the low-field stability is also improved by increasing the gate nitride deposition temperature. Since a-Si is deposited after the gate nitride, this means that defect creation in a-Si is not occurring in the bulk of a-Si, but rather very near the nitride, where the a-Si microstructure may be affected by that of the nitride underneath it.

B. TFT Stability for Driving OLED's

The stability of a-Si TFT's is typically measured at high gate stress fields (over 1 MV/cm) because high voltages are used in AMLCD's and to accelerate the testing. However, operation at lower voltages is required in AMOLED displays for low power. With high-quality green phosphorescent OLED's, for a pixel size of 100μm×100μm and a driver TFT with a W/L of ~1 and a threshold voltage of ~2.5V, a gate voltage of only

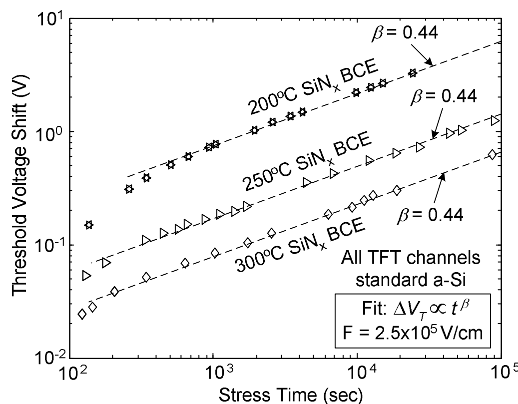

Fig. 4. Time dependence of the low-field a-Si TFT threshold voltage shift for three different gate nitride growth temperatures. All TFT's have BCE structures and standard a-Si channels.

~7.5 V (2.5×10^5 V/cm on a 300nm-thick gate nitride) is sufficient to drive the pixel at a luminance of $1000 Cd/m^2$ (200nA or $2mA/cm^2$ on the OLED), well above the minimum requirements for display brightness (5).

The low-field threshold voltage shift of conventional a-Si TFT's reported in the literature along with the low-field data from our lab are plotted in Fig. 5. Because of the different bias stress conditions, and since the threshold voltage shift induced by defect creation (low gate field regime) is proportional to the accumulation charge in the TFT channel (1-3) , the threshold voltage shift reported by other groups has been scaled by the ratio of the accumulation charge per unit area of the channel at their bias stress conditions (Q_{ch}) to that of ours ($Q_{ch,\,PU}$) for a fair comparison (3) (C_{ins} is the gate dielectric capacitance per unit area of the channel, V_{T0} is the initial threshold voltage and the subscript PU refers to our TFT's).

$$\Delta V_{T,\,scaled} = \Delta V_T \times \frac{Q_{ch,\,PU}}{Q_{ch}} = \Delta V_T \times \frac{(2/3)\,C_{ins,\,PU}\,(V_{GS,\,PU} - V_{T0,\,PU})}{C_{ins}\,(V_{GS} - V_{T0})} \qquad (1)$$

The coefficient of 2/3 accounts for the lower accumulation charge in the saturation regime (where our TFT's were stressed) compared to the linear regime (3). The low-field condition for scaling was chosen because it is the one appropriate to the bias condition as mentioned above. As seen in Fig. 5, an extrapolated ~1.2V shift in DC (corresponding to a 50% drop in current) occurs at times under 1 month, showing that the conventional a-Si TFT's are too unstable for driving

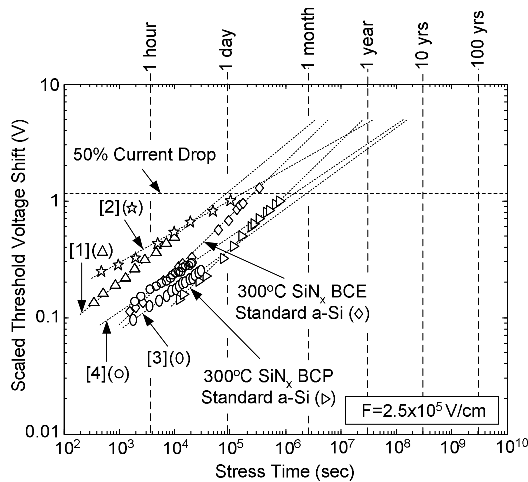

Fig. 5. Low-field (2.5×10^5 V/cm i.e. V_{GS} = 7.5V) threshold voltage shift of conventional a-Si TFT's fabricated in our lab or reported in the literature scaled to our stress conditions based on Eqn. (1). The TFT parameters are, Ref. (1): "BCE" structure, V_{GS}= 20V, V_{T0}=2.5V, insulator: SiN_x 500nm, Ref. (2): "BCP" structure, V_{GS} = 25V, V_{T0} =4.5V, insulator: SiO_x 300nm+SiN_x 50nm, Ref. (3): "BCP" structure, V_{GS} = 8V, V_{T0} =1.3V, insulator: SiN_x, 300nm, Ref. (4): "BCP" structure, V_{GS}= 15V, V_{T0} =2.7V, insulator: SiN_x, 200nm. Relative dielectric constants of 7.5 and 3.9 were assumed for all nitride and oxide insulators, respectively.

OLED's. The measured and extrapolated normalized saturation current of the TFT's fabricated with different structures and nitride temperatures using standard a-Si under constant DC bias stress (V_{GS} = 7.5V and V_{DS} = 12V) is given in Fig. 6. The BCP structure results in a higher TFT stability than the BCE structure for the same growth conditions, as a result of the *in situ* passivation of the back-channel and the protection of the channel from plasma etch damage during the fabrication process (7).

C. Improving the Low-Field TFT Stability

Because of the low-field degradation mode identified in Fig. 4, addressing the a-Si/nitride interface is key for long lifetimes. As noted earlier, increasing the gate nitride deposition temperature improves the interface quality and thus the TFT lifetime. However, a negligible improvement in TFT current lifetime is observed by increasing the nitride growth temperature from 300°C to 350°C (Fig. 6). This implies that further improvement requires improvement of the quality of the a-Si.

Recently we found that including H_2 dilution in silane during PECVD growth of a-Si improves the quality of a-Si and the a-Si/SiN_x interface by reducing the weak Si-Si bonds which could later easily be broken (7). After post-process annealing to remove the plasma etch damage, the half-life of the 300°C nitride device improves from ~ 1 month with standard a-Si to over 10 years with a-Si grown from a silane-hydrogen mixture (Fig. 7). This "improved" a-Si allows us to take advantage of the improved nitride quality at 350°C. After an optimized annealing, the half-life of the TFT's grown with the improved a-Si and 350°C nitride improves to over 100 years (Fig. 7). We also find the optimum H_2 dilution ratio ($[H_2]/[SiH_4]$) to be close to 10.

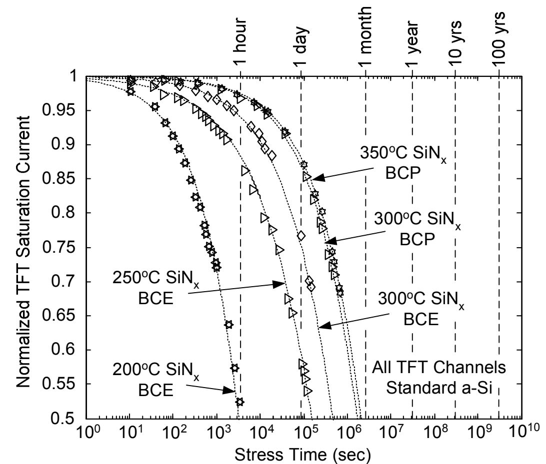

Fig. 6. Normalized TFT saturation current (V_{DS} = 12V) vs. time at a constant gate stress field of 2.5×10^5 V/cm (V_{GS} = 7.5V) for TFT's with different gate nitride deposition temperatures and different structures (BCE or BCP). All TFT have standard a-Si channel materials. The data is extrapolated using the low-field threshold voltage shift model of Fig. 2b.

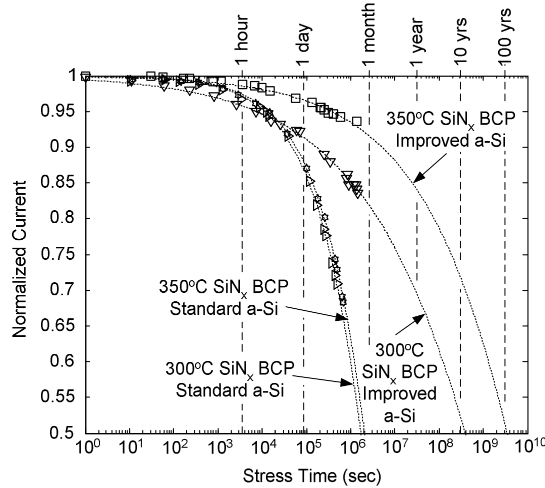

Fig. 7. Normalized TFT saturation current (V_{DS} = 12V) vs. time at a constant gate stress field of 2.5×10^5 V/cm (V_{GS} = 7.5V) for the improved a-Si TFT's. Extrapolations are based on the low-field model of Fig 2b.

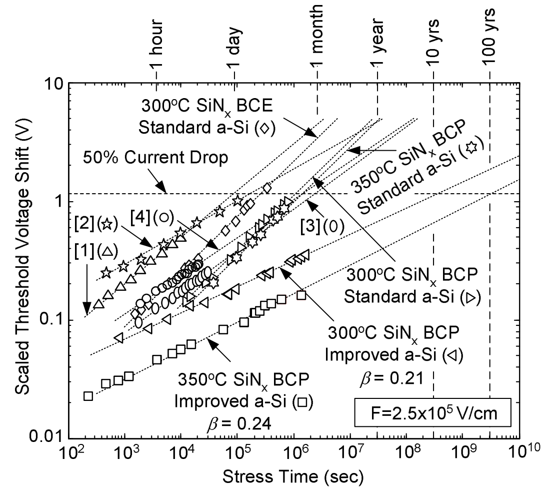

Fig. 8. Low-field (2.5×10^5 V/cm i.e. V_{GS} = 7.5V) threshold voltage shifts of conventional and improved a-Si TFT's fabricated in our lab or reported in the literature (1-4) and scaled to our stress conditions based on Eqn. (1). Extrapolations are based on the low-field model of Fig 2b. For standard a-Si, the β parameter is in the range of 0.34-0.45. The TFT parameters are given in the caption of Fig. 5.

The low-field threshold voltage shifts of the improved and standard a-Si TFT's are plotted in Fig. 8 and extrapolated in time, along with the data from other groups scaled to our stress conditions. For TFT's processed with standard a-Si, the β parameter of the defect creation model (Fig. 2b) is in the range of 0.34-0.45. For improved a-Si, the β parameter is much lower (0.21-0.24) resulting in a significant long-term stability improvement. The 50% drop in the TFT current corresponds to a 1.2V shift of the threshold voltage, showing an improvement of more than 1000X achieved over the previous work.

Summary and Conclusion

In summary, we have demonstrated a-Si TFT's with an extrapolated DC saturation current half-life of more than 100 years, an increase by a factor of more than 1000 compared to the previous art (1-4). This half-life is longer than the luminance half-life of high-quality green phosphorescent OLED's, showing that the TFT's are promising for driving OLED's in active-matrix OLED displays without requiring drift compensation circuits. The TFT's are grown in a conventional PECVD system on glass, with a high-temperature-plastic compatible process (5). This implies that a-Si TFT's and their commercial production equipment may be used for high lifetime a-Si TFT backplanes for AMOLED display applications.

Acknowledgement

We thank the DuPont Company for technical collaboration. This work was sponsored by the US Display Consortium.

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