Current Gain of Amorphous Silicon Thin-Film Transistors Above the Cutoff Frequency

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A key challenge for the development of high functionality thin-film large-area electronic systems is the operational frequencies achievable by Thin-Film Transistors (TFTs). These frequencies are typically limited by low transconductances and large (gate and overlap) capacitances. However, we have recently demonstrated energy-harvesting and communication systems, as shown in Fig. 1, utilizing thin-film circuit topologies that allow operation at or above the TFT cutoff frequency (*ft*) [1,2] by using inductors to "resonate out" the effect of TFT capacitances. Measurement and modelling of current gain near and above ft is thus critical (as opposed to conventional studies of current gain *below ft*). In this paper we (1) show above-*ft* measurements for standard bottom-gate amorphous silicon (a-Si) TFTs and self-aligned bottom-gate a-Si TFTs and (2) illustrate how large TFT gate-drain capacitances lead to a slow current-gain roll-off at frequencies *above ft*.

The cutoff frequency is an indicator of the intrinsic speed of a transistor, defined as the frequency at which the current gain (A_I) of the transistor has fallen to unity. Under the (initial) assumption that the magnitude of the transconductance (g_m) is greater than the quantity ωC_{gd} (frequency of operation x gate-drain capacitance), the current gain expression can be simplified as in Fig. 2. Plotting A_I vs frequency results in a curve with a slope of -20dB/decade, with the unity gain frequency (*ft*) occurring when $f = g_m/[2\pi(C_{gs}+C_{gd})]$. Current gain A_I is measured (from the two-port-network parameter *H21*) on TFTs biased in saturation, with a calibrated ENA5061B network analyzer.

Standard bottom-gate a-Si TFTs as shown in Fig. 3 are fabricated on glass (max. process temperature 180C, passivated with a blanket silicon nitride layer) with a channel length of 6µm and gate-source/drain overlaps of 5-15µm; A typical IV-curve in Fig. 4. A typical VNA *H21* measurement is shown in Fig. 9, with a TFT (5µm S/D-G overlaps, x_{ov}) biased in saturation with V_{gs}=V_{ds}=15V, showing a measured *ft* equal to 1.15MHz, in line with estimates that can be obtained from measurements of g_m and C_{gs} / C_{gd}.

Self-aligned, back-channel passivated bottom-gate TFTs as shown in Fig. 5 are also manufactured to evaluate the impact of significantly decreased parasitic TFT overlap capacitances on above-ft performance. Both the back-channel passivation and source/drain contacts are self-aligned to the TFT gate by angled lithographic exposure through the glass substrate [3,4]. A device micrograph is shown in Fig. 6. IV characteristics are similar to those in Fig. 4. As a result of the self-alignment, the measured TFT *ft* are correspondingly higher; this is expected from the expanded expression of *ft* shown in Fig. 7 (a). Fig. 8 shows that sweeping the gate voltage on self- and non-self-aligned TFTs, changes the transconductance of the TFT (in saturation) linearly, and as such also changes *ft* linearly. The ratio of the slopes (~3.7) corresponds to the ratio $L \times (L+2x_{ov})$ for both types of TFTs (non-self-aligned TFTs have 15µm overlaps).

Fig. 9 also shows the noteworthy property that close to the cutoff frequency, the curve tends away from a -20dB/dec slope to a shallower slope. This indicates the presence of an increasing frequency-dependent component in the numerator of the current gain (a 'zero'), which we motivate is due to the inaccurate initial assumption that $g_m \gg \omega C_{gd}$; for our a-Si technology, these terms are in fact comparable even at MHz frequencies due to the low TFT mobility. To illustrate this, Fig. 10 shows analytical plots for both the initial current gain expression and the more accurate current gain *H21* (which takes into account the numerator zero, case (b) in Fig. 9); the decrease in slope is evident, and analytical *ft* values are close to those obtained experimentally. For non-self-aligned transistors, the large overlap capacitances cause the slope transition to occur earlier, even before reaching the unity gain frequency- this has the 'beneficial' effect of actually slightly *increasing* the device ft by several tens of kHz. Additionally Fig. 10 also illustrates that at frequencies significantly above ft that the current gain for non-self-aligned TFTs levels off at a *higher value* than for the self-aligned devices.

In conclusion, TFT frequency response above ft must be considered in the light of recently reported systems [1,2]. A roll-off in current gain close to and above *ft* is observed, due to comparable TFT g_m and parasitic capacitances. Self-aligning source and drain contacts of TFTs *does* raise the cutoff frequency of TFTs (in our case by a factor of almost 4x), but *only* non-self-aligned TFTs benefit from slightly increased *ft* due to this current gain roll-off. In addition, it is shown that non-self-aligned TFTs can achieve higher minimum current gain at frequencies well-above ft.

[1] L. Huang et al., "A Super-Regenerative Radio on Plastic based on Thin-film Transistors and Antennas on Large, Flexible Sheets for Distributed Communication Links," ISSCC 2013, pp. 458-459.
[2] Y. Hu et al., Flexible Solar-Energy Harvesting System on Plastic with Thin-film LC Oscillators Operating Above ft for Inductively-coupled Power Delivery" CICC 2012.
[3] K. Cherenack et al. "Self-Aligned Amorphous Silicon Thin-Film Transistors Fabricated on Clear Plastic at 300C", IEEE Trans. on Electron Devices, 2010 , Vol 57.
[4] D. Thomasson, T. Jackson. "Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer" IEEE Electron Device Lett., vol. 19, no. 4.

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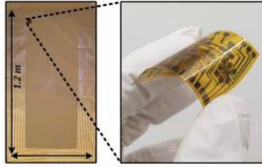


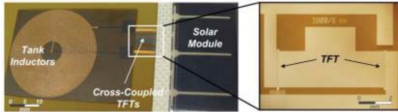
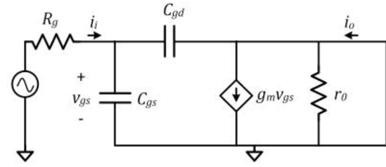


Fig. 1: TFT oscillator-based systems operating at or above TFT *ft* [1,2]



$$A_I \equiv \frac{i_o}{i_i} = \frac{g_m - sC_{gd}}{s(C_{gs}+C_{gd})} \approx \frac{g_m}{j\omega(C_{gs}+C_{gd})}$$

$$\text{when } |A_I| = 1, f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})}$$

Fig. 2: Derivation of TFT cutoff frequency

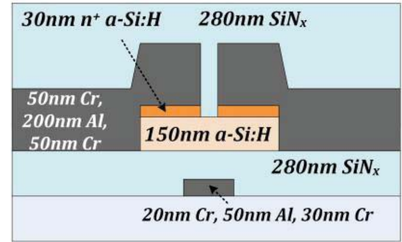


Fig. 3: Non-self-aligned TFT cross-section

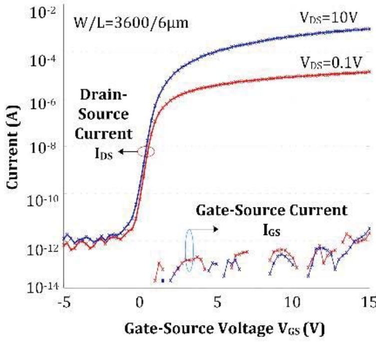


Fig. 4: Current-Voltage for TFT in Fig. 3

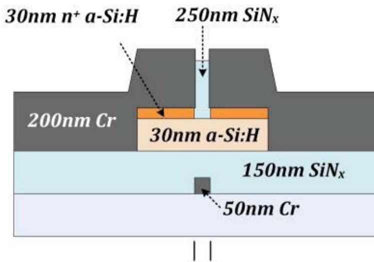


Fig. 5: Self-aligned TFT cross-section

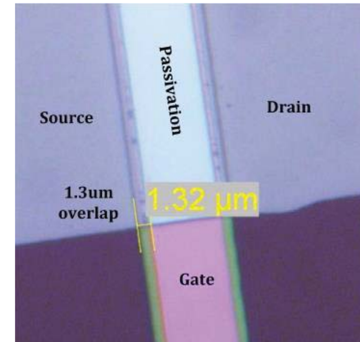


Fig. 6: Micrograph of self-aligned TFT

Case (a) $g_m \gg \omega C_{gd}$

$$\left|\frac{\mu(V_{gs}-V_t)}{j\omega L(L+2x_{ov})}\right| = 1$$

Case (b) $g_m \approx \omega C_{gd}$

$$\left|\frac{\mu(V_{gs}-V_t) - j\omega x_{ov}}{j\omega L(L+2x_{ov})}\right| = 1$$

Fig. 7: Expansion of TFT *ft* current expression

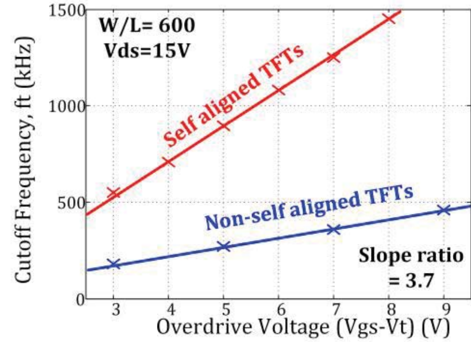


Fig. 8: *Experimental* cutoff frequency vs overdrive gate voltage

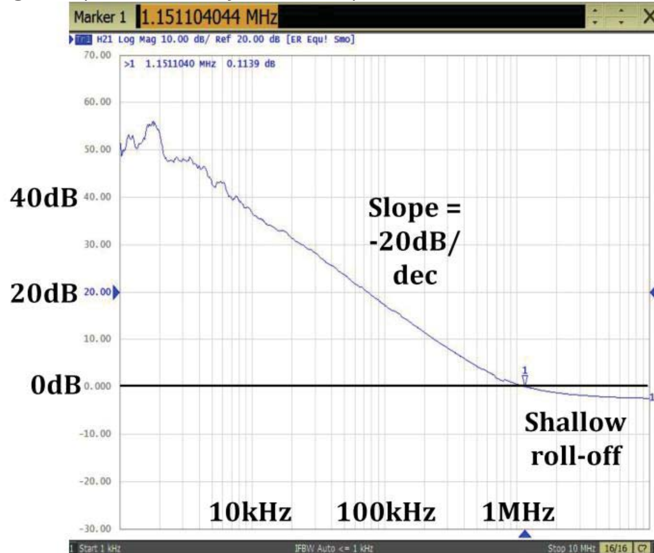


Fig. 9: *Experimental ft* measurement for non-self-aligned TFT with 5um overlaps

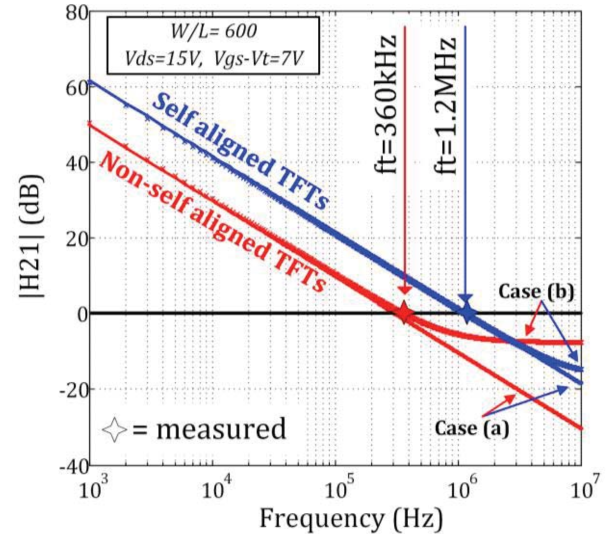


Fig. 10: Analytical plots for *ft* using expressions in Fig. 9 (with a *ft* ratio of 3.4, close to Fig. 8).