3D Multi-Gesture Sensing System for Large Areas based on Pixel Self-Capacitance Readout using TFT Scanning and Frequency-Conversion Circuits

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***Abstract*- This paper presents a flexible 40×40cm^2 gesture-sensing sheet for large-area interactive-spaces. The system achieves out-of-plane sensing to 16cm. Self-capacitance readout of individual electrode pixels in a 4×4 array enables multiple gestures to be sensed simultaneously without ghost effects. For high-sensitivity readout, pixel self capacitance is converted to frequency via high-Q LC oscillators formed from amorphous-silicon (a-Si) thin-film transistors (TFTs) and planar inductors patterned directly on flex. Frequency readout is then performed by a CMOS IC. Scalability in the number and scan rate of pixels is achieved by (1) inductively coupling all oscillators to the CMOS IC through a single interface, and (2) reading out all pixels in a row simultaneously in separated frequency channels. With a hand 10 cm in front of a pixel, an SNR of 22dB is achieved at a scan rate of 240Hz and power consumption of 26mW.**

I. Introduction

3D gesture sensing enables compelling interfaces for future electronic systems, particularly large-area interactive spaces. Optical and IR solutions provide rich features, but the resolution and sensing area is limited for gestures close by (<1m) [1], and the power consumption is substantially higher than capacitive systems. While traditional capacitance sensing has been limited to distances of 1-2cm, our previous work [2] focusing on display applications achieves extended range (>30cm) using row and column electrodes. This is achieved through the use of an underlying oscillating plane that mitigates electric field fringing caused by the display's ground plane beneath. The problem, however, is that row and column electrodes can suffer from ghost effects when sensing multiple gestures simultaneously (as in multi-touch displays). This is particularly limiting for large-area interactive-spaces applications, targeting collaborative interactions across multiple users via sensing interfaces embedded within every-day objects (table surfaces, wallpaper, furniture).

To overcome ghost effects, this work presents an extended-range capacitance-sensing system using an array of individually-addressable pixilated capacitance-sensing electrodes. Extended-range sensing requires high-sensitivity readout, posing several challenges for pixel-based sensing:

1. As the size of the array scales, the number of signals that must be interfaced to the CMOS readout IC increases; active-matrix approaches based on using thin-film transistors (TFTs) to control accessing of pixels can be considered, but these increase noise (due to TFT switching), degrade sensitivity (due to TFT on resistance), and limit the frame rate (due to TFT speed).
2. As the size of the array scales, higher readout rates are necessary due an increased number of electrodes per frame.
3. The routing required to each pixel in the array raises parasitic capacitive coupling to gestures, degrading the localization of capacitance sensing at the pixels.

To overcome these challenges, this work presents a system, which employs, for each pixel, embedded amorphous-silicon (a-Si) TFT circuits that are patterned on flex. The circuits perform capacitance-to-frequency conversion and control of pixel readout, greatly improving the interfacing and readout rate achievable with a CMOS IC. In the following sections, the system, circuits, prototype and performance are described.

II. System Overview

Fig. 1 shows the system architecture, consisting of a flexible pixel-based large-area sensing sheet, a flexible capacitance-to-frequency (C2F) conversion sheet, and a custom CMOS readout IC. The large-area sensing sheet consists of a 4×4 array of electrode pixels, each 5×5cm^2. Electrodes have been implemented using both ITO and copper. Extended-range sensing not only enables 3D gestures, but also substantially reduces power consumption by allowing a pixel separation pitch of 10cm. A large sensing area (40×40cm^2 in this system) can thus be achieved with relatively few (16) pixels.

For self-capacitance readout, the pixels connect to the C2F

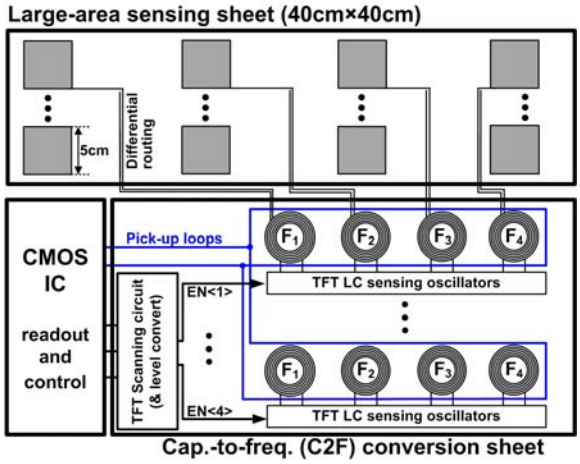

Fig. 1: Architecture of 3D pixel-based capacitance-sensing system.

conversion sheet. The C2F sheet consists of an array of TFT LC sensing oscillators (SOs), one for each pixel. Gestures perturb the self-capacitance of pixels, resulting in a frequency shift in the SOs. Frequency-division multiplexing has been proposed to increase readout frame rate [3]. In this work, the SOs corresponding to the four pixels in each row are set to four different nominal frequencies ($F_{1\text{-}4}$). This enables simultaneous readout of each row in four different frequency channels. Each row of SOs is surrounded by a pick-up loop, and the loops from the four rows are connected in parallel to a single interface of the CMOS IC. During readout, TFT scanning circuits, under the control of the CMOS IC, sequentially enable each row of SOs via the round-robin *EN<1-4>* signals. Scalability in the number of pixels, and thus the overall sensing area, is enabled by the use of a single interface to the CMOS IC, and increased frame rate is enabled by simultaneous readout of the four pixels in each row.

To enable extended-range sensing with pixels, two approaches are critical. First, high-Q TFT SOs are used, enabled by large patterned inductor. This enhances sensitivity by filtering both stray noise and TFT device noise. The SOs and low-noise CMOS readout channel are described further in the following section. Second, on the large-area sensing sheet, differential routing is used for the traces that connect the SOs to the pixels. Although only a single trace is required for each connection, electrostatic coupling from gestures to anywhere on the trace can affect the capacitance that is sensed, thus degrading sensing localization at the pixels. To ensure sensing localized at the pixels, a counter-phase signal is routed close to each trace (as shown in Fig. 1). This causes strong electrostatic coupling to the trace, confining its electric field, thus making the pixel self-capacitance the dominant coupling to gestures. The counter-phase signal is readily available from the TFT SOs.

III. Sensing and Readout Circuits

The details of the C2F sheet and CMOS IC are shown in Fig. 2. The four SOs in each row are designed to have nominal frequencies separated by a minimum of 400kHz (set by the patterned planar inductors). The four SOs inductively couple to a pick-up loop. The CMOS IC consists of four frequency-readout channels and a scanning-control driver.

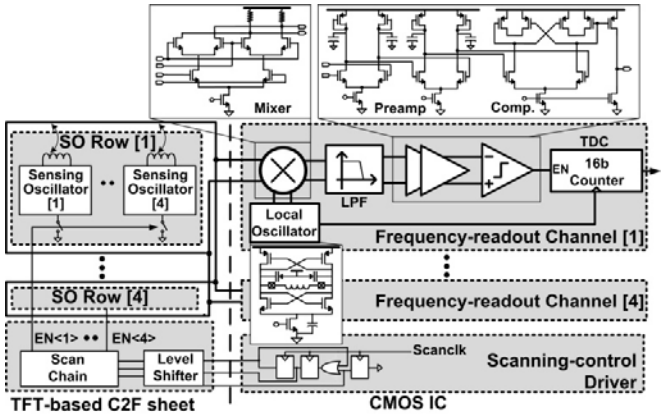

Fig. 2: C2F sheet and CMOS IC details.

The four CMOS frequency-readout channels are similar to that presented in [2]. Each channels consists of an LC local oscillator (set for each of the nominal SO frequencies). Frequency down conversion is performed via a differential Gilbert mixer, and frequency-channel isolation is achieved on the down-converted signal by a second-order low-pass filter (LPF). The LPF cutoff frequency is set at 20kHz, which results a minimum amplitude suppression of 26dB from adjacent channels. The resulting output is amplified into a frequency-modulated digital signal using a two-stage preamplifier and a continuous-time hysteretic comparator. To reduce noise, two approaches are adopted: (1) the preamps filter out noise with a cutoff frequency of 200kHz, set by the 5pF output capacitors; (2) hysteresis in the comparator prevents erroneous output edges that can occur due to noise near the crossing point of the down-converted signal. Digitization of the frequency is then performed using a 16-b time-to-digital converter (TDC) with clock derived from LO.

The scanning-control driver simply generates a global reset and two-phase clock signals with 3.6V swing to control generation of the round-robin *EN<1-4>* signals by the TFT circuits on the C2F sheet. The following subsections describe details of the TFT circuits, which are critical for enabling enhanced scan rate and scalability for the pixel array.

A. Thin-film Sensing Oscillators (SOs)

The SO circuit is shown in Fig. 3. High-frequency oscillations are required to adequately separate the four frequency-readout channels, and low phase noise (jitter) is required to ensure adequate capacitance-sensing accuracy within the channels. Although the TFTs have low performance, with f_T around 1MHz, high-frequency oscillations beyond f_T are achieved using an LC oscillator. This is possible because the tank inductor resonates out the TFT parasitic capacitances, thus enabling gain and oscillation at frequencies not limited by f_T. The critical requirement is that a positive-feedback oscillation condition be met ($g_m R_{tank}>1$). The ability to pattern physically-large spirals enables increased inductor Q (high R_{tank}), enabling robust oscillations despite the low TFT performance [4]. Fig. 4 shows the inductor parameters for the four nominal SO frequencies (3.0MHz, 2.4MHz, 1.7MHz, 1.3MHz). Oscilloscope waveforms of four parallel SO channels $F_{1\text{-}4}$ are also plotted. The resulting high-Q tanks also improve oscillator jitter against TFT noise. This is a critical factor since it poses the dominant limitation on system SNR. The TDC-measured down-converted frequency RMS noise is smaller than 38Hz for all four channels.

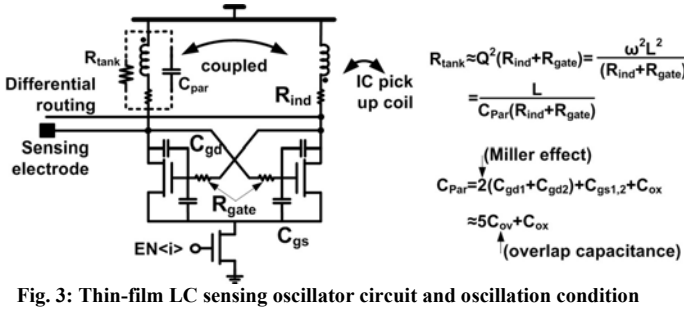

Fig. 3: Thin-film LC sensing oscillator circuit and oscillation condition derivation.

	Ind. 1	Ind. 2	Ind. 3	Ind. 4
Diameter	4cm (double layer)			
Frequency(MHz)	3.0	2.4	1.7	1.3
Inductance(μH)	114	207	310	639
Q (@resonance)	107	78	56	33
$g_m R_{tank}$	15	23	18	20

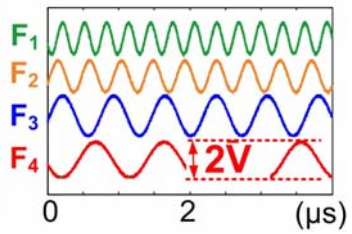

Fig. 4: Flexible planar inductor parameters and four channel SO waveforms with minimal frequency separation of 400kHz.

B. Thin-film Scanning Circuit

The aim of the TFT scanning circuit is to generate sequential row-enable signals (*EN<i>*) scalable to a large number of rows, yet using a minimal number of signals from the CMOS IC. The *EN<i>* signals drive the tail TFT of the SOs (Fig. 3). A challenge for the scanning circuit is that, on the one hand, a large and rapid output voltage swing is required both for adequate current (transconductance) in the SO devices (to meet the positive-feedback oscillation condition) and for high scan rate; on the other hand, the absence of PMOS devices in a standard a-Si process can lead to large static currents, elevating power consumption, particularly when using large supply voltages and devices for the required swing and speed.

The scanning circuit used is shown in Fig. 5, based on a design recently presented in [5]. The circuit requires only three control signals from the CMOS IC: two-phase clock signals (*CLK_IC*, *CLK_IC*) and a global reset (*GRST_IC*). Aside from the level converters (which convert the CMOS 3.6V IO voltages to ~15V), static power consumption is consumed by only one scan element (Scan[i]) at a time. This enables scalability in the number of rows with minimal scaling in total power consumption. Despite the absence of PMOS devices, *EN*<i> outputs with full swing close to the TFT supply voltage are generated.

Fig. 6 shows measured operational waveforms for both a level converter and the N^{TH} scan element in the chain. The level converter is a common-source amplifier biased for adequate gain through an input AC-coupling network (Fig. 5). The AC-coupling time constant is set slow enough to preserve the clock pulses. A low-value load resistor, chosen for fast rise time, prevents the output of the common-source amplifier from fully reaching ground. To achieve a swing to ground, an output capacitor and NMOS are included, thus ensuring maximal gating of static currents in the scan elements.

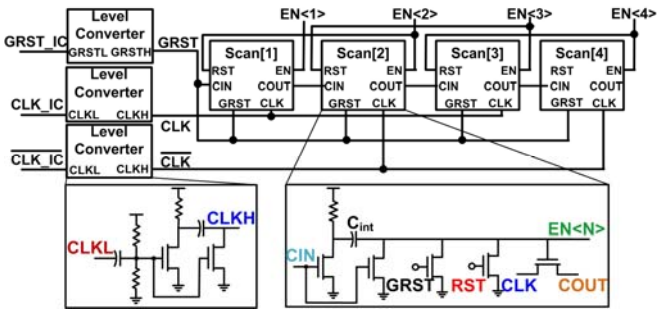

Fig. 5: TFT level-shifters and scan circuits.

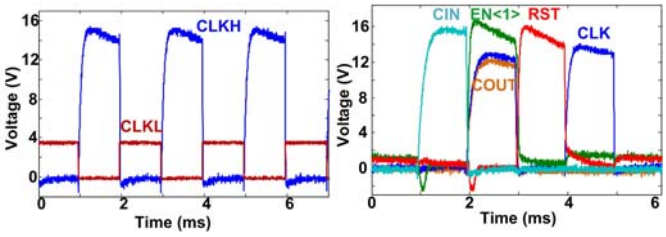

Fig. 6: Operation waveform of level converter and scan element.

The scan element (Fig. 5) works as follows. Initially, only the *EN<N>* node is discharged to ground through the global-reset signal (*GRST*). Then, during scanning, the N^{TH} element receives a charge-in signal (*CIN*) from the N-1 element, driven by *CLK/CLK*. This discharges both plates of the internal capacitor C_{int}. Subsequently, when *CIN* goes low, the pull-up resistor charges the bottom plate of C_{int} high. C_{int} (470pF) is set to be larger than the parasitic capacitors loading the output, thus causing *EN<N>* to also rise to a value close to the supply voltage. This then enables *COUT* to go high when controlled by *CLK/CLK*. Following this, only the top-plate of C_{int} is discharged through the reset signal (*RST*) received from N+1 element. Subsequently, leakage currents due to TFTs on the top plate of C_{int} act to hold the output voltage in this state. This allows the number of scan elements to be robustly increased despite longer time between active reset of the dynamic output node. Additionally, since *CIN* is asserted for only one scan element at a time, the active and static power does not scale with the number of elements in the chain.

IV. Experimental Results

The system is prototyped, as shown in Fig. 7, using a custom IC fabricated in 130nm CMOS from IBM and TFT circuits fabricated in house on 50μm polyimide (only half of the C2F sheet is shown for clarity). TFT processing is based on hydrogenated a-Si (a-Si:H), at a temperature of 180°C [6]. The cross-coupled TFTs of the SOs are sized 3600μm/6μm for the low-frequency channels (F_3 and F_4) and 1800μm/6μm for the high-frequency channels (F_1 and F_2). The TFTs of the scan circuits are sized 2000μm/10μm (*CIN* TFTs) and 1000μm/10μm (*GRST*, *RST* and *CLK* TFTs). The TFTs of the level shifters are sized 7200μm/10μm for the common-source amplifier and 3000μm/10μm for output pull-down device.

Fig. 8 shows sensitivity measurements using copper electrodes. On the left, the readout SNR and TDC code (with

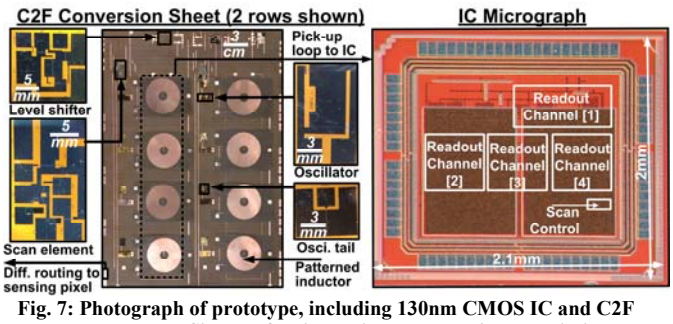

Fig. 7: Photograph of prototype, including 130nm CMOS IC and C2F sheet based on a-Si TFTs fabricated in house on 50μm polyimide.

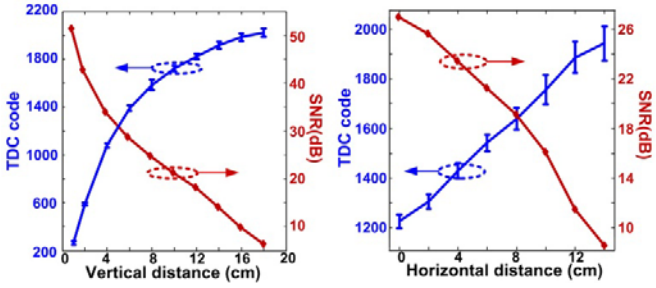

Fig. 8: Measured TDC output and SNR versus vertical distance and horizontal displacement of a hand with respect to sensing electrode.

RMS bars) are plotted versus distance for a hand positioned above a sensing electrode; as shown substantial SNR is maintained out to 16cm (with 22dB SNR at 10cm). On the right, the SNR and TDC code are shown versus horizontal displacement for a hand 5cm above a sensing electrode; 22dB SNR is achieved for a displacement of 5cm (corresponding to the worst-case displacement for the 10cm electrode pitch used).

Fig. 9 shows the measured waveforms and readout outputs in the time domain. The waveforms on the left show the round-robin *EN<1-4>* signals generated by the TFT scan circuits. The readout outputs on the right show the frequency shift obtained from the CMOS IC while swiping a hand across a row of electrodes at a distance 6cm above (the frequency change Δf shown is derived from the obtained TDC code).

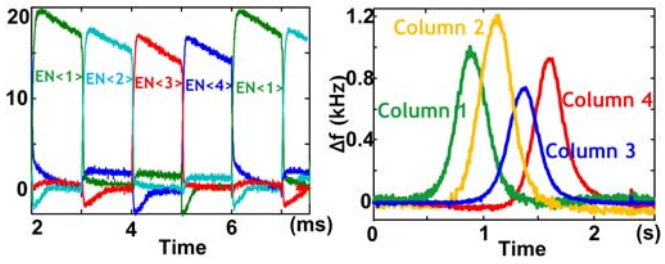

Fig. 9: Measured waveforms of scanning circuit output and readout output with a hand swiping 6cm above a row of electrodes.

Table 1 shows the systems measurement summary. The system achieves an SNR of 22B with a hand at 10cm distance. At the distance of 10cm, the x,y-direction resolution is 1.8cm, and the z-direction resolution is 1cm. The 4-channel CMOS readout circuit consumes 1.8mW. The TFT SO array and scanning circuits consume 24mW from a 20V supply. With the scanning circuit running at 1kHz, the readout time is 1ms per row, enabling a 240Hz scan rate.

V. Conclusions

3D gesture sensing enables compelling human-computer interfaces. Systems scalable to large-area sheets and based on flexible form factor are of particular interest due their potential to be integrated within objects and surfaces in typical living spaces. Capacitive-sensing systems have recently demonstrated the ability to achieve extended range, making them viable for 3D gesture sensing; however, pixel-based systems have not previously been achieved, limiting the ability

Table 1: System performance summary

Performance Summary (copper electrodes)			
Technology			
LAE		a-Si on 50µm polyimide @ 180 °C	
CMOS IC		130nm CMOS	
LAE Sensing Array			
Channels	4 x 4	Panel size	40cm x 40cm
Freq.	1.2~3MHz	SO power	24mW@20V
CMOS IC Readout			
SNR	35dB@4cm 22dB@10cm	Resolution* @10cm	1.8cm(x) 1.8cm(y) 1cm(z)
Scan rate	240Hz	Power consumption	1.8mW

*Resolution is defined as displacement where mean TDC code equals code RMS.

to detect and isolate multiple gestures simultaneously without ghost affects. This work achieves extended-range capacitive sensing (>16cm) using a scalable array of pixels. Pixel sensing poses a challenge due the need for an increased number of interfaces to the readout IC. The proposed system overcomes this by employing TFT sensing oscillators (SOs) for pixel capacitance-to-frequency conversion and TFT scanning circuits for sequentially enabling rows of pixel SOs. All pixels are thus interfaced to the readout IC through a single interface, via inductive coupling. All TFT circuits are fabricated in-house on flex and the IC is fabricated using a 130nm CMOS process from IBM. Using a 4×4 array of pixels, spanning a sensing area of 40cm×40cm, the system achieves a scan rate beyond 240 frames per second at a power consumption of 1.8mW for the IC and 24mW for the TFT circuits.

Acknowledgements

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