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High Current Density, Hybrid Nanocrystalline/Amorphous Silicon Schottky Diodes

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We are developing a manufacturable process for large-area systems, based on laminating multiple sheets of thin-film electronics and CMOS ICs, to form "sensing wallpaper" [1]. In order to transmit signals and power from one sheet to another in a robust manner, which is tolerant to misalignment, reliable, and flexible, we use non-contact inductive links. When a sheet of thin-film electronics receives an AC-modulated signal it has to down-convert it to the envelope signal, leading to the need for a thin-film diode for AC-to-DC rectification. In this talk we present a hybrid nanocrystalline silicon / amorphous silicon Schottky diode developed for this application. The diode has a current density of 5 A/cm^2 at 1 V, one of the highest current density thin-film diodes (of any technology processed at < 200°C) to date.

The diode is deposited at 180°C by plasma enhanced chemical vapor deposition at 70 MHz frequency. The structure consist of a Schottky chrome contact, 750 nm n- nc-Si, 150 nm n+ nc-Si, and a chrome ohmic contact. The Schottky interface is formed between the chrome contact and an amorphous silicon incubation layer, deposited before the n- nc-Si film has nucleated. The n- film is doped by background impurities and has an ionized impurity density of 10^{16} cm^{-3} (from CV measurements). The high current density of the device (5 A/cm^2 at 1V) can be attributed to the high conductivity of the nc-Si, which means that unlike a Schottky diode formed entirely out of a-Si, it is not affected by space charge limited current [2] . The device also has a high ON-to-OFF current ratio (>1000 V for +1 V/ –8 V). A Schottky device has the advantages over a p-n junction of reduced turn-on voltage and the need for only a single doping source.

For our application, it is desirable to operate at high frequencies, since inductive links are more power efficient at high frequencies. A 0.01 mm^2 hybrid diode has a series resistance of 120 Ω and a capacitance of 7 pF, leading to a calculated critical frequency ($f_c=1/(2\pi R_S C_J)$) of 190 MHz. Diodes have been tested in a half-wave rectifier configuration with a parallel 100 kΩ resistive and 10 nF capacitive load. At 10 MHz for an AC signal with a 4V amplitude, we obtain a DC rectified voltage of 3.4 V. Testing at higher frequencies is ongoing.

[1] Y. Hu et al., VLSI Symposium, June 2013 (In press)

[2] J. Sanz-Robinson et al., Device Research Conference (DRC), June 2012

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