Hole-Blocking Crystalline-Silicon/Titanium-Oxide Heterojunction with Very Low Interface Recombination Velocity

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Abstract — We demonstrate a hole-blocking crystalline-silicon/titanium-oxide heterojunction that can be fabricated by a modified MOCVD process at only 100 ºC substrate temperature. Ultra thin layers of only 1-4 nm TiO_2 can be reliably deposited on silicon with no pinholes. Band alignment at the Si/TiO_2, experimentally determined using surface spectroscopy, confirms that Si/TiO_2 interface has a large barrier at the valence band, which blocks holes. The hole-blocking characteristics allow the Si/TiO_2 heterojunction solar cells to achieve power conversion efficiencies > 7%. Finally, the electrical quality of the Si/TiO_2 interface was characterized in terms of interface recombination velocity. We show that annealed Si/TiO_2 interfaces can achieve recombination velocities of ~ 200 cm/s.

Index Terms — heterojunction, photovoltaic cells, silicon, titanium.

I. INTRODUCTION

One possible approach to low-cost silicon photovoltaics involves replacing the p-n junction, fabricated at temperatures higher than 800 °C [1], with a low-temperature fabricated heterojunction. Previously a solar cell using a silicon/P3HT heterojunction has been demonstrated with a power conversion efficiency of larger than 10%, as well as a solar cell using a silicon/PEDOT:PSS heterojunction with an efficiency of 12% [2-4]. Electrically the Si/PEDOT heterojunction functions as an electron blocker, i.e. photogenerated electrons in silicon are unable to pass through PEDOT. However, to date hole-blocking heterojunctions deposited on silicon have not been reported.

In this paper we present a hole-blocking Si heterojunction using TiO_2 as the wide bandgap material. Surface spectroscopy shows that the band-alignment at the Si/TiO_2 interface is such that there is a large difference between the valence bands of Si and TiO_2 which prevents conduction of holes from Si to TiO_2. Furthermore, there is a small difference between the conduction bands of Si and TiO_2, allowing electrons to easily flow from Si to TiO_2. Using such a heterojunction we have successfully fabricated solar cells with power conversion efficiency of > 7 % without a p-n junction and a maximum processing temperature of 100ºC.

Finally, we investigate the electrical quality of the 'as-deposited' Si/TiO_2 interface. X-ray spectroscopy reveals a Si band-bending of 0.4 eV at the $p-Si/TiO_2$ interface, which hints at the presence of surface defects in Si. Photoconductance decay experiments confirm that the "as deposited" $n-Si/TiO_2$
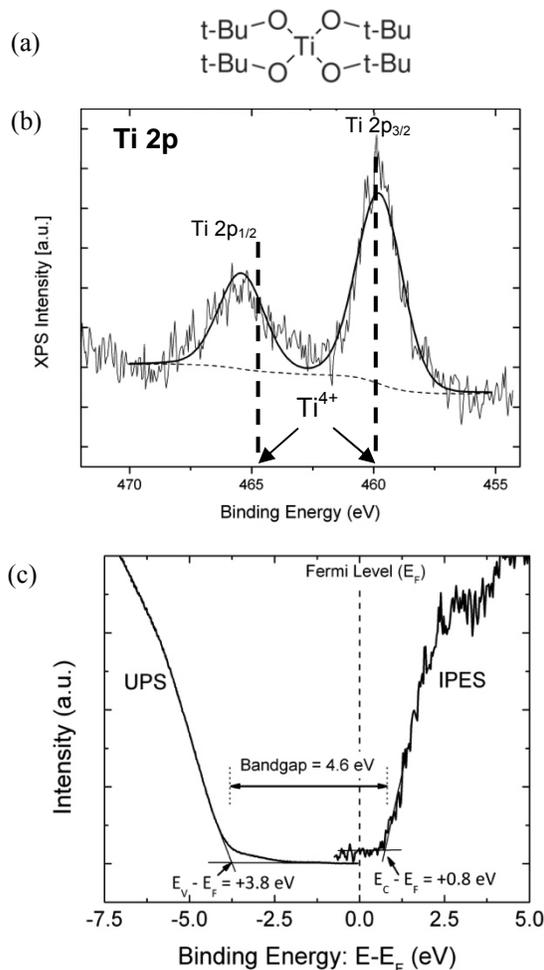

Fig. 1. (a) Structure of titanium(IV) tetra(tert-butoxide) - the titanium dioxide precursor. (b) XPS spectrum of the titanium dioxide layer on silicon. Also shown are the fitted Gaussian peaks (bold line) and the Shirley background (dashed line). (c) Combined UPS and IPES spectrum of TiO_2 on p^+Si, showing the bandgap of TiO_2 layer along with the conduction/valence band offsets.

interface does have a high recombination velocity (>10^6 cm/s). However, the $n-Si/TiO_2$ interface recombination velocity can be reduced from > 10^6 cm/s to ~200 cm/s with *ex-situ* annealing at only 400 °C in inert ambient– a four orders of magnitude reduction.
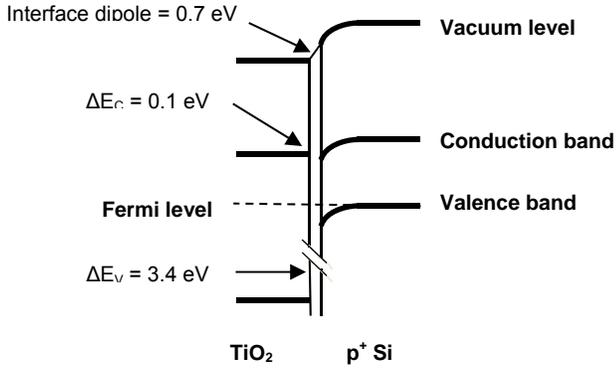
Fig. 2. Band alignment at the Si/p+-Si interface, as measured by surface spectroscopy.

II. FABRICATION & EXPERIMENTAL DETAILS

We deposit TiO_2 on silicon at substrate temperatures of only 100 °C using a modified metal-organic chemical vapor deposition (MOCVD) process with titanium (IV) tert-butoxide (Fig. 1(a)) as a precursor. Details of the silicon surface cleaning and deposition process have been published elsewhere [5]. Using this process we are able to reliably deposit ultrathin (1-4 nm) layers of TiO_2 on silicon without pinholes or defects.

All spectroscopic analysis was done in a separate ultra-high vacuum (UHV) chamber (base pressure $< 2 \times 10^{-10}$ mbar), details of which have been have been published elsewhere [6-7]. During transport to the UHV chamber, test samples were exposed to air for no more than 10 min.

Recombination lifetimes were measured by the quasi-steady-state photoconductance decay (QSSPCD) [8] using a WCT-120 manufactured by Sinton Consulting.

III. INTERFACE SPECTROSCOPY

X-ray photoelectron spectroscopy (XPS) was used was used to test if the deposited layer is indeed TiO_2. Experiment were

conducted with an Al kα radiation source (1486.6 eV), 0.5 eV resolution, on a highly-doped p+ Si (100) wafer (< 0.005 Ohm cm) coated with 3 nm thick TiO_2 film [6-7].

The Ti $2p_{3/2}$ peak for Ti^{4+} in TiO_2 generally lies in the range of 458.6 – 459.2 eV, while the Ti $2p_{3/2}$ peaks for Ti^{+2} and Ti^0 lie in the ranges 454.9 – 455.2 eV and 453.7 – 454.2 eV respectively [9]. The Ti $2p_{3/2}$ peak location in Fig 1(b) is at 459.7 eV, demonstrating it corresponds to Ti^{4+}. Additionally, a Ti $2p_{1/2}$ peak location is at 465.3 eV, implying a spin-orbit splitting of 5.6 eV, a value which lies much closer to the spin-orbit splitting of Ti^{4+} (5.5 eV) than to the spin-orbit splitting of Ti^0 (6.2 eV) [9]. Overall, the Ti 2p spectrum confirms the presence of Ti^{4+} species (from TiO_2) on the silicon surface.

Next, to measure the bandgap and band-alignment at the Si/TiO_2 interface, we used ultra-violet spectroscopy (UPS) and inverse-photoelectron spectroscopy (IPES). The UPS measurements used the He I line (21.22 eV) of a gas discharge source, and IPES used a commercial electron gun and a fixed photon energy detector (centered at 9.2 eV) [6-7].

Fig 1(c) shows a combined UPS and IPES spectrum of Si/TiO_2 interface as a function of the binding energy. UPS provides the valence band edge, which is found to be at 3.8 eV below the Fermi level. While IPES probes the conduction band edge, which is shown to be 0.8 above the Fermi level. The resulting band gap of the TiO_2 layer is hence 4.6 eV. This value is much bigger that the 3.8 eV reported for crystalline TiO_2 (rutile phase) [10]. This could be either the result of the TiO_2 layer being extremely thin or the TiO_2 layer being amorphous.

Combining the data from the surface science experiments we obtain the band diagram shown in Fig. 2. An interface dipole of 0.7 eV was found at the TiO_2/p-Si interface. Also, the silicon bands at the surface are not flat – a 0.3 eV band-bending is measured in silicon at the interface – which hints at the presence of surface defects at the as-deposited Si/TiO_2 interface. Finally, the band-diagram illustrates that the Si/TiO_2 interface has a large valence band offset ($\Delta E_V = 3.4$ eV) to block flow of holes from silicon to TiO_2. While there is a negligible conduction band offset ($\Delta E_C = 0.1$ eV), to allow flow of electrons from silicon to TiO_2 – suggesting that the Si/TiO_2 is a hole-blocking heterojunction.

(a)

Al (15 nm)
TiO$_2$ (1-4 nm)

Crystalline
p-Si

I

V

Ag (200 nm)

(b)

E_C
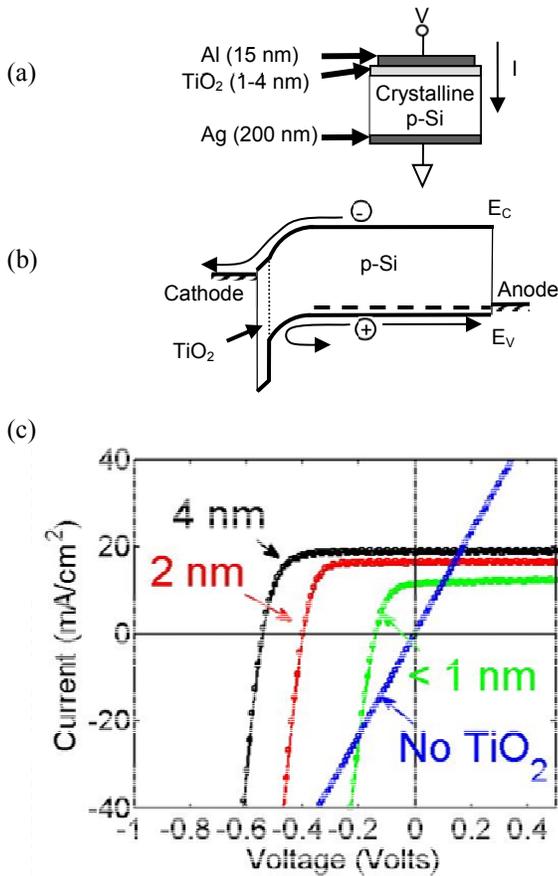
p-Si

Cathode

Anode

E_V

TiO$_2$

(c)

Fig .3. (a) Device structure and (b) band diagram of the Si/TiO$_2$ heterojunction solar cell showing blocked holes at the Si/TiO$_2$ interface and separation of photogenerated electrons and holes. (c) The I-V characteristics of the TiO$_2$/Si heterojunction solar cell under AM 1.5 illumination. The top metal lets in ~ 50% of the incident light.

To confirm the hole-blocking characteristics of the Si/TiO$_2$ heterojunction, diodes on 10^{15} cm^{-3} p-doped Si wafer were fabricated with TiO$_2$ layers 1 nm, 2 nm and 4 nm thick (Fig 3(a)). A control device with no TiO$_2$ was also fabricated. The top and bottom electrodes are deposited by thermal evaporation. The top electrode, made of Al, was kept intentionally thin (15 nm) so that ~ 50% of the light can go through and be absorbed in silicon. The bottom electrode was an Ohmic Ag/Si contact. The device area was 3.14 x 10^{-2} cm^2. It should be noted that the p-Si/TiO$_2$ heterojunction device shown in Fig 3(a) has a depletion region in silicon (Fig 3(b)) due to the low work-function of the Al anode (4.0 eV). Under illumination, this depletion region separates the photogenerated carriers in silicon, leading to a photocurrent.

The AM 1.5 response of these devices is shown in Fig. 3(c). The device without a TiO$_2$ layer behaves as a resistor because of insufficient hole-blocking. With a ~1 nm TiO$_2$ layer, holes from the p-Si are blocked, and we measure a short-circuit current and an open-circuit voltage. By a gradual increase in the TiO$_2$ layers thickness, from 2 to 4 nm, tunneling and,
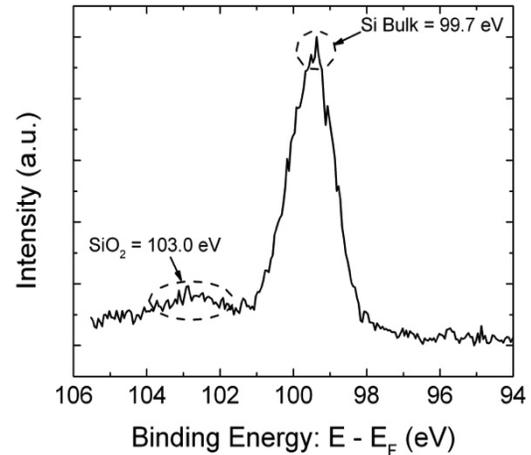

Fig. 4. Si 2p spectrum measured by XPS showing Si and SiO$_2$ peaks

perhaps, pinholes are reduced, leading to more effective hole blocking and resulting in higher values for V$_{OC}$ and J$_{SC}$. Further increase in TiO$_2$ thickness (beyond 4 nm) does not change the J-V, arguably because at that thickness most of the holes are effectively blocked. At 4 nm we obtain V$_{OC}$ of 0.52 V, J$_{SC}$ of 19.3 mA/cm^2 and fill factor of 70%, which translates to a power conversion efficiency of 7.1% At this point, the efficiency is primarily limited by the absorption losses in the semi-transparent top metal.

IV. INTERFACE QUALITY

To obtain the highest possible efficiency for the crystalline-Si/TiO$_2$ heterojunction, a fundamental understanding of the interface quality is important. An unpassivated silicon surface has dangling silicon bonds, which lead to midgap defects and Fermi level pinning. The former degrades device performance by reducing the effectiveness of the hole-blocking TiO$_2$ layer - if holes can recombine at the Si surface then TiO$_2$ is no longer relevant. The latter degrades device performance by adversely affecting the open-circuit voltage. Hence it is critical to characterize surface defects and if necessary, reduce the number of defect states.

To probe if there are any surface defects the Si 2p spectrum was measured using XPS (Fig 4). At the p$^+$-Si/TiO$_2$ interface, the Si 2p peak was measured at 99.7 eV. In flat band this value should be at 99.3 eV. The energy shift implies a band-bending of 0.4 eV at the Si/TiO$_2$ interface. The TiO$_2$ is undoped and only 3 nm thick, so the band-bending is probably not the result of charge transfer but evidence of charged interface states or Fermi-level pinning. Also observed in the Si 2p XPS spectrum is a small SiO$_2$ peak at 103.0 eV. At this point it is unclear if this peak originates from Si-O-Ti bonds or a result of adventitious oxygen trapped during the deposition process.

Interface quality can also be characterized in terms of an interface recombination velocity, which is directly related to
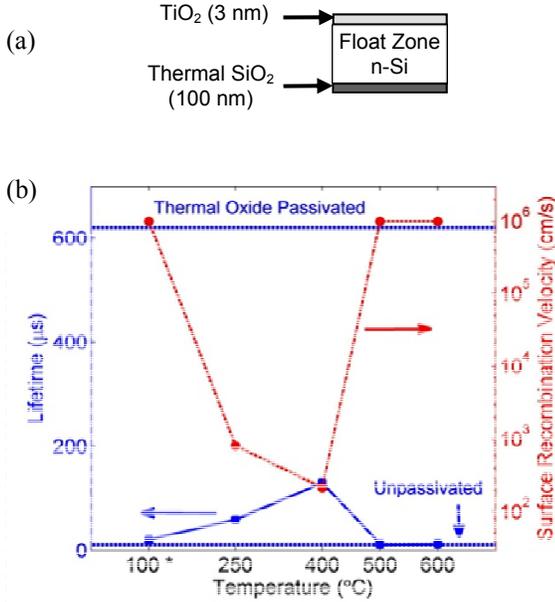
Fig. 5. (a) Structure used for photoconductance decay experiments (b) Measured effective recombination lifetime of TiO$_2$ coated silicon as a function of annealing temperature. Also shown are the calculated values of the interface recombination velocity

the interface defect density. The recombination velocity (S) can be determined by measuring the effective lifetime as given by the following equations:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} \qquad (1)$$

$$\tan\left(\frac{W}{\sqrt{D_p \tau_{surface}}}\right) = S\sqrt{\frac{\tau_{surface}}{D_p}} \qquad (2)$$

where τ_{eff} is the effective lifetime measured, τ_{bulk} is the lifetime associated with the bulk, $\tau_{surface}$ is the lifetime associated with the surface, W is the width of the substrate, D_p is the diffusion coefficient of holes in n-Si.

Lifetimes were measured using Quasi Steady-State Photoconductance Decay (QSSPCD) experiments [8] on 300 um thick 10^{15} n-type FZ silicon wafers with bulk lifetime larger than 500 μs.

First the Si wafer was coated with a high-quality thermal oxide grown at 1050 ºC. The effective lifetime measured after this step was 625 μs. Under the assumption that the recombination at the Si/SiO$_2$ is nearly zero, the effective lifetime measured with thermal-oxide is equal to the bulk lifetime (since, $\tau_{surface}$ approaches infinity). Next the oxide on the top surface was etched off and a native oxide was allowed to grow on the exposed Si surface. Due to the high-density of interface defects, the measured lifetime fell to 10 μs. Next, the silicon surface was cleaned using the RCA recipe and 3 nm of

TiO$_2$ was deposited (structure shown in Fig 5(a)). With TiO$_2$ on top of the surface, the measured lifetime slightly improved to 18 μs, arguably due to reduction of surface defects. From the measured lifetime values we extract an interface recombination velocity of $> 10^6$ cm/s at the "as-deposited" Si/TiO$_2$ interface. Such a high recombination velocity is not very surprising considering the band-bending in silicon measured by XPS (Fig 4).

To improve the interface quality, the samples were annealed in an inert ambient (N$_2$ gas) at different temperatures. The results are shown in Fig. 5(b). The effective lifetime increases to 130 μs as the annealing temperature increases to 400 °C. However beyond 500 °C, the lifetime drops rapidly below 11 μs. Concomitantly, the interface recombination velocity rapidly decreases till 400 °C, from $> 10^6$ to $\sim$ 200 cm/s and then rapidly increases again to 10^6 at 500 °C. The reason for the drop in effective lifetime at 500 °C is unclear. Two possibilities are: (a) the TiO$_2$ is undergoing phase transformation - TiO$_2$ is known to undergo phase transformation from anatase to rutile above 500 °C [11], or/and (b) the bulk lifetime (τ_{bulk}) is getting reduced due to furnace contamination.

It has been previously reported that Si/TiO$_2$ interface can be passivated by growing a silicon dioxide layer underneath the TiO$_2$ layer (between Si and TiO$_2$) [12]. However, the process requires very high temperatures (800 °C). To the best of our knowledge, this work is the first to report a method to passivate the Si/TiO$_2$ interfaces at temperatures of only 400 °C

V. CONCLUSIONS

We demonstrate that 1-4 nm thick TiO$_2$ can be deposited on silicon to create crystalline-Si/TiO$_2$ heterojunctions. These heterojunctions block holes while letting electrons through, enabling heterojunction solar cells with power efficiency >7%. Finally, we show that with suitable annealing, Si/TiO$_2$ interfaces can be electrically passivated to yield an interface recombination velocity of only 200 cm/s.

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