Integrated All-silicon Thin-film Power Electronics on Flexible Sheets For Ubiquitous Wireless Charging Stations based on Solar-energy Harvesting

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Abstract

With the explosion in the number of battery-powered portable devices, ubiquitous powering stations that exploit energy harvesting can provide an extremely compelling means of charging. We present a system on a flexible sheet that, for the first time, integrates the power electronics using the same thin-film amorphous-silicon (a-Si) technology as that used for established flexible photovoltaics. This demonstrates a key step towards future large-area flexible sheets which could cover everyday objects, to convert them into wireless charging stations. In this work, we combine the thin-film circuits with flexible solar cells to provide embedded power inversion, harvester control, and power amplification. This converts DC outputs from the solar modules to AC power for wireless device charging through patterned capacitive antennas. With 0.5-2nF transfer antennas and solar modules of 100cm^2, the system provides 47-120µW of power at 11-22% overall power-transfer efficiency under indoor lighting.

System Overview

Thin-film semiconductors (e.g., organics, a-Si, etc.) can be fabricated at low-cost on plastic foils, enabling conformal sheets spanning large areas. While this results in inexpensive solar cells for harvesting substantial power [1], the power electronics is typically implemented in discrete modules. By integrating all power circuits using a-Si thin-film transistors (TFTs), we demonstrate how complete functionality for a wireless device-charging station can be combined in a flexible monolithic sheet that could be applied onto arbitrary surfaces. Recent thin-film systems have been reported for power metering [2] and energy harvesting (by combining separate device technologies) [3]; we present an approach to integrate harvesting sources and circuits in the same a-Si technology, which is the dominant thin-film technology.

Since the TFTs have very low performance compared to crystalline silicon devices, several challenges are raised for power circuits. First, low currents limit the power that can be delivered. Second, low speeds (typical f_T is 1MHz) lead to low inductor quality factors. Third, only unipolar devices are typically available (either n-channel or p-channel), which limits the gating of currents in switching topologies.

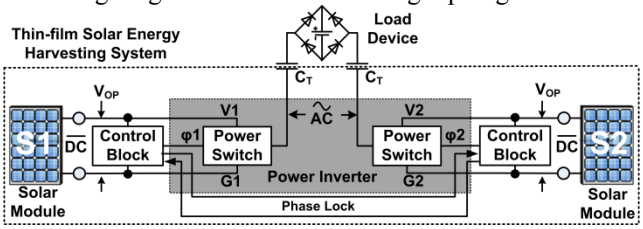

Fig. 1: Block diagram of solar-harvesting system.

Fig. 1 shows the architecture of the charging system. The blocks overcome these challenges and generate AC power using a power inverter and control circuits, all powered by the solar modules (S1/2). Each module consists of solar cells in series and operates at an output voltage V_{OP} of 8.4V; AC power is then wirelessly delivered to load devices via transfer capacitors (C_T). The power is then be stored on the load devices using a simple rectifier circuit (as shown).

Power Inversion and Control Circuits

Fig. 2 shows the power inverter circuit. To generate an AC output current, the two solar modules (S1/2) are used. The anodes (V1/2) are directly connected to transfer capacitors, and only the return path currents are switched at the cathodes via NMOS TFTs; M1/2 must thus switch in counter-phase, alternatingly drawing current from S1/2. Using two solar modules in this way enables a topology free of inductors and PMOSs (which are difficult to realize in a-Si). The output current is thus set by NMOS power switches, which maximizes the current, and all of the S1/2 current is delivered to the load, yielding high power-inverter efficiency.

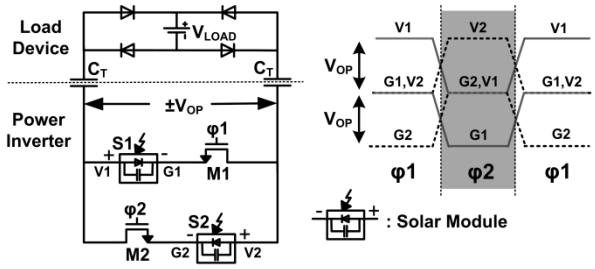

Fig. 2: Power inverter using two solar modules to provide alternating current via only NMOS power switches; waveforms shown on right.

However, this scheme results in switching connections between G1/V2 and G2/V1, causing the nodes to oscillate with respect to each other (see waveforms of Fig. 2). With oscillating source nodes, M1/2 are difficult to control simultaneously. To achieve synchronized, non-overlapping control signals (φ1/2), the coupled oscillators (O1/2) shown in Fig. 3 are used. Each oscillator is formed using five NMOS stages with pull-up resistors. The oscillators are separately powered by S1/2, and their last stages are cross-coupled via pull-down devices (M3/4). These ensure that one of the φ control signals is de-asserted before the other can be asserted.

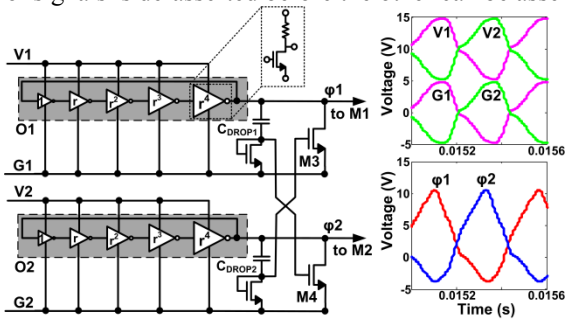

Fig. 3: Coupled oscillators generate non-overlapping control signals.

During φ1, V1/G1 are raised compared to V2/G2, as in the simulation waveforms of Fig. 3. When φ1 is de-asserted by the inverter-delayed path (O1), M4 is switched off; the correct voltage levels required to control M4 are achieved through C_{DROP1}. This causes φ2 to be asserted, allowing V2/G2 to rise (due to the switching of M1/2). Then, φ1 is held low through control of M3 (with the correct voltage levels set by C_{DROP2}).

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Analysis and Optimization

With the power inverter outputs oscillating to $\pm V_{OP}$ (as desired), the output power to the load, assuming a regulated load voltage (V_{LOAD}) and an oscillator frequency of f_{OSC}, is

$$P_{LOAD} = I_{OUT}V_{LOAD} = 2(V_{OP} - V_{LOAD})C_T f_{OSC} V_{LOAD}, \quad (1)$$

and the power drawn from S1/2 by the power inverter is

$$P_{INVERTER} = I_{OUT}V_{OP} = 2(V_{OP} - V_{LOAD})C_T f_{OSC} V_{OP}. \quad (2)$$

The power-inverter efficiency is thus the ratio V_{LOAD}/V_{OP}. In an energy-harvesting system, however, the output power is typically a more important metric; P_{LOAD} is optimized at $V_{LOAD}=V_{OP}/2$, as can be seen from (1).

Additional power is consumed by the coupled oscillators, whose static current is set by the pull-up resistors. Resistor values are chosen based on desired frequency and the stage capacitances of the NMOS devices, which are ultimately sized to drive the load capacitances of the power switches ($C_{M1/2}$). From simulation, an optimal stage up-sizing factor (r) of 1.6 is chosen. The resulting oscillator power is given by

$$P_{OSC} = kC_{M1/2} f_{OSC} V_{OP}, \quad (3)$$

(with k as a scaling constant), and overall efficiency is thus given by

$$\eta = \frac{2(V_{OP}-V_{LOAD})C_T f_{OSC} V_{LOAD}}{2(V_{OP}-V_{LOAD})C_T f_{OSC} V_{OP} + kC_{M1/2} f_{OSC} V_{OP}}. \quad (4)$$

Fig. 4 shows the effect of scaling C_T and f_{OSC}, from analysis and simulation (for simulation, we create Level 61 SPICE models from fabricated TFTs). In order to increase η, C_T must be increased; as indicated in (1) and (4), this permits higher output power without increasing P_{OSC}. Raising f_{OSC} does not affect η, until the point where M1/2 can no longer fully charge the outputs to $\pm V_{OP}$; the analytical model shown accounts for this. f_{OSC} should thus be increased to this point for highest output power. As shown in Fig. 4, however, the maximum harvested power (P_{LOAD}) achievable is limited ultimately by the saturation current of the M1/2 power switches. Further output power requires up-sizing M1/2. This also increases P_{OSC}, thus cancelling the effect on η.

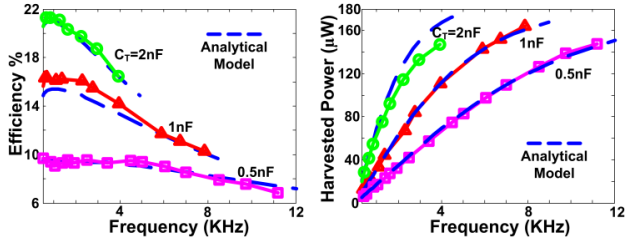

Fig. 4: Efficiency and output power versus oscillator frequency.

Thin-film Processing

Fig. 5 shows the structure of the a-Si NMOS TFTs and integrated resistors (used in O1/2). The TFT channel length is 6μm, and the layout is optimized for minimum gate-source/drain capacitance. Measured I-V curves for a typical TFT are shown.

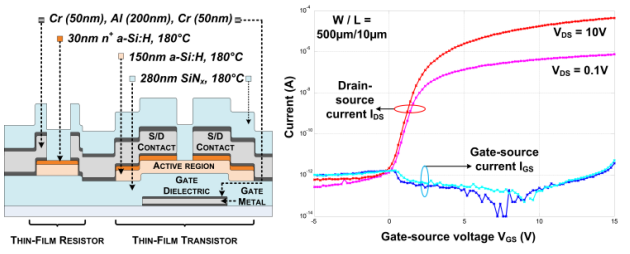

Fig. 5: Low-temp. processing of a-Si resistors and NMOS TFTs.

The resistors use an n+ doped 30nm a-Si layer, which also serves to form Ohmic TFT source/drain contacts; the resulting sheet resistance is 90MΩ/sq. Fabrication is achieved by plasma-enhanced chemical vapor deposition at low temperature (180°C), enabling deposition on flexible 50μm-thick polyimide foil [4]. Metal layers use chrome-aluminum-chrome stacks to maintain electrical properties under flexing.

Measurement Results

The circuits are fabricated and combined with solar modules on a flexible polyimide foil (Fig. 6). Table I gives a summary, with power and efficiency quoted for C_T from 0.5nF-2nF.

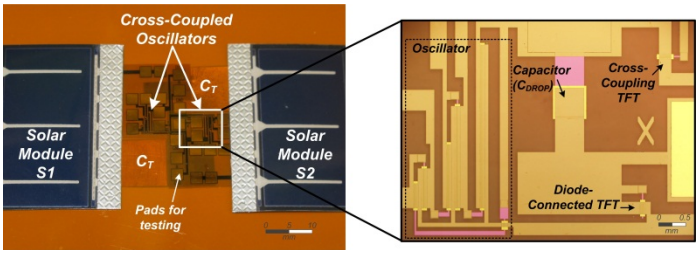

Fig. 6: System implementation on 50μm-thick polyimide foil.

Table 1: Summary of system performance

V_{OP} (V)	Solar Modules (cm^2)	Power Switch Size (μm)	f_{OSC} (kHz)	P_{OSC} (μW)	P_{LOAD} (μW)	η (%)
8.4	100	3600/6	4.5	336	47→120	11 → 22

As mentioned, for maximum power and efficiency the system should operate at the highest f_{OSC} that permits output charging to $\pm V_{OP}$; f_{OSC} is thus set to 4.5kHz. Fig. 7 shows the efficiency and output power for various C_T values, as V_{LOAD} is swept. V_{LOAD} is optimized at $V_{OP}/2$ for output power and slightly higher for efficiency. Fig. 8 shows the measured maximum efficiency and output power versus C_T, illustrating that efficiencies beyond 22% and output powers beyond 120μW are readily achievable.

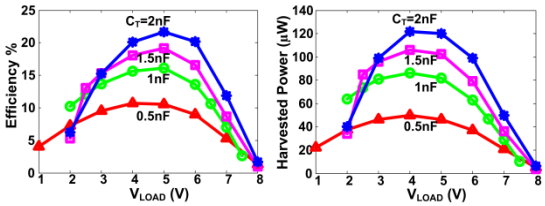

Fig. 7: Efficiency and output power versus V_{LOAD}.

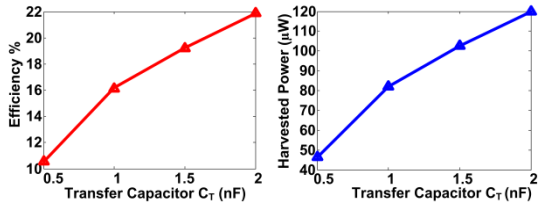

Fig. 8: Efficiency and output power versus C_T.

References

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