Transient phenomena in top-gate amorphous silicon thin film transistor with low-temperature self-aligned silicide source/drain and high mobility

Yifei Huang, Sigurd Wagner, James C Sturm
Electrical Engineering Department, Princeton University, Princeton, NJ 08544 USA
yhtwo@princeton.edu, wagner@princeton.edu, sturm@princeton.edu

Abstract

The transient response of top-gate amorphous silicon thin-film transistors with low-temperature self-aligned silicide source/drain contacts (no n^+ region) was examined. During TFT operation, a positive gate bias induces a high electron concentration in the a-Si active layer, which reduces the tunnel barrier thickness between the silicide source and the channel. This results in a low resistance ohmic contact, despite the lack of n^+ a-Si. Although the device DC mobilities are ~1cm^2/Vs, the TFTs require an abnormally long time to turn on (milliseconds). In this work, it is shown that the delay is associated with the application of bias voltage at the gate electrode, and the transient response strongly depends on duration of the bias pulse and temperature. The phenomena are manifestations of the gate-controlled turn-on of the silicide source to channel contact, and are qualitative explained with a model of defects on the sidewall of the gate insulator, discharging via surface conduction.

1. Introduction

In our previous work, we have demonstrated a top-gate α-Si TFTs with silicide source and drain (S/D) that are self-aligned to the edges of the gate [1]. The silicide S/D are formed directly on the intrinsic α-Si at low temperatures (280°C) compatible with flexible substrate, and the TFT structure contains no n^+ doped regions at all. Our self-aligned structure eliminates the parasitic S/D-to-gate overlap capacitance that adversely affects device performance in conventional bottom gate amorphous silicon TFTs. Furthermore, our results show that the DC performance of the top-gate a-Si TFT with self-aligned silicide S/D is comparable with that of bottom gate devices. The device structure and transfer characteristics are shown in Figure 1.

The nature of electron injection mechanism in our device is significantly different from that of the convention bottom gate TFT due to the lack of an n^+ layer. We have previously examined the injection mechanism through the lens of device contact resistance and found the contact resistance to decrease a function gate voltage, as shown in Figure 2 [2]. This was explained by the fact that positive gate bias induces a high electron concentration in the active a-Si, which reduces the tunnel barrier thickness between the silicide source/drain and the channel. The gate-voltage-controlled tunnel barrier thickness translates into the observed gate-voltage-dependent contact resistance. In this paper, we further examine the injection mechanism of electron from the silicide source into the channel by studying the transient response to the application of voltage pulses to the gate and drain electrodes.

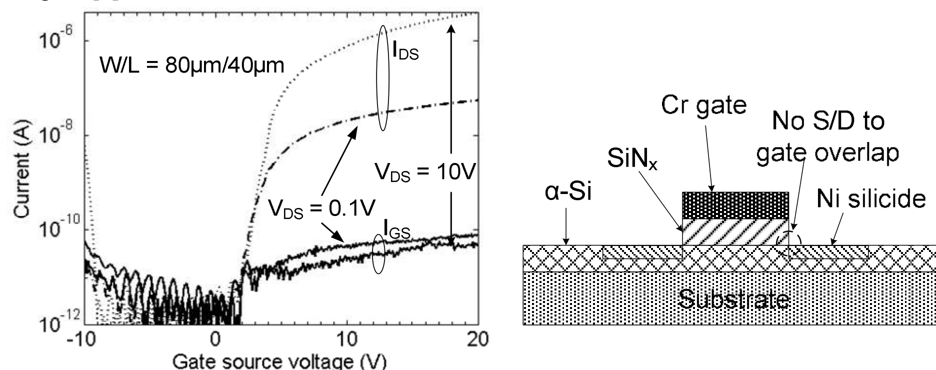

Figure 1. transfer characteristics (drain and gate current as a function gate voltage at two different drain biases) and device structure of the top-gate amorphous silicon TFT with self-aligned silicide S/D

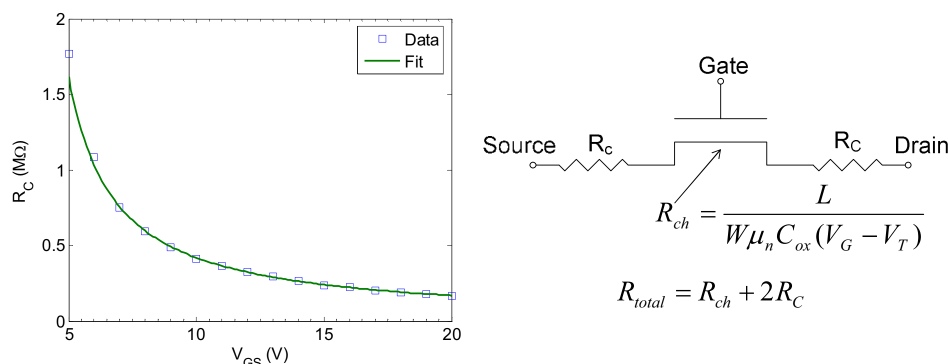

Figure 2. Contact resistance as a function gate-source voltage in the top-gate a-Si TFT with self-aligned silicide S/D (Contact resistance refers the parasitic resistance between the S/D contacts and the channel extracted using Transmission Line Model [2]

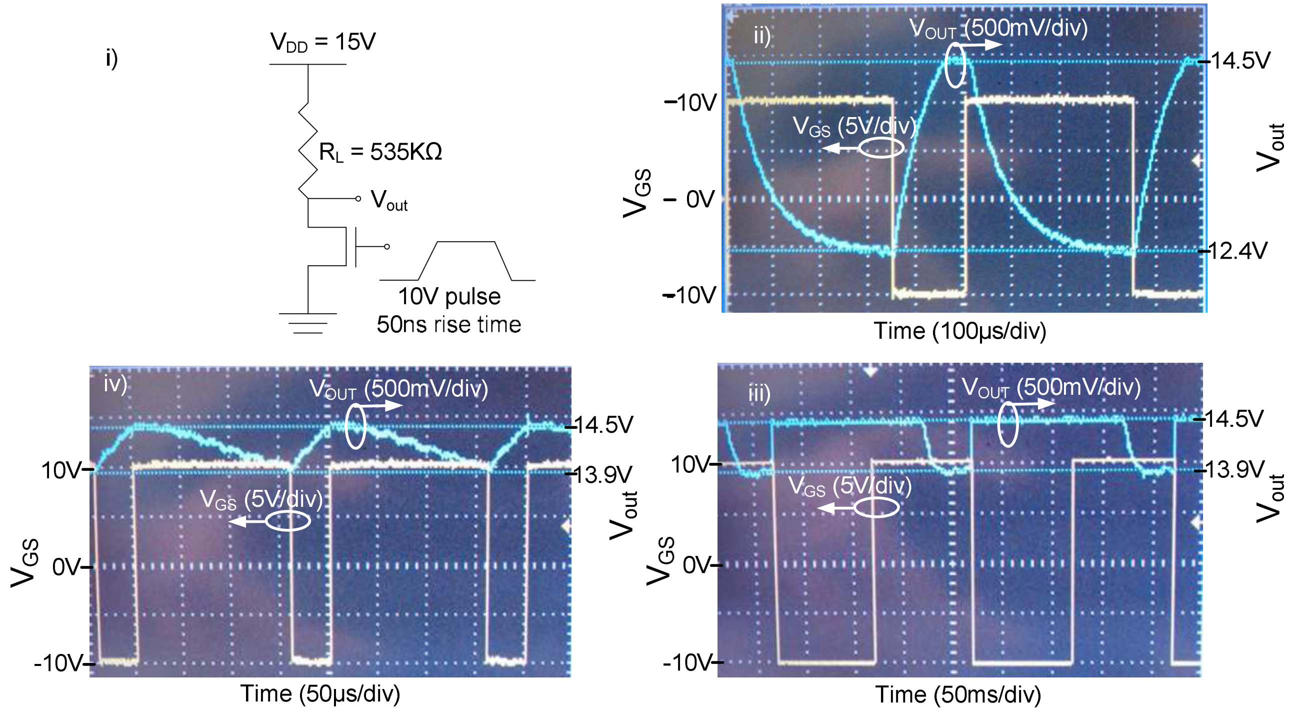

Figure 3. i) circuit used to measure the gate transient response of the TFTs, ii) transient response of a conventional bottom gate TFT, iii) transient of the top-gate TFT with long gate pulses, iv) transient of the top-gate TFT with short gate pulse

2. Results

2.1 Gate Transient

The gate transient response was measured with the setup shown in Figure 3.i. In the transient response of the top-gate a-Si TFT with self-aligned silicide S/D (Figure 3.iii), there is an abnormally long delay (~50ms) before the voltage at the node V_{out} changes in response to the applied gate voltage pulses, as indicated by the increase in drain current. This delay is absent in the transient response of the conventional bottom gate device (Fig. 3.ii). Since our top-gate TFT only differs significantly from the conventional device in its contact structure, the observed delay must be a result of the formation of ohmic contacts due to gate-voltage-induced reduction in tunnel barrier between the silicide source and the channel. This is consistent with the disappearance of the long delay when the applied gate pulse train has a high duty cycle (Fig 3.iv) (i.e. the device is turned off for only a short period of time). In this case we see the device turn on and off normally (microseconds), and no abnormal delays due to the effects of the contact (milliseconds).

2.2 Drain Transient

Drain transient responses were obtained with the same circuit by applying voltage pulses to the drain electrode while maintaining a fixed +15V DC voltage on the gate electrode (Figure 4.i). No abnormal delays were observed, and the transients of the top-gate and conventional TFTs were very similar in terms of time constants for device switching between ON and OFF (Figure 4.ii and 4.iii). This shows that the long turn-on time is indeed associated with a gate-controlled phenomenon, and not a drain-controlled one. Specifically, the delay in device turn-on is not associated with drain-field induced breakdown of the S/D-contact-to-channel electron injection barriers.

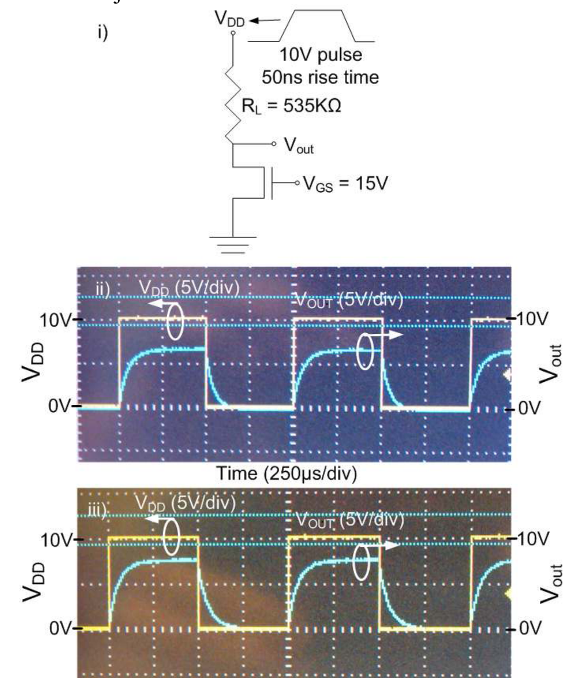

Figure 4. i) circuit used to measure drain transient response, ii) transient response of a conventional bottom gate TFT, iii) transient of the top gate TFT with self-aligned silicide S/D

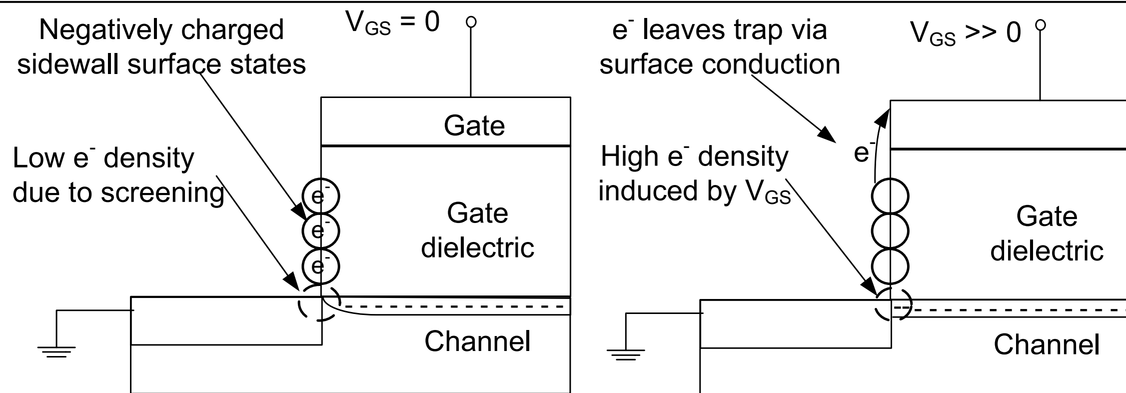

Figure 5. Sidewall defect state model

4. Model

The sidewall of the gate dielectric is formed by reactive ion etching and is unpassivated in the final device structure. There is likely a high density of the defect states on this surface. If these defect states were negatively charged, then they will screen the channel from the gate electric field. This reduces the electron concentration at the silicide-source-to-channel interface induced by the applied gate bias, which increases the thickness of the tunnel barrier to electron injection, resulting in high contact resistance. Upon the application of a positive gate bias to turn on the TFT, adsorbed moisture facilitates surface conduction of electron to the gate electrode (Figure. 5). As a result, the sidewall surface becomes neutral and the gate field can effectively turn on the contact. This is supported by the fact that the delay in the transient response first increases in duration as a function of increasing measurement temperature, then disappears all together. Adsorb moisture on the sidewall is reduced by increasing temperature, and since surface conduction is largely facilitated by the adsorbed moisture, there is a corresponding decrease in the current that discharges the sidewall surface defect states. This results in an increase in the delay in device turn on (lower discharging current means longer time required to discharge the sidewall), and when all the moisture de-adsorb from the sidewall, there is no longer any surface conduction to discharge the sidewall leading to the disappearance of the delay in device turn-on.

5. Conclusion

The transient response of the top-gate a-Si TFT with self-aligned silicide S/D was studied. These devices respond to gate voltage much slower than the conventional bottom gate TFTs, even though the DC performances are comparable. A model of dielectric sidewall discharging by surface conduction was proposed to explain the slow turn-on of the device. The results imply that the reduction of dielectric sidewall surface defect density via optimization of the reactive ion etching, dielectric properties and passivation on top of the gate insulator are the key to improving device performance.

6. Acknowledgements

The authors thank Professor Yvan Bonnassieux for arranging the review of this paper. The authors also acknowledge the United State Display Consortium for the support of this work.

7. References

[1] Y. Huang, B. Hekmatshoar, S. Wagner, J. C. Sturm, *Top-Gate Amorphous Silicon TFT With Self-Aligned Silicide Source/Drain and High Mobility*, Electron Device Letters, IEEE, Vol. 29, no. 7, pp. 737 – 739, July 2008

[2] Y. Huang, B. Hekmatshoar, S. Wagner, J. C. Sturm, *Electron Injection Mechanism in Top-gate Amorphous Silicon Thin-film Transistors with Self-Aligned Silicide Source and Drain*, Digest of the IEEE 66th Annual Device Research Conference, Santa Barbara, California June 2008