Amorphous Silicon Thin-Film Transistors with Low-Stress Silicon Nitride for Flexible Display

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ABSTRACT

We have developed low-defect, low-stress plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) at 200˚C. The intrinsic stress of this SiN_x film is only -12.9 MPa (compressive). Coupled with the low defect (low charge trapping) characteristic of this low-stress SiN_x, we are able to demonstrate amorphous silicon thin-film transistors (a-Si TFTs) with nearly threefold increase in mobility μ_e to 0.87 cm^2/Vs and 50% decrease in V_T to 2.8 V, compared to a control SiN_x. The low-stress a-Si TFT technology is amenable to flexible AMOLED and AMEPD display applications.

INTRODUCTION

Silicon nitride (SiN_x) is commonly used in thin-film transistor (TFT) backplanes as gate dielectric, isolating interlayer, and impurity barrier. Conventionally, SiN_x deposited on glass at 300-350˚C using plasma-enhanced chemical vapor deposition (PECVD) technique offers a low charge-trapping gate dielectric interface with amorphous silicon (a-Si) for commercial TFT-LCD flat-panel displays. Recently, as flexible active-matrix displays have caught much attention, [1] the technical challenge that must be met is accommodating thin film device layers on unconventional substrates, such as plastic foils. These foils typically are compatible with process temperatures of 200 ˚C or below, and one seeks both mechanical reliability and electronic performance. [2] One strategy involves the deployment of a new transparent plastic with a high glass transition temperature (T_g) for a 300-350˚C a-Si TFT fabrication process, with a demonstrated DC current lifetime over 100 years. [3] Alternatively, H_2 dilution during the PECVD of both a-Si ad SiN_x has improved TFT performance, due to the "in-situ" removal of weakly bonded Si atoms in a-Si during growth. [3,4] Furthermore, adding H_2 to the deposition of SiN_x also shows evidence of reducing the electron trap density in SiN_x and improving the quality of a-Si:H grown on top of it. [5,6] In this paper, we explore the latter strategy by comparing 200˚C SiN_x films with different H_2 and SiH_4-to-NH_3 gas compositions, in terms of interface defect density and mechanical stress. Furthermore, improved a-Si TFT performance with low-stress SiN_x is reported.

EXPERIMENT

A set of 200˚C PECVD SiN_x films were prepared on 4-inch p-type Si substrates for intrinsic stress measurements. "Recipe A" for 300-nm SiN_x film (SiN_x-A) corresponds to a precursor gas mixture of SiH_4, NH_3, N_2, and H_2 with a 1:4:16:18 gas ratio (46% H_2 dilution), resulting in an intrinsic film stress of -251.4 MPa (compressive) measured by the substrate curvature technique. "Recipe B" SiN_x (SiN_x-B) comprises SiH_4, NH_3, and H_2 with a 1:25:50 gas ratio (65% H_2 dilution) and an intrinsic stress of -12.9 MPa (compressive) for a 250-nm film. Metal-Insulator-Semiconductor (MIS) capacitors (in the inset of Figure 1) were fabricated on Generation 2 (G2) 370×470 mm^2 glass for 100-kHz capacitive-voltage (C-V) measurements of the two SiN_x films. The capacitors comprise MoW (100 nm) bottom electrode, SiN_x-A (300 nm) or SiN_x-B (250 nm) insulator, 90% H_2-diluted a-Si (200 nm) semiconductor, n^+ a-Si (50 nm) ohmic contact, and Ti/Al/Ti (50/100/50 nm) top electrode. Their charge-trapping densities were deduced from the plot areas enclosed by the hystereses in C-V curves.

Back-channel-passivated (BCP) a-Si TFTs on G2 glass using SiN_x-A as gate and passivation dielectric were contrasted with those using SiN_x-B. The TFT process flow was described elsewhere [7] with the process conditions and thicknesses substituted by those described in this report.

TEST RESULTS AND DISCUSSIONS

Intrinsic Film Stress

Mechanical stress of SiN_x is crucial for flexible display fabrication since it can induce self-roll-up of the flexible substrate, causing handling issues in manufacturing and product design. SiN_x films with high intrinsic stress are also susceptible to cracking or buckling on flexible substrate with poor thermal stability, leading to a high failure rate for the thin film devices. The intrinsic stress of SiN_x-B film is -12.9 MPa, which is only 5% that of SiN_x-A film (-251.4 MPa). Not only is the low stress of SiN_x-B film essential for ease of fabrication and design convenience for flexible displays, it also reduces excessive mechanical damages to the display with a flattened rollout. Furthermore, the low interface defect density of SiN_x-B in MIS capacitors and a-Si TFTs are discussed next.

C-V Measurements

Figure 2 illustrates the hysteresis in MIS capacitance due to charge-trapping at or near the SiN_x interface with a-Si. Capacitances for SiN_x-A and SiN_x-B are normalized to their maximum values at strong accumulation with 23.8 and 26.4 nF/cm^2, respectively. The clockwise direction of the hysteresis is indicative of negative (electron) charge trapping. Referring to the inset of Figure 1, it is possibly due to the electron transfer from a-Si accumulated at the interface to the deep traps in SiN_x, causing a positive threshold voltage (V_T) shift in a-Si TFT. [8] The magnitude of trapped charges (Q_{trap}) and trapped charge density (N_{trap}) can be estimated from the area enclosed by the hysteresis using these equations,

$$Q_{trap} \approx \int_{V_{bias}} \Delta C(V) dV \,, \qquad (1)$$

and, $N_{trap} = Q_{trap} / q$, with q = 1.6×10^{-19} C. (2)

The trapped charge densities for SiN_x-A and SiN_x-B are 1.1×10^{11} and 6.9×10^{10} cm^{-2}, respectively, a 36% lower charge trapping with the low-stress, H_2-diluted SiN_x. It is well known that H can passivate Si dangling bonds and promote strong Si bonds by breaking weak Si bonds and supplying the needed energy for strong bond formation. [3,4] Similarly, the hydrogen could reduce the number of trapping sites in the SiN_x. [5] The effect of SiN_x stress, however, is less clear. It may exert strain on a-Si at the interface, thereby breaking a certain amount of weak bonds in a-Si network without the accompanied "bond-healing" energy from H for Si bond reformation.

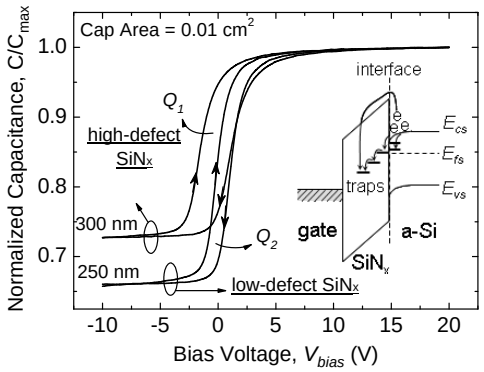

FIGURE 1. C-V curves for MIS capacitors with SiN_x-A (high defect) and SiN_x-B (low defect) films

I-V and On-Resistance Measurements

Figure 3 compares the I-V characteristics of BCP a-Si TFTs with SiN_x-A and SiN_x-B gate dielectric, respectively. Device mobility (μ_e), V_T, subthreshold slope (SS), and maximum gate current at V_{DS} = 10 V for SiN_x-A devices are measured to be 0.33 cm^2/Vs, 5.8 V, 1.67 V/dec, and 2.3 pA, in contrast with those for SiN_x-B devices of 0.87 cm^2/Vs, 2.8 V, 0.63 V/dec, and 2.55 pA. These results indicate that the lower interface defect density for the SiN_x-B devices is consistent with their low charge-trapping characteristic, yielding higher μ_e, lower V_T, steeper SS, and approximately one order of magnitude higher drive current than SiN_x-A devices in current saturation mode. Such an improvement is conducive to high brightness and contrast for current-driven display devices, e.g., organic light emitting diode (OLED).

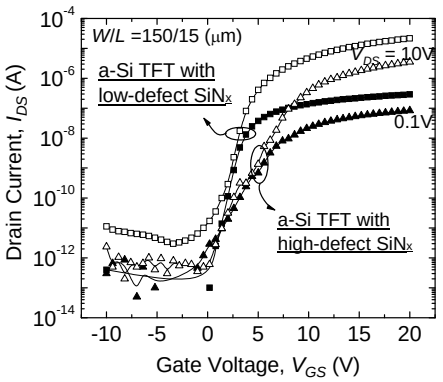

FIGURE 2. I-V characteristics of a-Si TFTs with SiN_x-A (high defect) and SiN_x-B (low defect) gate dielectric

On-resistance (R_{ON}) measurements for a family of TFTs with different channel lengths (L) and a fixed channel width (W) of 150 μm are shown in Figure 4. With V_{GS} = 40 V, the channel (R_{ch}) and contact resistances (R_{DS}) for SiN_x-A devices are 9.4 MΩ/□ and 0.24 MΩ, as compared to those of 4.2 MΩ/□ and 0.06 MΩ for SiN_x-B devices, respectively. Therefore, faster switching with shorter RC time constant for the latter is expected.

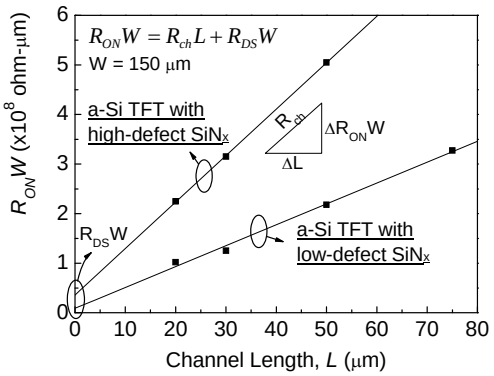

FIGURE 3. On-resistance of a-Si TFTs with SiN_x-A (high defect) and SiN_x-B (low defect) gate dielectric

CONCLUSIONS

We studied the low-stress 200°C SiN_x as a device dielectric layer from the standpoint of electrical stability in MIS capacitors and performance in a-Si TFTs. C-V measurements show low trapped charge density of $6.9x10^{10}$ cm^{-2} with this SiN_x, which yields a device mobility of 0.87 cm^2/Vs and V_T of 2.8 V when incorporating in a-Si TFT as gate and passivation dielectric. The channel and contact resistances of low-stress a-Si TFTs are also halved from those for high-stress devices. Studies on the compliance and reliability of these low-stress devices on flexible PI plastic foil are currently in progress.

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