Amorphous silicon floating-gate thin film transistor

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Amorphous silicon (a-Si) based memory devices have the potential to greatly expand the functionality of a-Si thin-film transistor (TFT) circuitry. Recently, an a-Si floating gate TFT (FGTFT) based memory element has been demonstrated, but the memory window was only 0.5V and the retention time was only ~1hour [1]. Furthermore, a-Si FGTFTs in general have a threshold voltage which depends on the drain voltage. In this work, we explore the effects of tunnel dielectric deposition condition and floating gate (FG) geometry on the performance of a-Si FGTFT. Through this analysis, we achieved a-Si FGTFTs with memory windows of >4V, room temperature retention times of >150hours and threshold voltages (V_T) which are independent of the drain voltage.

The structure of the a-Si FGTFT memory device is shown in Fig. 1 along with that of the standard TFT control device. The fabrication process of the memory element is similar to that of a standard bottom-gate back-channel-passivated a-Si TFT [2], with the addition of deposition and patterning of an a-Si floating gate layer. The device works based on electrons tunneling in/out of the FG controlled by gate voltage - no drain field or hot electron effects are involved. The FGTFT exhibits a V_T shift of ~4V after the application of a programming voltage of 32V to the control gate terminal, with the source and drain(S/D) terminals grounded, for 10ms. An erasing voltage of -50V on the control gate (S/D grounded) for 10ms forces the trapped electrons out of the floating gate and V_T returns to its pre-program value (Fig. 2). When the control device is subjected to the same cycle, no appreciable V_T shift is observed.

The quality of the tunnel dielectric material is crucial to the endurance and retention of floating gate memory devices, therefore the tunnel SiN_x in our devices is deposited using high temperature (~350°C) and high RF power (~210mW/cm^2) to maximize the film density and minimize defects. We use two different recipes for SiN_x deposition in our study - H_2 diluted SiN_x which uses $SiH_4/NH_3/H_2$ flow of 5/55/225sccm and N-rich SiN_x which uses SiH_4/NH_3 flow of 14/130sccm. The devices with H_2 diluted SiN_x can be programmed and erased at much lower voltages than those with N-rich SiN_x (Fig. 4&5). However, the retention time of the N-rich SiN_x devices are significantly better. Retention time ($T_{90\%}$) is defined as the amount of time it takes for 10% of the trapped electrons to leak out of the floating gate. Extrapolating high temperature data to 297K, we found $T_{90\%}$ of 150.8 hours and 38.9 hours for the N-rich and H_2 diluted SiN_x, respectively (Fig. 6). It was also found that the N-rich SiN_x has a higher activation energy (0.93eV) than the H_2 diluted SiNx (0.74eV). Data suggest that the H_2 diluted SiN_x has a higher defect density that facilitates electron tunneling (providing low voltage program/erase), while the N-rich SiN_x has a lower defect density that reduces leakage of charge trapped from the FG (providing better data retention).

The apparent V_T's are different for different drain voltages in FGTFTs (Fig. 7). This can be explained by the capacitive coupling of voltages between the floating gate and the drain terminals [3]. Further, by obtaining floating gate voltage via voltage transformation (Fig. 8), one can see that the turn-on voltage from the FG terminal is actually the same. By controlling the overlap between the floating gate and the drain, this effect can be eliminated all together (Fig. 9). This demonstrates that the geometry of the floating gate has dramatic impacts on device characteristics and is a key parameter in device optimization.

We have successfully fabricated a-Si FGTFT as memory elements. The memory window and retention time are the best ever reported for such devices. With respect to tunnel SiN_x, we found a trade-off between films with a higher defect density (allowing easier electron injection in/out of the FG) and those with lower defect density (having higher retention time). As for FG geometry, we found that V_T dependence on drain voltage can be eliminated by controlling the overlap capacitance between the drain and floating gate.

[1] Y. Kuo et al., *Applied Physics Letters*, vol 89, pp 173503-6, October 2006
[2] K. Cherenack et al., *IEEE Electron Device Letters*, Vol. 28, No. 11, pp. 1004-1006, NOVEMBER 2007
[3] S. T. Wang, *IEEE Transactions on Electron Devices*, Vol. ED-26, No. 9, pp. 1292-1293, September 1979

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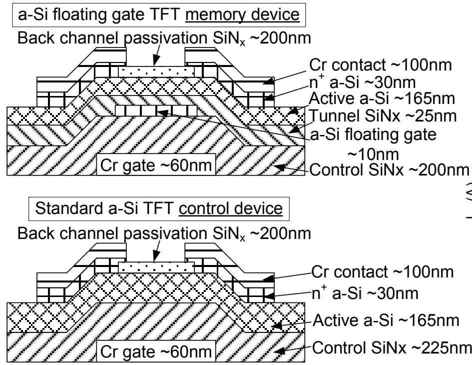

Figure 1. **Top**: structure of the a-Si floating gate TFT memory element. The floating gate is an intrinsic a-Si thin film patterned with RIE, and sandwiched between two SiN_x dieletric layers. **Bottom**: structure of the a-Si TFT control device, fabricated in the same way as the floating gate TFT without the floating gate layer. The total dielectric film thickness are the same in the two devices

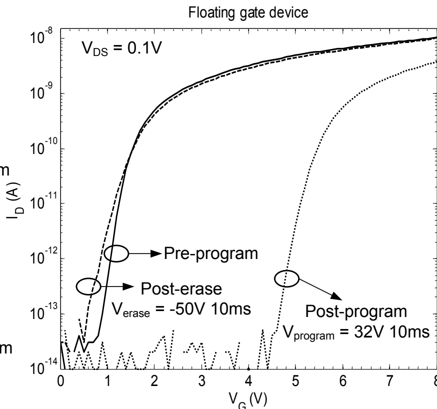

Figure 2. The DC transfer characteristics (V_{DS} = 0.1V & V_{GS} swept from 8V to 0V in 0.1V increment) of the FGTFT memory device at various stages of the program/erase cycle. Program: gate held at 32V with S/D grounded for 10ms; erase: gate held at -50V with S/D grounded for 10ms

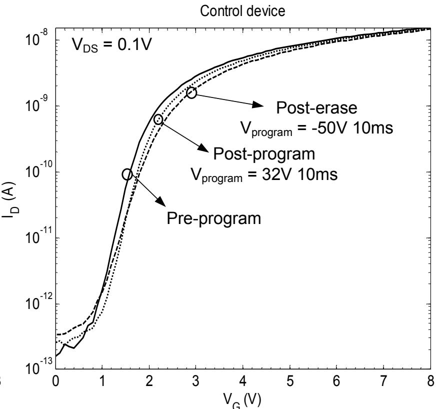

Figure 3. The DC transfer characteristics (V_{DS} = 0.1V & V_{GS} swept from 8V to 0V in 0.1V increment) of the control device at various stage of the program/erase cycle. Program: gate held at 32 V with S/D grounded for 10ms; erase: gate held at -50V with S/D grounded for 10ms

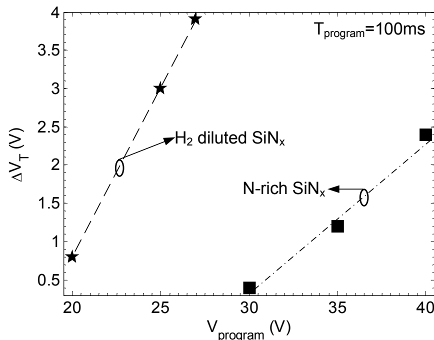

Figure 4. V_T shift dependence on amplitude of the programming voltage pulse for two different SiNx deposition recipes. $T_{program}$ = 100ms

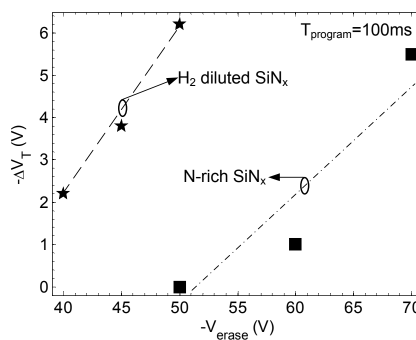

Figure 5. V_T shift dependence on amplitude of erasing voltage pulse (Both H_2 diluted and N-rich SiN_x are programmed such that V_T is approximately 6V) T_{erase} = 100ms.

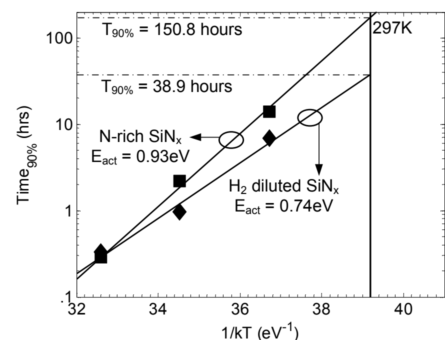

Figure 6. Arrenhius plot of retention times of the memory devices with H_2 diluted SiNx and N-rich SiNx. Retention time: the time for 10% of the trapped electrons to leak out. Measurements for retention time made at three different temperatures: 43°C, 63°C and 83°C in air ambient. Retention times for room temperature (T = 23°C) and the two activation energies were obtained by a linear fit to the measured data points.

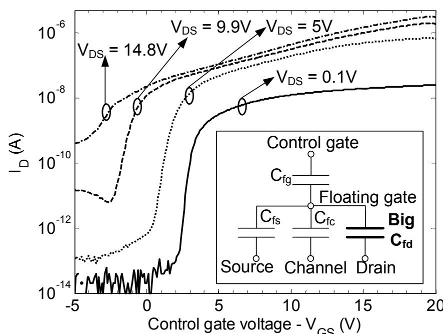

Figure 7. DC transfer characteristics of the floating gate TFT memory devices at four difference drain bias conditions. Capacitive coupling between the drain terminal and the floating gate causes an apparent V_T shift and high off current.

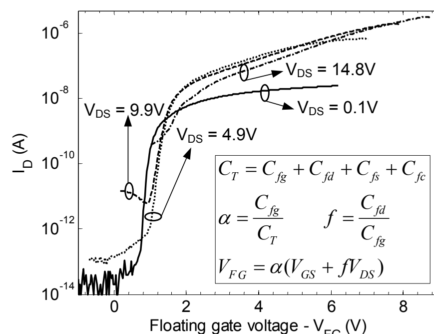

Figure 8. Drain currents of Fig. 7 versus floating gate voltage. The FG voltage was calculated using the capacitive coupling model of Fig. 7. The similar turn-on voltages as seen from the FG terminal show that the different V_T's in Fig. 7 can be explained by the voltage coupling between the drain and FG terminals

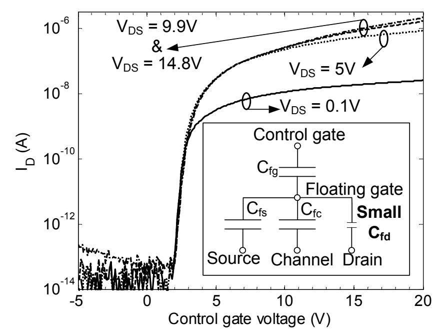

Figure 9. DC transfer characteristics of floating gate TFT memory device with reduced parasitic capacitance between the drain and the floating gate. No apparent threshold shift is observed.

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