Two-stage Model for Lifetime Prediction of Highly Stable Amorphous-Silicon Thin-Film Transistors under Low-Gate Field

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Highly stable a-Si TFTs reported recently with extremely long operating lifetimes under DC gate bias are attractive for analog drivers of the OLEDs in AMOLED displays [1]. At room temperature, the time for the DC saturation current to drop to 50% is predicted to be 100 to 1,000 years. However, the lifetimes were extrapolated with a stretched-exponential model for defect creation in a-Si, based on only month-long room temperature tests. In this study, we present a two-stage threshold voltage shift model for lifetime prediction from temperature dependent measurements. We find that (i) a "unified stretched exponential fit" models the drain current degradation from 60°C to 140°; and (ii) there is a second instability mechanism that initially dominates up to hours or days at low temperatures, so that tests conducted only at room temperature may not predict lifetime accurately.

Highly stable back-channel passivated (BCP) a-Si TFTs were fabricated with a standard bottom-gate non-self-aligned process. The TFTs were biased in the saturation regime with a constant gate voltage of 5V (a gate field of 2.0×10^5V/cm) and a constant drain voltage of 7.5V. The positive threshold voltage shift of a-Si TFTs under gate bias leads to reduced drain current and thereby reduced OLED brightness in AMOLED displays.

At low-gate field, electrons in the channel of a-Si cause weak Si-Si bonds to break into dangling bonds, and the resulting electron trapping raises the threshold voltage (Fig. 1) [1-3]. The density of weak bonds with barrier-to-break energy E_b is usually modeled with an exponential function $n(E) \propto e^{E_b/kT_0}$ [2], where the characteristic temperature T_0 reflects the density distribution in bond energy of weak bonds. Thus, the threshold voltage shift vs. time can be characterized with the stretched exponential expression [2], with weaker bonds breaking first and stronger bonds later, and exhibiting a strong temperature dependence.

With fixed gate and drain bias, we measured drain current vs. time at temperatures from 20°C to 140°C in steps of 20°C, with a fresh TFT measured at each temperature (Fig. 2). Through a "thermalization energy" $E_{th} = kT\ln(\nu t)$ [3] and the current-voltage equation in saturation, we show that a "unified stretched exponential fit" to normalized drain current degradation $I_{D,nor} \equiv \frac{I_D(t)}{I_D(t=0)}$ can be obtained [4] (Fig. 3), with $I_{D,nor}(E_{th}) = \exp\left\{-2\exp\left[\frac{E_{th}-E_{act}}{kT_0}\right]\right\}$. Combination with the expression for thermalization energy enables a three parameter (ν, E_{act}, T_0) fit of drain current vs. time (Fig. 2). The fit agrees well with the experimental data in the temperature range from 80°C to 140°C. At lower temperatures (20°C to 60°C), the drain current degradation approaches the model only at long times. The short time degradation suggests that a second instability mechanism contributes in the beginning (Stage I), in addition to the above model (Stage II).

By subtracting the threshold voltage shift of the "unified stretched exponential fit" from the total threshold voltage shift data at 20°C, one finds that the stage I mechanism is fast and saturates around 0.1V in ~10^3 seconds (Fig. 4). A two-stage fit by adding Stage I to Stage II agrees well with the experimental data of the threshold voltage (Fig. 4) and normalized drain current (Fig. 5) over the entire measurement time for all temperatures from 20°C to 140°C. Clearly, using 20°C data for times less than 10^6 seconds does not accurately predict long term (Stage II) performance.

In summary, the drain current degradation has a strong temperature dependence and therefore is accelerated by raising temperature. However, initial fast mechanism needs to be identified and separated from the mechanism that dominates stage II for accurate lifetime prediction. Such a two-stage model will enable engineers to determine a-Si TFT operating lifetimes and stability with much greater confidence.

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[2] R. S. Crandall, Phys. Rev. B, Vol. 43, pp. 4057 (1991)
[3] S. C. Deane et al., Phys. Rev. B, Vol. 58, No. 19, pp. 12625-12628 (1998)
[4] T. Liu et al., IEEE International Reliability Phys. Symp., pp. 2E.3.1 - 2E.3.5 (2011)

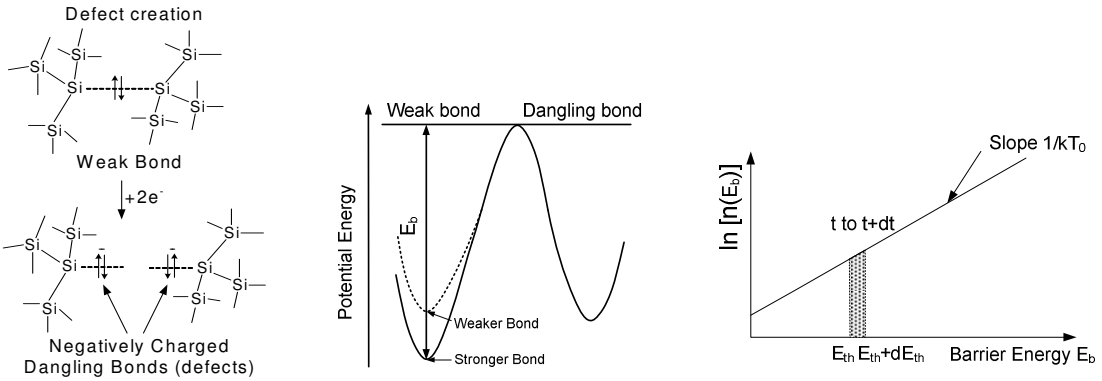

Fig. 1 Defect creation in a-Si TFTs. (a) Defect creation mechanism; (b) configuration coordinate diagram of defect creation and (c) density of weak bonds with barrier energy E_b modeled with $n(E) \propto e^{E_b/kT_0}$. From time t to $t + dt$, we approximate that weak bonds with barrier energies from E_{th} to $E_{th} + dE_{th}$ all break into dangling bonds (shaded area).

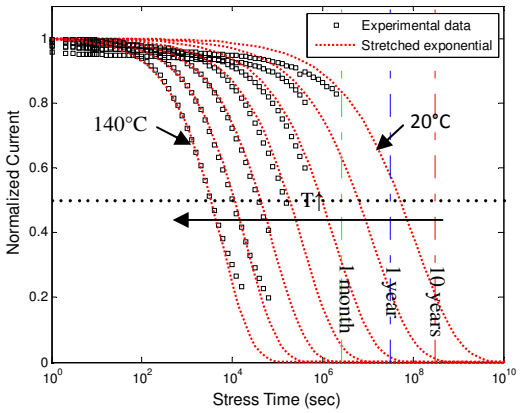

Fig. 2 Current degradation measured from 20°C to 140°C in steps of 20°C, and unified stretched exponential fit to experimental data.

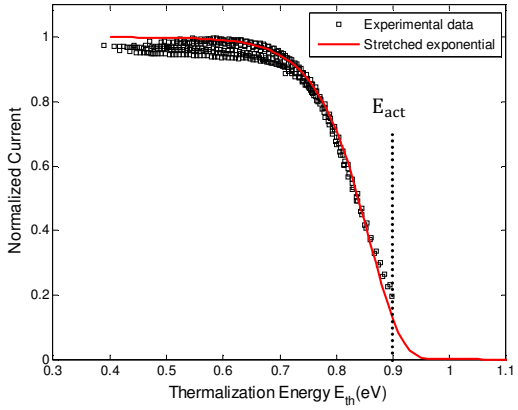

Fig. 3 Normalized drain current unified with thermalization energy $E_{th} = kT\ln(\nu t)$, where $\nu = 5\times10^6$ Hz, $E_{act} = 0.9$eV and $T_0 = 643$K.

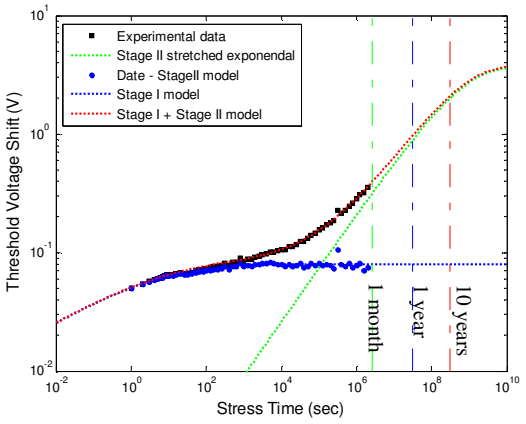

Fig. 4 Two-stage fit to threshold voltage shift vs. time at 20°C. The blue squares for Stage I "data" result from subtracting the Stage II model (determined by high temperature experiments) from the experimental data

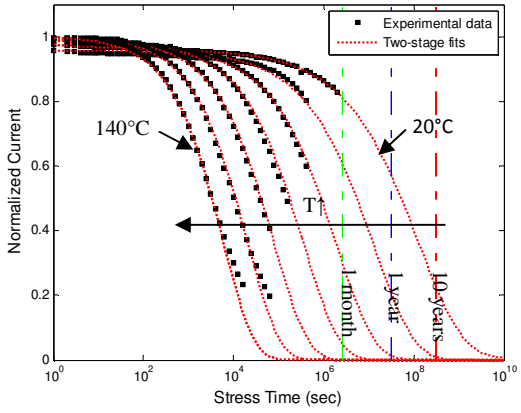

Fig. 5 Two-stage (Stage I + Stage II) fits to drain current degradation from 20°C to 140°C.