Electron Injection Mechanism in Top-gate Amorphous Silicon Thin-film Transistors with Self-Aligned Silicide Source and Drain

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The overlap between the source/drain (S/D) electrode and the gate electrode in conventional bottom-gate amorphous silicon (a-Si) thin-film transistors (TFTs), typically several μm, results in parasitic capacitance that negatively impacts the power and speed performance of a-Si circuits. Devices with S/D self-aligned to the gate do not suffer from this problem. However, self-aligned implementations of bottom-gate TFTs require lithographic exposure through the backside of the substrate, which uses nonconventional lithography tools and precludes the use of flexible substrates that are opaque in the UV range, such as metals and many plastics. Therefore, we propose, and demonstrate, a top-gate structure (Fig. 1), which achieves self-alignment by using the gate electrode to mask the silicide S/D formation. S/D contacts are formed directly on intrinsic a-Si (without doping) using a low-temperature (<280ºC) silicidation process that is compatible with flexible substrates [1]. Typical DC transfer and output characteristics of a Ni silicide S/D device are shown in Fig. 2 and Fig. 3, respectively. The devices exhibit a threshold voltage of 2.7V, saturation mobility of $1cm^2/Vs$, subthreshold slope of 600mV/dec and an ON/OFF ratio of $2x10^6$. These values are among the best ever reported for top-gate a-Si TFTs and comparable with that of the state-of-the-art bottom-gate devices.

In this abstract, we examine the nature of the electron injection from the silicide contact into the channel through the lens of contact resistance (R_c). We extract R_C by examining the total TFT resistance in the linear regime as a function of channel length for a range of V_{GS} values, Fig. 4 [2]. By extrapolating these curves to 0 channel length, we isolate the contact resistance from channel resistance at each of the V_{GS} values (Fig. 5). R_C is also separately and directly obtained by using a gated four-terminal device, shown in Fig. 6, to measure the voltages at nodes inside the channel during TFT operation [3]. The two results are in good agreement. To gain a semi-quantitative understanding of observed VGS dependence, we performed simulations to obtain the band diagram near the semiconductor surface from the silicide source to the channel (Fig. 7). The results show significant decreases in Schottky barrier thickness and no change (to first order) in Schottky barrier height with increases in V_{GS}. Thus we conclude that the electron injection mechanism must be tunneling.

Without correcting for the effect of R_C, the experimentally observed effective mobility decreases from $1cm^2/Vs$ at L=100μm to 0.65 cm^2/Vs at L=5μm while the observed effective threshold is independent channel length. This can be accurately modeled by incorporating the experimentally determined V_{GS}-dependent R_C into conventional MOSFET equations (Fig. 8). Thus, we conclude the threshold of the device is determined by the formation of the channel and not by effect of the contact as in conventional MOSFETs.

In summary, we have successfully demonstrated top-gate a-Si TFT with self-aligned nickel silicide S/D. We have shown, by examining R_C, the dominant electron injection mechanism is tunneling from silicide S/D to the channel. Further, we show that the contact resistance has no influence on device threshold and little effect on effective mobility down to L=5μm.

[1] K. Long, A. Z. Kattamis, I. C. Cheng, H. Gleskova, S. Wagner and J. C. Sturm, *IEEE Elec. Dev. Lett.*, Vol. 27, no. 2, pp. 111-113. Feb. 2006
[2] S. Luan and G. W. Neudeck, *J. App. Phys.*, vol. 72, no. 2, pp. 766-772, July 1992
[3] S.-D. Liu, A. Shih, S.-D. Chen, and S.-C. Lee, *Journal of Vacuum Science & Technology B*, vol. 21, pp. 677-682, 2003.

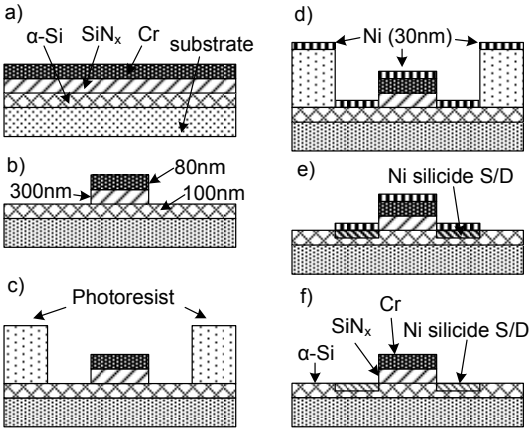


Fig. 1. Illustration of fabrication process: a) Deposition of TFT stack (α-si, gate dielectric, and gate metal); b)definition of gate electrode; c) definition of channel width electrical isolation of devices; d) blanket deposition of Ni; e) lift off and silicidation; f) selective removal of unreacted Ni

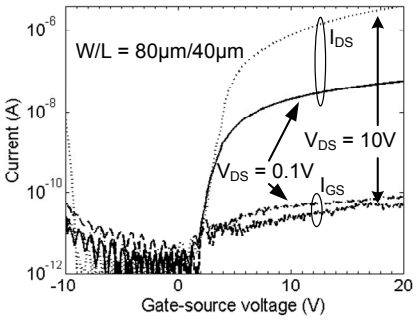


Fig. 2. Room-temperature transfer characteristics (drain current vs gate-source voltage for drain-source bias of 0.1V and 10V) of a top gate a-Si TFT with self-aligned nickel silicide source drain.

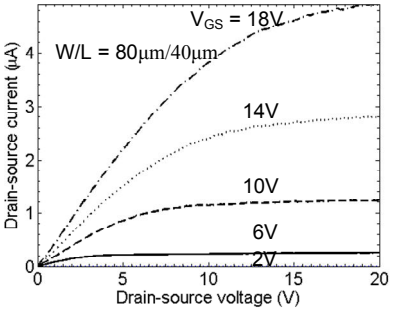


Fig. 3. Room-temperature output characteristics of a top gate a-Si TFT with self-aligned silicide source drains.

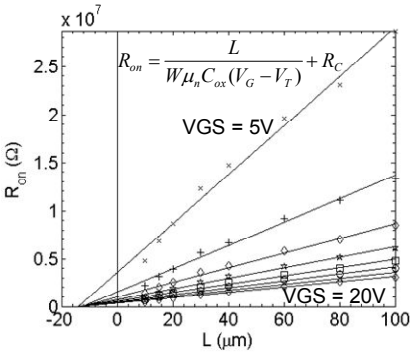


Fig. 4. Total device resistance in the linear regime (R_{ON}) as a function of channel length for V_{GS} ranging from 5V to 20V and fits to model for extracting R_C

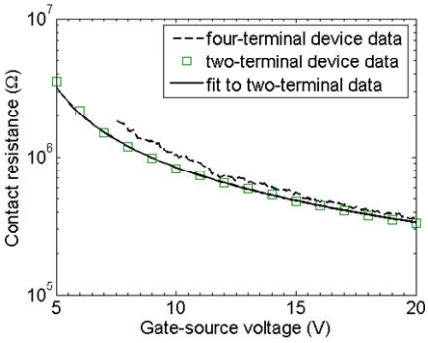
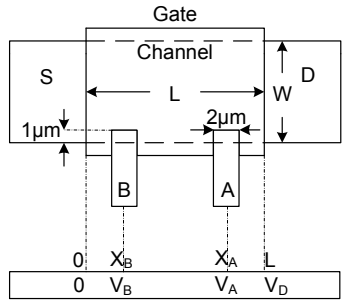


Fig. 5. Contact resistance vs VGS – two-terminal device data extracted using the approach shown in Fig. 4 and four-terminal device data measured using the approach shown in Fig. 6.



$$R_S = \frac{1}{I_{DS}}\left[V_B - \frac{(V_A - V_B)}{(X_A - X_B)}X_B\right]$$

$$R_D = \frac{1}{I_{DS}}\left[V_D - V_A - \frac{(V_A - V_B)}{(X_A - X_B)}(L - X_A)\right]$$

Fig. 6. Gated four-terminal device fabricated to directly measure the contact resistances. Probes A and B use the same type of contact as the S/D, and extend into the channel by 1μm.

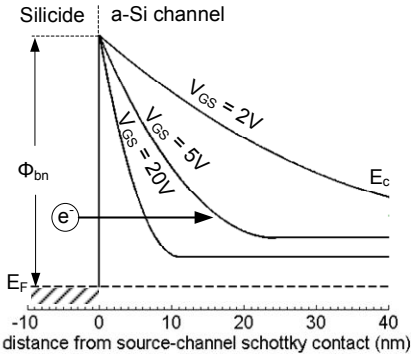


Fig. 7. Band diagram near semiconductor surface from source to channel. Increasing V_{GS} lowers conduction band and increases electron concentration in the channel, resulting in a thinner tunnel barrier to enable electron injection

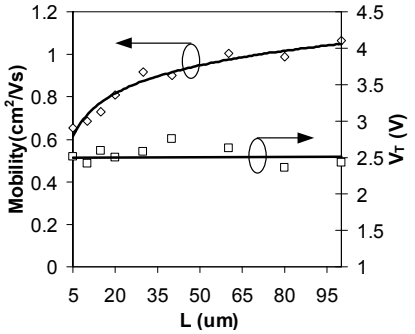


Fig. 8. Simulated and measured channel length dependence of effective mobility and threshold voltage. μ_{eff} is decreased by 30% from its long channel value at L = 5μm, V_T is unchanged.