Enabling Mechanisms for a-Si TFT's with 100-year Lifetimes Compatible with Clear Plastic Substrates

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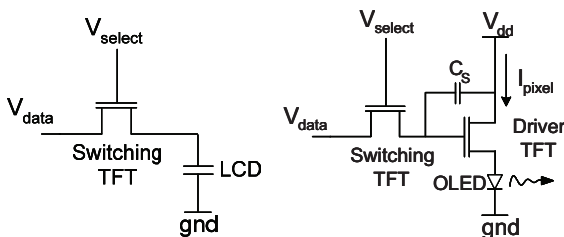sturm@princeton.edu
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Abstract

Amorphous silicon (a-Si) TFTs typically have a large positive voltage shift vs. time, leading to a decrease in current at fixed voltages. This prevents the realization of active matrix OLEDs using a-Si TFTs unless complicated correction circuits are used. In this abstract, we show that by addressing the underlying mechanisms behind the drift, the time for the current to drop by 50% under DC conditions consistent with OLED pixel brightness in excess of 1000 cd/m^2 can be extended from one month to over 100 years. This is longer than the luminance lifetime of OLEDs themselves. Furthermore, we show the fabrication of such TFTs is compatible with novel clear plastic substrates.

1.   Introduction

Amorphous silicon TFTs are the workhorse of today's flat panel display industry, which is approaching $100B/yr in economic value. A current outstanding question is which TFT technology will be used for future manufacturing of AM OLED displays, both on glass and then on flexible substrates. If a-Si TFTs can meet the AMOLED technical requirement, it will be highly attractive because of the existing large installed manufacturing base for a-Si TFTs, because new investments for a new technology would not be required.

The technical requirements of the TFT for AMOLED pixels are much more demanding that those for AMLCD pixels. The TFT in AMLCD pixels operates only as a digital switch to transfer the data voltage to an effective storage capacitor. Further, it operates typically for one row time out of each frame time, corresponding to a duty cycle on the order of 0.1%. Thus they are fairly tolerant to instabilities in the TFT.

AMOLED pixels have at least two TFTs. One is the TFT for capturing the data from the data column line, which operates similarly to the TFT in AMLCDs. For this TFT, threshold voltage shifts are not critical. However, a second TFT is required to convert the data voltage into a current through the OLED. This TFT operates in analog mode – any changes in its gate-source voltage directly translate to changes in current and thus to pixel brightness. Further, the OLED and this transistor operate in DC, so it is most likely to have its threshold voltage rise (compared to a device with 0.1% duty cycle). Reducing the magnitude of this threshold voltage shift   to improve the TFT stability is the focus of this paper.

2.   Current and Bias Points for AMOLEDs

The rate of increase of the threshold shift in a-Si TFTs is well known to increase with increased gate voltage [1]. Thus one must establish an appropriate current and bias level for TFTs before device stability can be established. Two-transistor AMOLED test arrays using the pixel design of Fig. 1(b) were fabricated both on glass and clear plastic using a-Si TFTs fabricated between 250 and 300 ^{o}C. Phosphorescent OLEDs were deposited after the TFT fabrication, with an efficiency of 55-60 cd/A. For large test pixels of 500 um x 500 um, a W/L for the driver transistor of 30 was used. Fig. 2 shows the pixel current and average areal pixel brightness as a function of the gate-source voltage applied to the driver TFT.

(a)

(b)

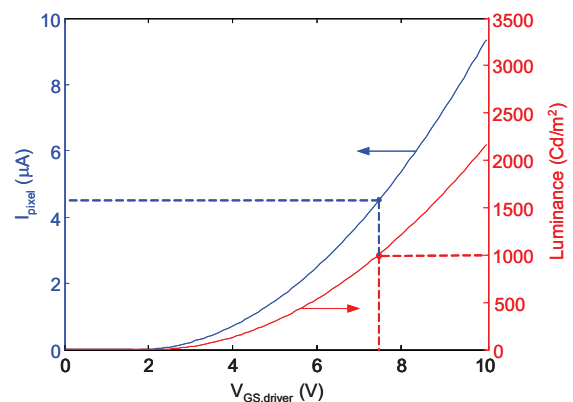Fig. 1.   Schematic pixels for (a) AMLCD and (b)

Fig. 2.   Pixel current and average areal pixel brightness as   a function of gate-source voltage on the driver TFT. A system polarizer loss of 50% was assumed, so the actual emission brightness was twice that on the right vertical axis.   The TFT was in saturation.

Fig. 2 shows that a brightness of 1000 cd/m^2 (2000 cd/m^2 before a polarizer) can be achieved at a gate-source voltage of 7.5 V, corresponding to a current level of 4.5 uA.   The gate insulator was 300 nm of silicon nitride. For more typical pixels of 100 um x 100 um, the current level would be only ~0.2 uA, which could be achieved at the same bias level (7.5V) using W/L ~ 1.   Thus a gate-source bias level of 7.5 V was chosen for subsequent transistor stability tests.

3.   Mechanisms of TFT Threshold Voltage Shifts

The threshold voltage in a-Si TFTs typically rises because of two mechanisms: the trapping of electrons in the gate dielectric, and the creation of defects through Si-Si bond breaking (and trapping of electrons at those defects) in the a-Si. [1,2] (Fig. 3).   These mechanisms may be distinguished in practice by their different dependence on time and gate voltage.

The trapping of electrons in the gate nitride has been well studied and typically has a logarithmic time dependence   [3]. It increases sharply with gate voltage as the higher gate field leads to more electrons in the channel and more tunneling into the nitride.
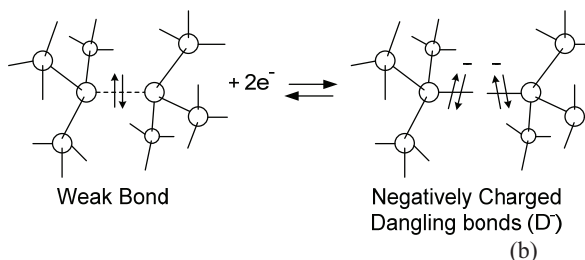
(a)

(b)
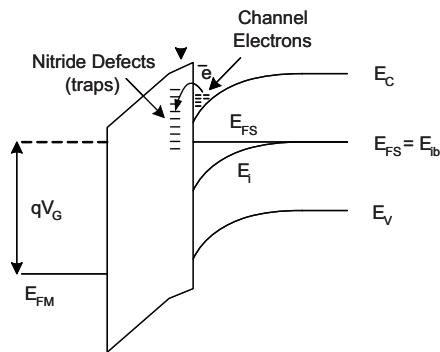
Fig. 3.   Mechanisms of electron trapping leading to increased threshold voltage of (a) trapping of channel electrons in the gate nitride and (b) bond-breaking in the a-Si and subsequent trapping of channel electrons.

Amorphous silicon contains many strained Si-Si bonds. In the presence of a high electron density, it is energetically favorable for some of these bonds to break, since the resulting defect states offer a lower energy for electrons than the relatively high conduction band of the channel.   Higher gate voltages (and more electrons in the channel) also lead to increased defect formation in the amorphous silicon and thus higher threshold voltage as electrons are trapped.   Because of the range of bond energies, this mechanism typically has a "stretched exponential" dependence on time [4], which may be approximated at short times by a power law relation [5].

By fitting the threshold voltage shift vs. time, the dominant mechanism (trapping in the gate nitride or defect formation in the amorphous silicon) can be distinguished.

4.   Improvements in Stability

Fig. 4 shows the normalized current (current divided by initial current) for a-Si TFTs biased in DC operation in saturation at the bias levels described in Sect. 2 of this paper for bright pixel operation (gate-source voltage of 7.5V.   The current decreases as a function of time as electrons are trapped in the gate or in the a-Si.   The Princeton TFTs were fabricated using a conventional bottom-gate process with gate nitride deposited from silane and ammonia, and amorphous silicon deposited using a silane, all by PECVD.
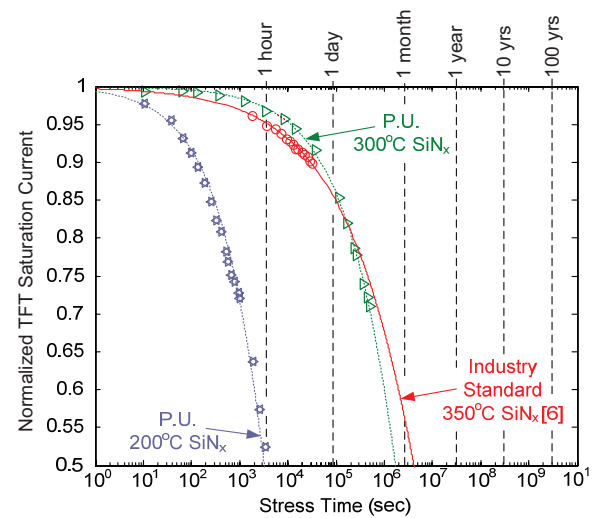
Fig. 4.   Normalized current for Princeton TFTs (PU) fabricated at process temperatures of 200 and 300 ^{o}C , and a similar "standard" TFT at 350 ^{o}C [6].   The TFTs were operated in saturation a gate-source voltage of 7.5V.

At a process temperature of 200 ^{o}C, the poor quality of the gate dielectric led to a rapid increase in threshold voltage. Within one hour, the threshold voltage had risen by 1.2V, corresponding to a 50% decrease in the pixel current.   This decrease would correspond to a 50% decrease in brightness in an AMOLED.   Raising the process temperature to 300 ^{o}C, more typical of industrial AMLCD processes, resulted in a slower trapping rate, increasing the 50% lifetime by three orders of magnitude to 1 month.   This lifetime is probably still insufficient for a display product.   A similar lifetime could be inferred from threshold shift data for a "standard" process with a 350°C process from the literature [6].

The TFTs fabricated at 300 ^{o}C were then analyzed to determine the dominant charge trapping mechanism at various gate voltages and times.   The corresponding space of gate voltage (gate field) vs. time was divided into regions according to the dominant mechanism (Fig. 5).   The measurement paths at the 30 V and 7.5V gate-source voltage condition are indicated as horizontal lines in Fig. 5, labeled "high field" and "low field" respectively.   For the low-field condition representative of AMOLED operation (7.5 V gate-source voltage), after a brief initial transient, the dominant instability mechanism was found to be defect formation in the amorphous silicon.   In our experience, increasing the process temperature beyond 250-300 ^{o}C did not increase the quality of

amorphous silicon. Therefore a different approach was required to further increase the TFT stability.
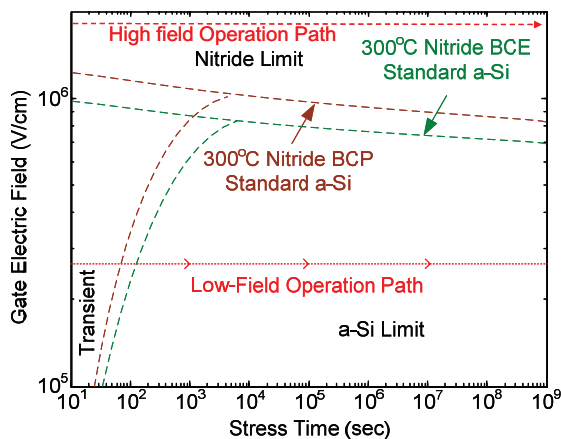

Fig. 5. "Phase Diagram" of space of gate field vs stress time showing dividing lines between different dominant mechanisms of threshold voltage shift of "initial transient," "nitride limit," and "a-Si limit." Data is given for two different TFT processes (BCE and BCP), both with a nitride deposition temperature of 300 °C. Nitride was deposited from ammonia and silane, and a-Si was deposited from silane at 250 °C.

In the "a-Si limit" region of Fig. 5, the breaking of Si-Si bonds is though to be the dominant mechanism of the threshold voltage shift. Because of the amorphous nature of the material, there are a range of bond energies. We hypothesize that the weakest of these bonds are the ones which break first and contribute to the shift in threshold voltage. Thus we seek a way to reduce the number of "weak" bonds in the a-Si.

This was accomplished by adding hydrogen to the silane during the a-Si deposition process [7]. Atomic hydrogen is known to be able to etch silicon under PECVD conditions by breaking Si-Si bonds to form volatile hydrides. Thus the addition of hydrogen to the PECVD process to deposit a-Si could remove weak Si-Si bonds as they are formed, resulting in a final film with fewer weak Si-Si bonds. With such a process, the TFTs were indeed more stable, and the 50% lifetime increased by two orders of magnitude to ~10 years (Fig. 6). The gate nitride process was unchanged. Note that actual measurements were only conducted for times up to one month. By fitting the models for the dominant threshold voltage shift over that time, extrapolations were made to predict threshold voltage and thus current for longer time [7].

Examining these highly stable transistors showed that the rate of defect formation in the amorphous silicon was so low that electron trapping in the gate nitride was an important factor in limiting the lifetime to 10 years. We recently showed that by increasing the nitride temperature to 350 °C, the nitride trapping could be reduced, so that lifetimes over 100 years could be achieved [8]. These are generally well in excess of the 50% luminescent decay times of OLED's at the brightness levels corresponding to the TFT currents (~1000 cd/m^2). Thus the TFT stability is no longer a limiting factor in the fabrication of realistic pixels for products.

Because of the high temperature, a 350 °C process is not attractive for processing on plastic. Therefore the SiNx process at 300 °C was modified to achieve a similar reduction
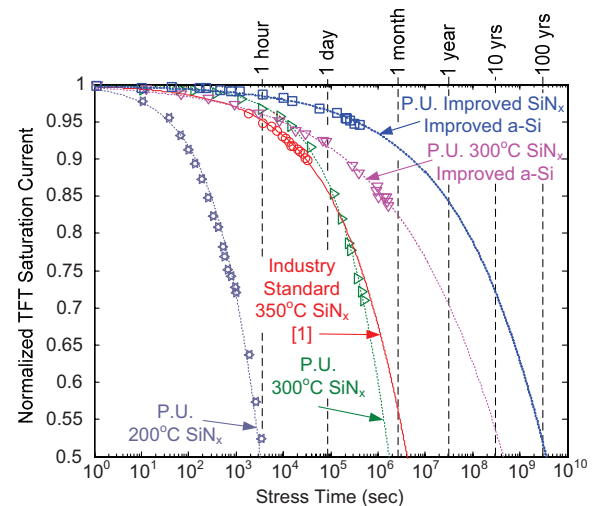

Fig. 6. Normalized current for TFTs of Fig. 4 (at bias level of Fig. 4), for a TFT with the same nitride as the "300 °C PU SiNx" device but with a-Si deposited at 250 °C with hydrogen dilution ("improved a-Si). Also shown is a data device with the same "improved a-Si", but with an improved SiNx process at 300 °C.

in the trapping to achieve 100-year devices with a 300°C maximum process temperature. Such a temperature is compatible with TFT fabrication on clear plastic substrates (next section).

5. TFT's and Pixels on High-Temperature Clear Plastic for Flexbile Displays

The best and most mature OLED processes use bottom light emission, through a transparent anode and then through a glass substrate. Therefore for flexible OLED's displays, a clear plastic substrate is needed. It should be capable of 300 °C processing to take advantage of the 100-year TFT lifetimes. Typical clear plastic substrates such as PET and PEN have glass transition temperatures below 200 °C, limiting their process temperature. Some polyimides such as Kapton ® have a glass transition temperature in excess of 300 °C, but these substrates are orange and thus not suitable for displays which require transparent substrates.

Furthermore, the inorganic materials in the TFT stack (a-Si, SiNx, metals, etc) have low coefficients of thermal expansion (CTE) (generally < 10 ppm/K). Many plastic substrates have a thermal expansion coefficient which is much larger, for example ~50 ppm/K. Thus a large compressive stress builds up in the TFT stack after deposition as the substrate cools. This large stress must be sustained by the interface between the plastic substrate and the SiNx barrier layer on the plastic (under the TFT itself). As the thickness of the inorganic layers builds up, eventually cracks will form to relieve the compressive stress in the inorganic films.

Fig. 7 shows the thickness of the SiN which can be deposited under certain conditions on a plastic substrate with a 50 ppm/K CTE before cracking occurs. Note that the maximum thickness without cracking decreases as the deposition temperature increases, a signature that the integrated stress in the films due to the thermal mismatch is limiting the allowable thickness without cracks [8]. At 250 °C, a thickness of only 200 nm could be deposited without cracks. Given that the gate nitride alone is typically 300 nm, this

shows that TFTs could not be fabricated on these substrates at 250 ^{o}C or higher.   Thus the limit to the fabrication temperature was not the glass transition temperature, but rather the mismatch in thermal expansion coefficients.
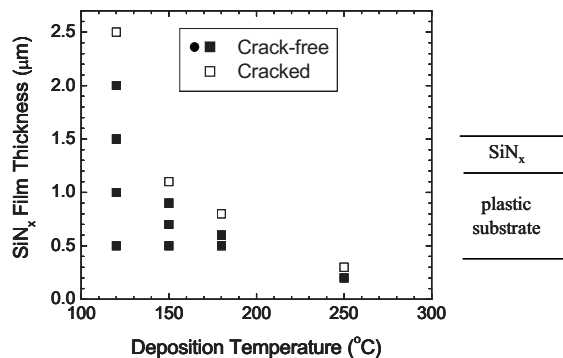

Fig. 7.   Resulting SiNx condition (cracked or crack-free) for deposition of SiN by PECVD at various temperatures and thicknesses on clear plastic substrates with CTE of 50 ppm/K [9].

Our collaborators at the DuPont company then supplied us with novel plastic substrates which were clear across the visible spectrum, had a glass transition temperature in excess of 300 ^{o}C, and a CTE of only ~10 ppm/K. This enabled SiNx layers over 1 micron thick to be deposited successfully without cracks from 250 to 280 ^{o}C, compared to 200 nm at similar temperatures on substrates with a higher CTE.

The clear plastic substrates with low CTE and high glass transition temperatures allowed the fabrication of high quality TFTs on clear plastic substrates from 280 up to 300 ^{o}C [2, 7, 10] (Fig. 8).   Typical mobilities were $0.8 - 1$ cm^2/Vs and threshold voltages were $1.5 - 2.5$ V.   There was no systematic difference between TFTs fabricated on glass vs the clear plastic substrates, either in DC operating parameters or stability.

6.   Summary
By improving the quality of both the nitride and the amorphous silicon, the 50% current lifetime at bias levels appropriate for AMOLED pixels can be extended from ~1 month to over 100 years under DC operation.   This can be achieved with conventional fabrication equipment at temperatures of 300 ^{o}C or less.   The TFT fabrication of these highly stable TFTs is compatible with novel clear plastic flexible substrates, which combine a high glass transition temperature with a low coefficient of thermal expansion.
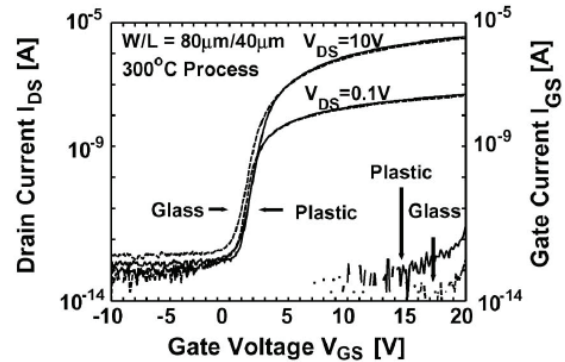

Fig. 8.   Comparison of characteristics of a-Si TFT's fabricated on glass and clear plastic at 300 ^{o}C.

7.   Acknowledgements

8.   References
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