# 65.1: *Invited Paper:* Amorphous Silicon TFT's with 100-year Lifetimes in a Clear Plastic Compatible Process for AMOLEDs

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## Abstract

We demonstrate critical elements of a-Si technology on clear plastic for flexible AMOLED applications. First, we show that a-Si TFT's with gate voltages under 5 V provide sufficient current for OLED pixel brightness of over 1000 cd/m<sup>2</sup>, with minimum geometries (W/L = 1) for 100  $\mu$ m × 100  $\mu$ m pixels. Critical to this result is a clear plastic with the combined properties of high transparency, glass transition temperature in excess of 300 °C, and low coefficient of thermal expansion. Second, we show that by engineering the a-Si TFT stack, under the bias conditions for pixel operation, the "half-life" of the TFT (defined as the time for the current to fall by 50% in DC operation) is 10 years for a 280 °C process on clear plastic, and at least 100 years for 300 °C. This is several orders of magnitude higher than that of common a-Si TFT processes and in general larger than the lifetimes for the 50% decay of the luminescence of the OLED's themselves. Finally, we provide a framework demonstrating the tradeoff between drive current and TFT stability.

### 1. Introduction

The large amorphous silicon (*a*-Si) TFT industry was largely developed for AMLCD's on glass. The TFT's themselves operate with low duty cycle (~0.1%) and only in a digital switching mode (Fig. 1(a)), so that the requirement for the stability of the TFT is not very severe. Future AMOLED operation (Fig. 1(b)) on flexible plastic is much more demanding, requiring DC operation including analog mode. The gate voltage on the driver TFT translates the data voltage into current for the OLED and thus pixel brightness. Changes in the TFT characteristics over time will thus affect the image quality, and the stability of the devices has been a major concern. Process compatibility with plastic is also of great interest for flexible applications.

# 2. TFT Technology and OLED Drive Conditions

The stability of a-Si TFT's is well known to decrease with increasing gate-source voltage [1-4]. Thus there is a trade-off



Fig. 1. Schematic pixels for (a) AMLCD and (b) AMOLED.

between a high drive current from the TFT (high gate-source voltage) and high stability (low gate-source voltage). The drive current part of this problem was investigated by integrating green phosphorescent OLED's onto test pixel arrays (as in Fig. 1(b)) using a-Si TFT's on glass and clear plastic [5, 6]. Plastic substrates were first coated with a silicon nitride (SiN<sub>x</sub>) buffer. The TFT's were fabricated using a standard bottom-gate process in a plasma-enhanced chemical vapor deposition (PECVD) process, with a gate nitride of 300 nm unless otherwise noted. Good pixel uniformity and yield were observed (Fig. 2) under QVGA timing. Fig 3(a) shows current (and average pixel brightness) vs. gate-source voltage on the driver transistor. An average pixel brightness of 2000 cd/m<sup>2</sup> (500  $\mu$ m × 500  $\mu$ m pixels) required a current of 4.5  $\mu$ A for W/L = 30. This was achieved at a gate voltage of 7.5 V for 300 nm SiN<sub>x</sub> ( $2.5 \times 10^5$  V/cm gate field) or 1.6 V for 50 nm  $SiN_x$  (Fig. 3(b)), and corresponds to the same voltage at W/L = 1 for a pixel of 100  $\mu$ m × 100  $\mu$ m. This gate voltage condition (7.5V on 300 nm SiN<sub>x</sub>) was chosen for subsequent stability tests.

# 3. TFT Stability

#### 3.1. Degradation Mechanisms

The main source of degradation in our TFT's was an increase in the threshold voltage with time. The change in mobility was less than 5%, even for current drops as large as 50%. The threshold voltage in *a*-Si TFTs typically rises because of two mechanisms: the trapping of electrons in the gate dielectric, and the creation of defects through Si-Si bond breaking (and trapping of electrons at those defects) in the *a*-Si. [1–4]. These mechanisms may be distinguished in practice by their different dependences on time and gate voltage.

The trapping of electrons in the gate nitride has been well studied and typically has logarithmic time dependence [1, 2]. It increases



Fig. 2. Checkerboard image of test pixel array of OLED pixel test array using *a*-Si TFT's, with QVGA timing [6].



Fig. 3. (a) Measured pixel current and average areal pixel brightness as a function of gate-source voltage on the driver TFT. A system polarizer loss of 50% was assumed, so the actual emission brightness was twice that on the right vertical axis. The TFT was in saturation. (b) Comparison of drive currents (in saturation) vs. gate voltage for TFT's with 300 and 50 nm SiN<sub>x</sub> thickness.

sharply with gate voltage as the higher gate field leads to more electrons in the channel and more tunneling into the nitride. This mechanism typically dominates at high gate fields, such as those which occur in AMLCD operation.

Amorphous silicon contains many strained Si-Si bonds. In the presence of a high electron density, it is energetically favorable for some of these bonds to break, since the resulting defect states offer a lower energy for electrons than the relatively high conduction band of the channel. Higher gate voltages (and more electrons in the channel) also lead to increased defect formation in the amorphous silicon and thus higher threshold voltage as electrons are trapped. Because of the range of bond energies, this mechanism typically has a "stretched exponential" dependence on time, which may be approximated at short times by a power law relation [3, 4]. By fitting the threshold voltage shift vs. time, the dominant mechanism (trapping in the gate nitride or defect formation in the amorphous silicon) can be distinguished. This mechanism has a weaker dependence on gate voltage than the

tunneling mechanism, and thus often dominates at low gate voltages.

### 3.2. > 100-year Lifetimes

Fig. 4 shows the normalized current (current divided by initial current) for *a*-Si TFT's biased in DC operation in saturation (as in pixel operation) at the bias levels described in Sect. 2 of this paper for bright pixel operation (gate-source voltage of 7.5V). The current decreases as a function of time as electrons are trapped in the gate or in the *a*-Si. We define a "lifetime" as the time required for the current to decrease to 50% of its original value, which would lead to a 50% decrease in brightness. We choose this point since the lifetime of OLED's is similarly defined as the time required for the brightness to decay to 50% of its initial value (under fixed current operation).

At a process temperature of 200 °C, the poor quality of the gate dielectric led to a rapid increase in threshold voltage. Gate trapping dominated even for the low gate voltage conditions. Within one hour, the threshold voltage had risen by ~1.5V, corresponding to a 50% decrease in the pixel current. Raising the process temperature to 300 °C, more typical of industrial AMLCD processes, resulted in a slower trapping rate, increasing the 50% lifetime by three orders of magnitude to one month. A process with back-channel SiN<sub>x</sub> passivation had marginally better performance than the one with an etched and exposed back channel. The baseline Princeton process at 300 °C used an a-Si channel deposited from PECVD using pure silane, and the nitride was deposited using a combination of silane and ammonia. The one-month lifetime is probably still insufficient for a display product. A similar lifetime could be inferred from threshold shift data for a "standard" process with a 350 °C process from the literature [7].

The Princeton TFT's fabricated at 300 °C were then analyzed to determine the dominant charge trapping mechanism at various gate voltages and times. The corresponding space of gate voltage



Fig. 4. Normalized current for *a*-Si TFT's (at bias level of 7.5V  $V_{GS}$ ) fabricated under different conditions. With the same nitride as the "300 °C PU SiN<sub>x</sub>" device but with *a*-Si deposited at 250 °C with hydrogen dilution ("improved *a*-Si"). Also shown is a data device with the same "improved *a*-Si", but with an improved SiN<sub>x</sub> process at 300 °C.



Fig. 5. "Phase diagram" approach showing the dominant drift mechanisms in a space of gate electric field and DC stress time. Specific measurement paths are shown for both high and low gate voltages. Maps for both the "standard" and "improved *a*-Si" process conditions are shown.

(gate field) vs. time was divided into regions according to the dominant mechanism (Fig. 5). The measurement paths at the 30V and 7.5V gate-source voltage conditions are indicated as horizontal lines in Fig. 5, labeled "high field" and "low field" respectively. At high fields (e.g. above 30V gate voltage), electron trapping in the gate nitride was responsible for most of the drift. For the low-field condition representative of AMOLED operation (7.5 V gate-source voltage), after a brief initial transient, the dominant instability mechanism for the baseline ("standard *a*-Si") process was found to be defect formation in the *a*-Si. Increasing the process temperature beyond 250-300 °C did not increase the quality of *a*-Si.

In the "*a*-Si limit" region of Fig. 5, the breaking of Si-Si bonds is though to be the dominant mechanism of the threshold voltage shift. Because of the amorphous nature of the material, there is a range of bond energies. We hypothesize that the weakest of these bonds are the ones which break first and contribute to the shift in threshold voltage. Thus we seek a way to reduce the number of "weak" bonds in the *a*-Si.

This was accomplished by adding hydrogen to the silane during the a-Si deposition process [8]. Atomic hydrogen is known to be able to etch silicon under PECVD conditions by breaking Si-Si bonds to form volatile hydrides. Thus the addition of hydrogen to the PECVD process to deposit a-Si could remove weak Si-Si bonds as they are formed, resulting in a final film with fewer weak Si-Si bonds. In the extreme case, such a process is well known to result in microcrystalline and not amorphous silicon. However, our conditions were chosen to yield a material which was still predominately amorphous silicon. With such a process, the TFTs were indeed more stable, and the 50% lifetime increased by two orders of magnitude to ~10 years (Fig. 4) on glass or clear plastic. The gate nitride process was unchanged. Note that actual measurements were only conducted for times up to one month. By fitting the models for the dominant threshold voltage shift over that time, extrapolations were made to predict threshold voltage and thus current for longer time [8].

Examining these highly stable transistors showed that the rate of defect formation in the amorphous silicon was so low that electron trapping in the gate nitride was again an important factor in limiting the lifetime to 10 years, even for gate voltages of only 7.5V. We recently showed that the nitride process can be improved at either 300 or 350 °C, so that extrapolated lifetimes over 100 years could be achieved [9, 10]. Data and extrapolation for the 350 °C process is shown in Fig. 4; data for the 300 °C improved process is similar. These 100-year lifetimes are generally well in excess of the 50% luminescent decay times of nearly all OLEDs. Thus the stability of the amorphous silicon may no longer be a limiting factor in the fabrication of realistic pixels for products.

#### 3.3. Framework for Technology Comparison

Changing TFT structural parameters such as the gate insulator thickness will change both the TFT current and the rate of degradation. This makes comparing different designs difficult. Further, other TFT technologies may have very different mobilities, etc. As a framework to compare different technologies for TFT stability, consider the choices faced by the circuit designer. The circuit designer cares about the channel resistance (in ohms/square). This determines the drive current of the TFT and what W/L is necessary to achieve a given current. Second, the circuit designer cares about the stability of the device (time for current to decay by a certain percentage). Both of these will be affected by choices such as gate voltage, insulator thickness, semiconductor (a-Si, organic, etc). Thus one can consider a "space" of lifetime vs. channel sheet resistance (Fig. 6(a)). A "good" technology will be in the upper left hand side of the figure (high lifetime and low sheet resistance). Conversely, a "poor" technology will be in the lower right. For a given technology, increasing the gate voltage will move it towards the left (lower channel sheet resistance) and also possibly down (lower lifetime). High mobility will move a technology to the right and a poor gate dielectric moves it down.

For data, we chose a "90% lifetime" (corresponding to only a 10% reduction in current) for such a chart — a more severe definition than the 50% definition used earlier. This was done because data in the literature is more easily available for less change in current, and so that less extrapolation of data is required. Figure 6(b) shows data for several of our TFT technologies at Princeton. Plotted as a vertical line is a desired design point of a channel sheet resistance so that a driver TFT of W/L = 1 can be used in a pixel of size 100  $\mu$ m × 100  $\mu$ m to achieve a pixel brightness of over 1000 cd/m<sup>2</sup> (as in Fig. 3).

One notes that at high gate voltages the sheet resistance decreases and the lifetime decreases, as expected. At low gate voltages and high channel sheet resistances, the lifetime saturates and becomes constant. These two regimes can be shown to correspond to dominant threshold shift mechanisms of trapping in the gate nitride and defect creation in the amorphous silicon, respectively.

#### 4. Integration on Plastic

Conventional <u>clear</u> plastics have two limits for processing at the elevated temperatures (250 °C and above) required for high *a*-Si TFT lifetimes: low glass transistion temperatures (generally under 200 °C) and high coefficients of thermal expansion. Novel plastics have been developed which allow both a glass transistion temperature in excess of 300 °C and a CTE under 15 ppm/K, and which are still clear throughout the visible spectrum. These plastics allow *a*-Si TFT's to be fabricated at temperatures as high as 300 °C [5, 11, 12]. No differences in TFT performance or lifetime are seen on glass vs. plastic.



Fig. 6. (a) Framework for technology comparison of lifetime vs. channel sheet resistance, and effect of main device/material parameters on lifetime vs. sheet resistance tradeoff. (b) Measured data for various *a*-Si TFT processes at Princeton. Note a 90% lifetime (10% current degradation) is used. The general trend is lower lifetimes and lower sheet resistances at high gate voltages, with lifetime saturating at low gate voltages.

#### 5. Summary

Amorphous silicon TFT's are promising candidates for realizing AMOLED pixels on either glass or plastic substrates. They can provide sufficient currents to drive bright OLED's even with low gate voltages, and the lifetime of the TFT's under DC operation exceeds that of virtually all OLED materials.

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#### 7. References

- M. Powell, C. van Berkel, J. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors", Appl. Phys. Lett. 54, 1323-1325 (1989)
- [2] Y. Kaneko, A. Sasano, T. Tsukada, "Characterization of instability in amorphous silicon thin-film transistors", J. Appl. Phys. 69, 7301-7305 (1991)
- [3] F. R. Libsch, J. Kanicki, "Bias-stress-induced stretchedexponential time dependence of charge injection and trapping in amorphous thin-film transistors", Appl. Phys. Lett. 62, 1286-1288 (1993)
- [4] J. Kakalios, R. Street, W. Jackson, "Stretched-exponential relaxation arising from dispersive diffusion of hydrogen in amorphous silicon", *Phys. Rev. Lett*, 59, 1037-1040 (1987)
- [5] B. Hekmatshoar, A. Kattamis, K. Cheranack, K. Long, J. Chen, S. Wagner, J. Sturm, K. Raman, M. Hack, "Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays With Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic", IEEE Elect. Dev. Lett. 29, 63-66 (2008)
- [6] B. Hekmatshoar, A. Kattamis, K. Cherenack, S. Wagner, J. Sturm, "A Novel TFT-OLED Integration for OLED-Independent Pixel Programming in Amorphous-Si AMOLED Pixels", J. Soc. Info. Display, 16, 183-188 (2008)
- [7] S. Karim, A. Nathan, M. Hack, W. Milne, "Drain-bias dependence of threshold voltage stability of amorphous silicon TFTs", IEEE Elect. Dev. Lett. 25, 188-190 (2004)
- [8] B. Hekmatshoar, K. Cherenack, A. Kattamis, K. Long, S. Wagner, J. Sturm, "Highly Stable Amorphous-Silicon Thin-Film Transistors on Clear Plastic", Appl. Phys. Lett. 93, 032103 (2008)
- [9] B. Hekmatshoar, K. Cherenack, S. Wagner, J. Sturm, "Amorphous Silicon Thin-Film Transistors with DC Saturation Current Half-Life of More than 100 Years", Tech. Digest Int. Elec. Dev. Mtg. 89-92 (2008)
- [10] B. Hekmatshoar, K. Cherenack, Y. Huang, S. Wagner, J. Sturm, "100-Year Low-Gate-Field Half-Life of Amorphous-Si Thin-Film Transistors with a Plastic-Compatible Modified Gate Nitride Process", Mat. Res. Soc. Spring Meet. (2009)
- [11] K. Long, I-C. Cheng, A. Kattamis, H. Gleskova, S. Wagner, J.C. Sturm, "Amorphous-silicon thin-film transistors made at 280 degrees C on clear-plastic substrates by interfacial stress engineering," J. Soc. Info. Display, 15, 167-176 (2007)
- [12] K. Cherenack, A. Kattamis, B. Hekmatshoar, J. Sturm, S. Wagner, "Amorphous-Silicon Thin-Film Transistors Fabricated at 300 °C on a Free-Standing Foil Substrate of Clear Plastic," IEEE Elect. Dev. Lett. 28, 304-306 (2007)