Analytical Model of Apparent Threshold Voltage Lowering Induced by Contact Resistance in Amorphous Silicon Thin Film Transistors

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The interest in amorphous Si (*a*-Si) thin-film transistors (TFT's) has increased recently due to active matrix organic light emitting diode (AMOLED) display applications. Unlike active matrix liquid crystal display (AMLCD) applications where the TFT only charges a capacitor, the DC driving requirement in AMOLED's makes the source/drain series resistance and modeling of current in saturation very important. It is well-known from Si VLSI MOS technology that the presence of the drain/source contact resistance lowers the driving current and as a result the "apparent" mobility extracted from the electrical characteristics is lower than the "true" mobility especially at short channel lengths [1]. Amorphous Si TFT's have a much larger series resistance than VLSI FET's because in addition to the metal/n^+ contact, *a*-Si which is a low conductivity material also contributes to the contact resistance. This is because in the TFT structure, the metal/n^+ contact is on top of the a-Si film while the channel is at the bottom. In this abstract, we (i) show that this series resistance causes a large lowering of the "apparent" threshold voltage when it is extracted by conventional methods, and (ii) develop an analytical model to explain this effect. The model is supported by experimental data at different channel lengths and series resistances.

Conventionally, the apparent mobility and threshold voltage of a FET are extracted by plotting the square root of the saturation current versus the gate voltage and a least square fit (LSF) calculation is performed to approximate the square root of the drain current with a straight line. Fig. 1 shows that the values of apparent threshold voltage extracted by this method are lower at shorter channel lengths and higher contact resistances. To explain this behavior, we first assume that the contact resistance in a-Si TFT's is a constant voltage-invariant resistance as in MOSFET's. Also, in our model, we assume that a-Si TFT's are described by MOS I-V characteristics, which is a relatively good approximation for hydrogenated a-Si TFT's. As shown in Fig. 2, an LSF to the saturation regime of the MOS-based characteristic results in an apparent threshold voltage and mobility which are lower than their true values. However, the actual a-Si TFT problem is more complicated, since the contact resistance is not constant, and has a gate-voltage dependent series component that results from the presence of a-Si beneath the metallurgical junction [2] as shown in Fig. 3 for a typical inverted-staggered a-Si TFT. The extracted values of contact resistance for our test TFT's are plotted in Fig. 4. It is observed that both components of the contact resistance increase with decreasing the overlap between the gate and drain/source. By direct application of the MOS equation (the model given in Fig. 2) it can be shown that the gate-voltage dependent component of the contact resistance lowers the apparent mobility but does not change the apparent threshold voltage. By adding this effect, the apparent mobility and threshold voltage can be evaluated analytically. This model is given in Fig. 5 and compared with the experimental I-V curves for two different contact resistance values. Fig. 6 shows the variation of the apparent threshold voltage as a function of contact resistance for different channel lengths. In Fig. 7, the model is compared with the experimental I-V curves to show that changing the drain bias changes the extracted apparent threshold voltage and mobility by changing the saturation to linear transition point and therefore changing the range over which the LSF is calculated. Finally, the variation of the apparent threshold voltage is plotted versus the channel length in Fig. 8 and compared to the experimental data at two different drain biases.

In summary, we have shown that in a-Si TFT's the apparent threshold voltage extracted by conventional methods is lowered by the presence of the source/drain contact resistance, especially at short channel lengths and the analytical model presented to explain this effect is in good agreement with the experimental data. This model is particularly useful for AMOLED applications where the contact resistance has a crucial role in determining the driving current and thus the brightness of the pixels.

[1] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits,* 3rd Edition, John Wiley & Sons, New York, NY 1993
[2] S. Luan and G. W. Neudeck, *J. Appl. Phys.* vol. 72, no. 2, July 1992, pp. 766-772

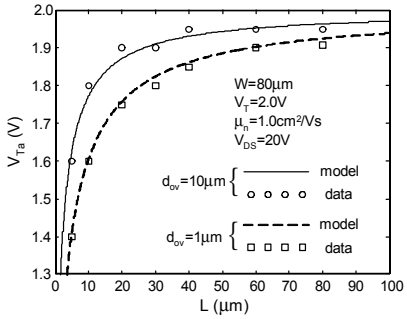
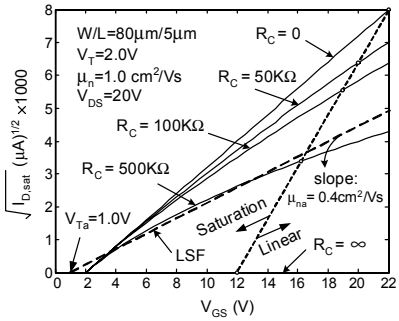
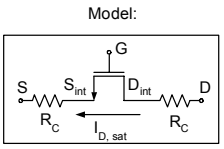


Fig.1. Apparent threshold voltage (V_{Ta}) extracted from test TFT's using the conventional method, for several channel lengths (L) and two gate to drain/source overlap lengths, d_{ov} (see Fig. 3). The shorter d_{ov} corresponds to the higher contact resistance. It is observed that V_{Ta} is lower at shorter L and also lower for higher contact resistance (shorter d_{ov}).



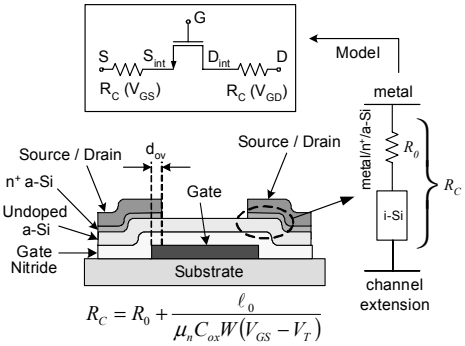


$$\begin{cases} V_{GS,int} = V_{GS} - R_C I_{D,sat} \\ V_{DS,int} = V_{DS} - 2R_C I_{D,sat} \end{cases}$$

$$I_{D,sat} = k_n (V_{GS,int} - V_T)^2,\ k_n = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$$

$$I_{LSF} = k_{na}(V_{GS} - V_{Ta})^2,\ k_{na} = \frac{1}{2}\mu_{na} C_{ox}\frac{W}{L}$$

Fig.2. Plot of the square root of the saturation current in a FET for several values of contact resistance R_C, when the current is calculated by a simple FET model plus R_C at the source and drain. Using a least square fit (LSF) to estimate the current results in an apparent threshold voltage (and mobility) that is lower than its true value, i.e. $V_{Ta} < V_T$ (and $\mu_{na} < \mu_n$), as shown for $R_C = 500\text{K}\Omega$. The LSF is calculated (and the result is valid) only where V_{GS} is low enough (for a given V_{DS}) to ensure saturation. The saturation to linear transition point occurs at $V_{DS,int} = V_{GS,int} - V_T$.



$$R_C = R_0 + \frac{\ell_0}{\mu_n C_{ox} W (V_{GS} - V_T)}$$

Fig.3. Cross-section of an inverted-staggered a-Si TFT. The contact resistance R_C is composed of a metal/n$^+$Si/a-Si metallurgical junction and an a-Si region beneath that junction. The latter component makes R_C gate-voltage dependent [2].

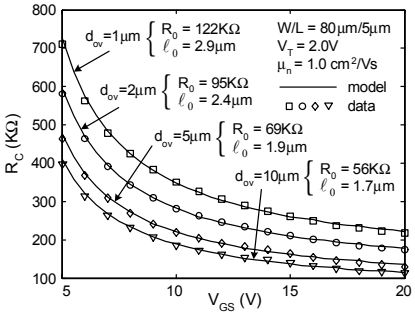
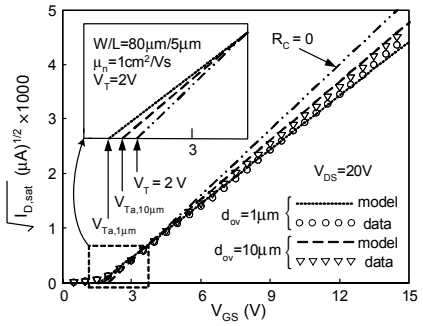


Fig.4. Gate voltage dependence of the contact resistance R_C for various gate to drain/source overlap d_{ov}. The R_C values are extracted from the I-V curve of the test TFTs following the approach introduced in [2].



$$\mu_{na}/\mu_n = 1/\left(1+\alpha\left(1+\frac{16}{15}\times\frac{\alpha}{1-\alpha}\right)\right)^2 \times\left(\frac{\sqrt{1+2\ell_0/L}-1}{\ell_0/L}\right)^2$$

$$V_{Ta} = V_T - \left(\frac{\alpha}{1-\alpha}\right)^2 (1+0.2\alpha)\frac{1}{6R_0 k_n}$$

$$\sqrt{\alpha} = \frac{\sqrt{1+4R_0(V_f - V_T)}-1}{\sqrt{4R_0(V_f - V_T)}}$$

$$V_f = V_T + \frac{V_{DS}}{2} + \frac{\sqrt{1+8k_n V_{DS} R_0}-1}{8k_n R_0}$$

Fig.5. Comparison of our LSF-based model with the experimental data. The apparent threshold voltage V_{Ta} (and μ_{na}) is lower for smaller d_{ov} (higher R_0).The model predicts that V_{Ta} is not affected by the gate-voltage dependent component of R_C (though μ_{na} is). In the model, V_f is the gate voltage at which the saturation to linear transition occurs and α is the ratio $R_0 I_{D,sat}/(V_{GS} - V_T)$ at the transition point, $V_{GS} = V_f$.

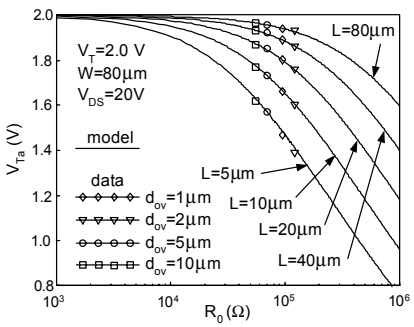


Fig.6. Variation of V_{Ta} versus R_0 for several values of channel length, L. The extracted V_{Ta} is lower at shorter L and higher R_0, as predicted by the model.

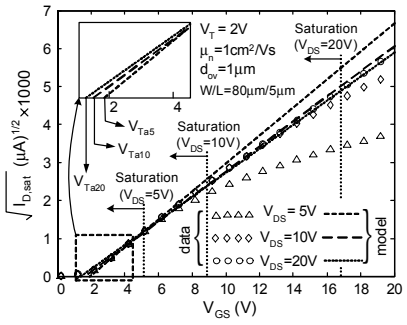


Fig.7. Variation of V_{Ta} for different drain biases. Reducing V_{DS} shrinks the saturation regime over which the LSF is calculated. The extracted V_{Ta} (and μ_{na}) increases with reducing the drain bias as predicted by the model.

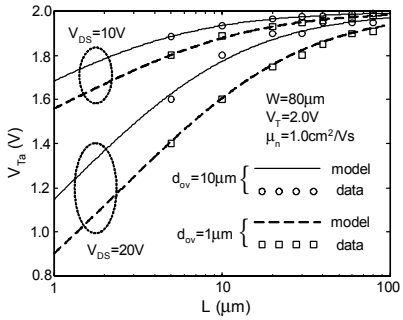


Fig.8. Variation of V_{Ta} versus L for two d_{ov} and V_{DS} values and comparison with the model. The extracted V_{Ta} is lower at shorter L, higher R_0 and higher V_{DS}, as predicted by the model.