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SiN_x barrier layers deposited at 250°C on a clear polymer substrate

Kunigunde Cherenack, Alex Kattamis, Ke Long, I-Chun Cheng, Sigurd Wagner, and James C. Sturm
Department of Electrical Engineering, Princeton University, Princeton, 08544

ABSTRACT

Interest is widespread in flexible thin-film transistor backplanes made on clear polymer foil, which could be universally employed for a variety of applications. All ultralow process temperatures, plastic compatible thin film transistor (TFT) technologies battle short or long term device instabilities. The quality and stability of amorphous silicon thin-film transistors (a-Si:H TFTs) improves with increasing process temperature. TFT stacks deposited at less than 250ºC by radio frequency plasma enhanced chemical vapor deposition (RF-PECVD) exhibit higher threshold voltage shifts after gate bias stressing than stacks deposited at ~300°C in the active matrix liquid-crystal display (AMLCD) industry [1]. Therefore, optically clear plastic (CP) substrates are desired that tolerate high process temperatures. The first step in a-Si:H TFT fabrication on a polymer is the deposition of a planarizing barrier and adhesion layer. For this purpose we have been using silicon nitride (SiN_x) grown by PECVD.

This paper discusses the substrate preparation and SiN_x deposition for the process temperature of 250ºC. We study the mechanical strain in the SiN_x film on the CP substrate, as a function of RF power. Earlier work has shown that SiN_x films deposited at low RF power are under tensile strain, and become increasingly compressed as the deposition power is raised [2]. Additionally, at very high deposition power the substrate is bombarded at the beginning of film growth to achieve good film adhesion. The goal is to identify the correct processing conditions at which the total mismatch strain between the film and the substrate is minimized, to keep the film/substrate composite flat and avoid mechanical fracture as well as peeling due to poor adhesion. Optimal deposition conditions were identified to obtain crack-free SiN_x barrier layers. The barrier layers were tested by fabricating a-Si:H TFTs on them at 250°C.

INTRODUCTION

It is desirable to deposit the SiN_x barrier layers at high temperature on plastic substrates that are intended for the fabrication of display backplanes. The reason is that barrier layers need to be deposited at a temperature close to that of the subsequently deposited TFT stack. TFTs deposited at low temperatures are less stable [1], which is critical for AMOLEDs which require a stable dc drive current. TFT stability is also a key issue for AMLCDs.

The threshold voltage of a-Si TFTs changes with the application of the gate bias voltage, because of carrier trapping in the silicon nitride gate insulator and creation of new dangling bonds in the a-Si:H channel.

Figure **1** shows the threshold voltage shift of TFTs deposited on glass substrates at 150°C and 250°C after application of positive gate bias at room temperature for 600 s, as a function of gate stress field. It is clear that the threshhold voltage shift is smaller for TFTs fabricated at higher temperature.

Therefore, it is desirable to keep the entire process close to the optimum temperature range of 300°C–350°C, which is that in large scale industrial use for a-Si:H TFTs on glass. The barrier layers were optimized at 250°C, which is our standard high temperature platform.

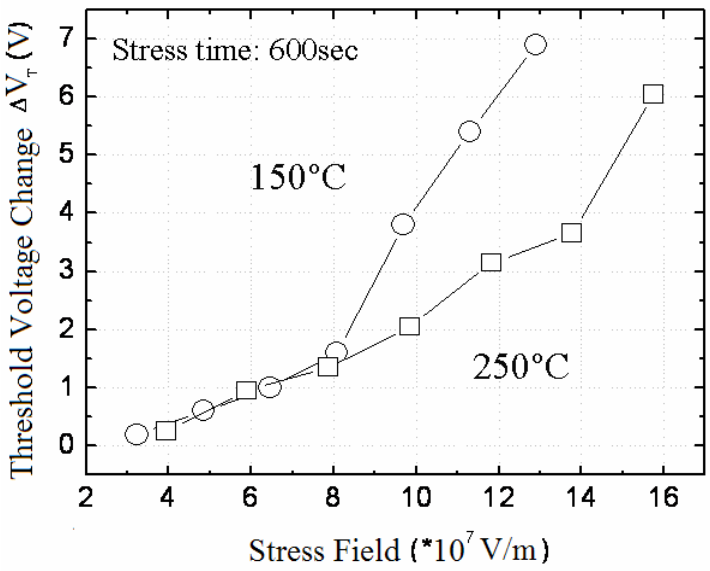

Figure 1 TFT threshold voltage shift after gate stressing at room temperature for 600 s, as a function of gate stress field (for glass substrates). Squares are for the 250°C process, circles are for 150°C process [1].

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THEORY

An important first step in fabricating display backplanes on plastic substrates is to identify the optimal processing conditions to reproducibly deposit crack-free SiN_x barrier layers. Strain also develops in the structure by built-in stresses in the deposited layers (Hooke's law: $\sigma = Y\varepsilon$, where σ is stress, Y Young's modulus, and ε strain), or, upon cooling down, by the differences in the thermal expansion between the deposited film and the substrate, or between different films, and by differences in humidity expansion coefficients. The total strain in the SiN_x barrier layers needs to be carefully controlled to prevent cracking.

A. Controlling Built in Strain

The total mismatch strain between the SiN_x layer and the clear plastic is given by $\varepsilon_M = \varepsilon_0 + \varepsilon_{th} + \varepsilon_{ch}$, where ε_0 is the built-in strain, $\varepsilon_{th} = (\alpha_f - \alpha_s) \times (T_{room} - T_{substrate})$ is the thermal mismatch strain where α_f is the film coefficient of thermal expansion and α_s is the substrate's coefficient of thermal expansion; $\varepsilon_{ch} = (\beta_s - \beta_f) \times \%\Delta R.H.$ is the humidity mismatch strain where the β denotes the coefficient of humidity expansion (CHE) and $\%RH$ is the percent of

relative humidity for a sample taken out from vacuum (R.H. = 0%). The mismatch strain ε has two dominant components: the thermal mismatch strain and the built-in strain ε_{bi} in the deposited film. [2]

It is desirable to keep the mismatch strain close to zero. It is clear that as the deposition temperature is increased, the thermal mismatch strain produced upon cooling to room temperature increases proportionately. Therefore it is necessary to compensate for the CTE mismatch by adjusting the built-in strain in the film. This is done in such a way that $(\alpha_f - \alpha_s) \times \Delta T \cong -\varepsilon_{bi}$. The built-in strain depends on the film deposition conditions and can therefore be adjusted.

This is clearly illustrated in Figure 2. Here the built-in strain in a layer of SiN_x deposited on Kapton is varied by changing the deposition power. This figure shows the result of a series of experiments in which a SiN_x barrier layer is deposited on the Kapton substrate at increasing PECVD deposition powers. The first substrate is a bare Kapton substrate, illustrating that there is an initial curvature to the substrate. In each case, the SiN_x film is deposited on the side of the substrate facing to the left. The changing radius of curvature of each combined structure illustrates a change in the total strain. As can be seen, the SiNx layer is tensile at low powers, then goes through a transition region and is ultimately compressive at very high deposition powers. Our goal now becomes to deposit the barrier layer as close to the transition region as possible in order to minimize the total strain in the barrier layer.

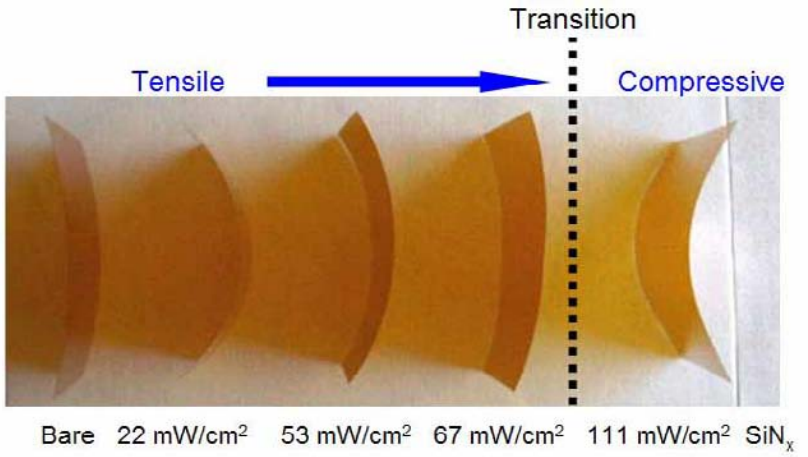

Figure 2 Curvature of 300-500nm thick SiN_x films deposited on 50 μm thick Kapton E. The PECVD deposition power is varied from low to high. The deposited SiN_x films face to the left. The built in strain in the SiN_x film changes from tensile to compressive from left to right. [2]

B. Investigating SiN_x Barrier Layer Adhesion

SiN_x films deposited on clear plastic for various deposition power densities are shown in Figure 3. At the beginning of the deposition, the substrate is bombarded with high energy particles to improve adhesion. At low deposition power densities, the SiN_x adhesion to the clear plastic is very poor and sections of the film have delaminated and flaked away. At intermediate power densities excessive stress in the film causes buckling and cracking of the SiN_x layer. It is

only once the films are deposited at very high power densities (150 mW/cm^2 or more) that the films become crack-free. This result once again confirms that it is necessary to work at high power densities in order to achieve crack-free barrier layers. This agrees with the argument made with Figure 2.

Optimized SiN_x barrier layers of 200-300 nm thickness were deposited at at the very high power density of ~200 mW/cm^2. The clear plastic substrate was coated on both sides at a deposition temperature of 250^{o}C.

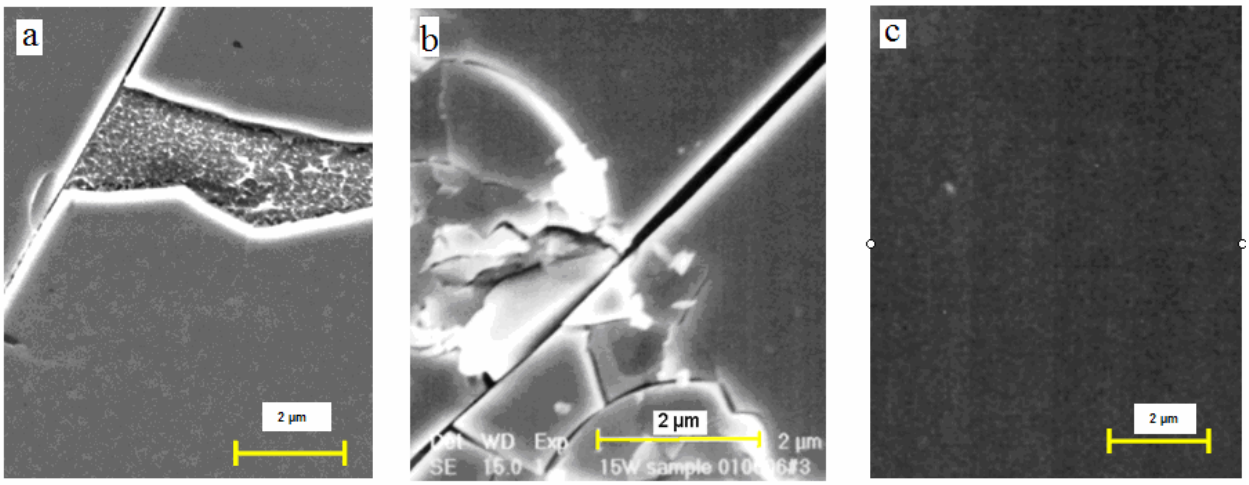

Figure 3 SiN_x film deposited at a) Low power density, poor adhesion; b) Intermediate power density, cracking due to large stress ; c) High power density, no delamination.

RESULTS

Cracking can also occur during TFT stack deposition, as additional sources of strain are introduced. A barrier layer therefore needs to be tested to see if it survives TFT fabrication. The barrier layer was tested by fabricating bottom-gate, staggered, non self-aligned TFTs on the clear substrate.

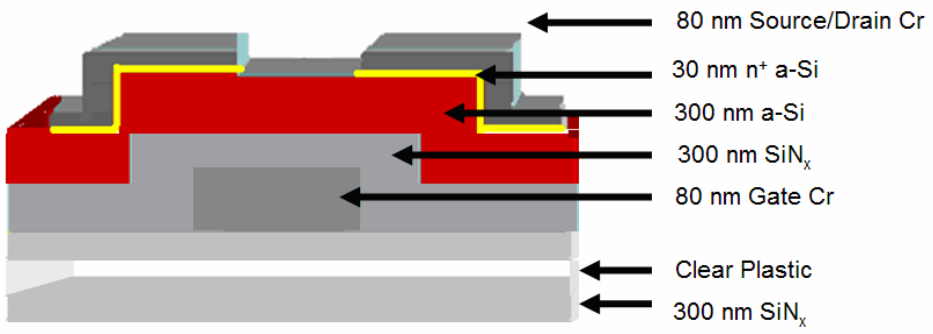

Figure 4 Schematic cross-section of a-Si:H TFT fabricated on a clear plastic substrate

TFT fabrication at 250°C

The first step was to coat the substrate on both sides with a 200-300 nm thick SiN_x barrier layer. Then a 70-80 nm layer of chromium was deposited on the substrate using thermal evaporation. The gates were patterned. Then the TFT stack (300nm SiN_x, 300nm a-Si:H, 30nm n^+ a-Si:H) was deposited at 250°C using plasma enhanced chemical vapor deposition (PECVD). Finally, the TFT stack was covered by a layer of chromium. The last chromium layer was then patterned to form the source-drain regions. Subsequently, the n^+ layer was etched everywhere except under the source-drain metal, and the islands and gate vias were defined using standard photolithography. The schematic cross section of the finished TFT is shown in Figure 4.

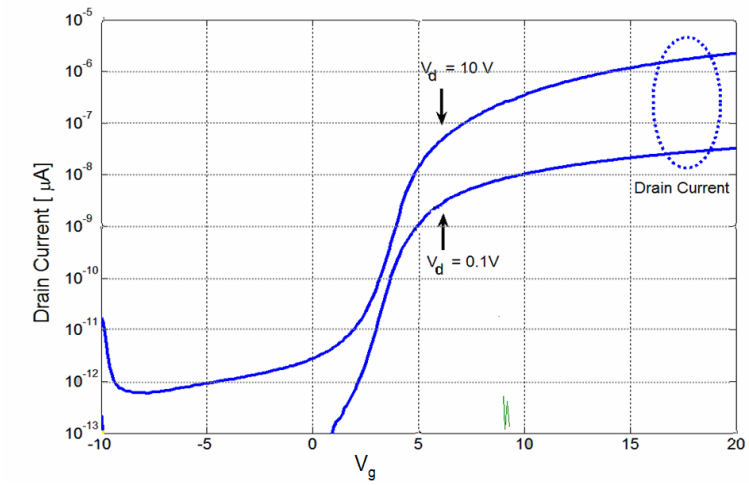

Figure 5 Transfer characteristic of a-Si:H TFT fabricated on the optimized barrier layer at 250°C

For the measured TFT, the W/L ratio is 20μm / 20μm. The TFT transfer characteristics are given in Figure 5. The main performance characteristics are μ_{lin} = 0.8 cm^2/Vs and μ_{sat} = 1 cm^2/Vs. V_t = 3.5 V, S = 700 mV/decade. These results are a good match for TFTs fabricated on glass using the same process.

CONCLUSIONS

SiN_x barrier layers were repeatedly deposited crack-free at 250°C. The key parameter identified for successful deposition was sufficiently high PECVD deposition power density. Finally, TFTs were fabricated on top of the barrier layers. The TFT stack was crack-free and TFT performance was comparable to results obtained from a TFT batch processed on glass.

ACKNOWLEDGMENTS

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REFERENCES

1. Ke Long, A. Z. Kattamis, I.-C. Cheng, H. Gleskova, S. Wagner, and J. C. Sturm, IEEE Electron Device Letters, **27** (2), 111-113 (2006).
2. I-Chun Cheng, Alex Kattamis, Ke Long, James C. Sturm, Sigurd Wagner, Journal of the SID **13** (7), 563-568 (2005).