Increased reliability of a-Si TFT's deposited on clear plastic substrates at high temperatures

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There is great interest in flexible displays. One critical barrier is TFT's on clear plastic, for both active-matrix addressing (for LCD, OLED, and E-ink displays) and for driving DC current in OLED's. The industry standard for AMLCD's is amorphous silicon (a-Si) TFT deposited on glass near 280°C. Several groups have reported TFT's on clear plastic [1,2], but the process temperature must be lowered to accommodate the maximum temperature of clear plastics. (Most clear plastics have glass transition temperature (T_g) of 120°C or less). While the mobility suffers somewhat, the two real problems for low temperature processes are (i) lower temperature a-Si based TFT's have worse carrier trapping in the gate nitride (device reliability, which is critical for OLED's with DC driving), and (ii) industry groups want drop in substitute for glass substrates -- they do not want to adjust their TFT recipes.

In this work we report (i) first a-Si TFT's processed at 280°C on free-standing clear plastic and (ii) demonstrate their increased reliability vs FET's processed at lower temperatures (180°C).

Fig. 1 shows the cross-section of the TFT structure we use on free-standing clear plastic substrates. A thick SiN_x buffer layer on each side of the substrate planarizes the substrate, passivates it against process chemicals, and helps the device layers adhere to the organic polymer. The TFT structure is the standard inverted-staggered structure, with a bottom gate and top source/drain contacts. The TFT channel is defined by a back-channel-etch. Using this structure we successfully fabricated TFT's at 250°C and 280°C with very good performance (Fig. 2). For a TFT made at 280°C with gate width/length of W/L = 80μm/40μm, the threshold voltage is 3.8 V, the ON/OFF ratio is ~10^6 with gate voltages varied from 0 to 20V, the linear mobility is 1.15cm^2/Vs and the saturation mobility is 0.99 cm^2/Vs. The source-gate leakage current is smaller than 4 pA, which is the limit of measurement system. These results enable TFT fabrication on flexible clear plastic substrate like that on glass. The critical element is a novel clear plastic with both a very high glass transition temperature and a low thermal expansion coefficient .

Amorphous silicon TFT degradation due to gate stress is caused by carrier trapping in the gate nitride and it is not related to hot carrier (little drain voltage dependence) [3]. We performed gate stress testing on the TFT's made at 250°C compare to TFT's made at lower temperature of 180°C. Fig. 3 shows the threshold voltage changes after 10 minutes of stress testing with gate connected to high voltage and source and drain grounded. The threshold voltage change under stress is smaller for TFT's made at 250°C compare to those made at 180°C, confirming the superior of the high temperature process. Yet larger improvement compare to usual process on clear plastic (~ 120-150°C) are expected. This is due to improved quality of the gate nitride. While improvement are seen in TFT's made on glass substrates or plastic, the new substrates allow the 280°C process on plastic. The stressing does not substantially alter the mobility, subthreshold slope, or gate leakage of the TFT's. (Fig. 4)

In summary, we developed an a-Si TFT process on clear plastic substrates which allows direct transfer of industry a-Si TFT process on glass to plastic substrate for flexible electronics applications. The high temperature process increases the reliability of the a-Si TFT's, which is critical for OLED's where one TFT must operate in a DC condition.

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[1] D. Styahilev, A. Sazonov, and A. Nathan, "Amorphous silicon nitride deposited at 120°C for organic light emitting display-thin film transistor arrays on plastic substrates", J. Vac. Sci. Technol. Part A Vac. Surf. Films, Vol. 20, No. 1, 2002, pp. 1087-1090

[2] K. Long, H. Gleskova, S. Wagner, and J. C. Sturm, "Short Channel Amorphous-Silicon TFT's on High-Temperature Clear Plastic Substrates", Dig. 62nd Device Research Conf., 2004, pp. 89-90

[3] H. Gleskova, and S. Wagner, "DC-gate-bias stressing of a-Si:H TFTs fabricated at 150°C on polyimide foil", IEEE Trans. Electron Devices, Vol. 48, No. 8, 2001, pp. 1667-1671

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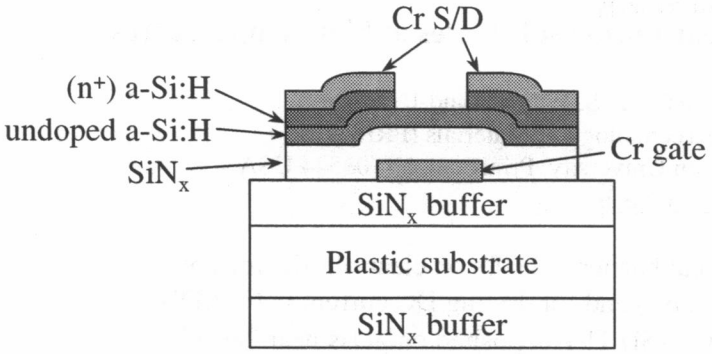

Figure 1. Schematic cross-section of an a-Si TFT on plastic substrate [1].

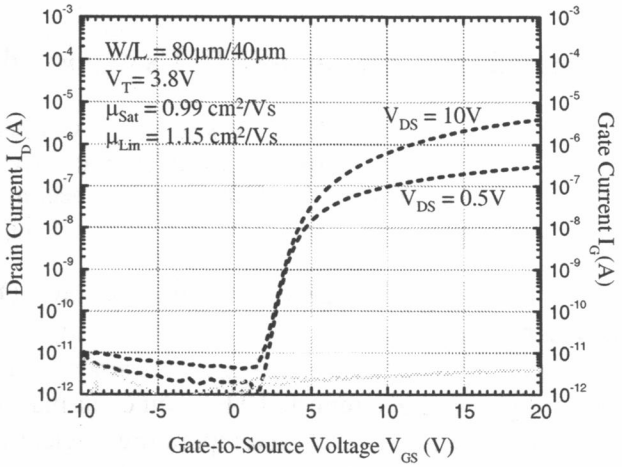

Figure 3. Transfer characteristics of a TFT on a free-standing clear plastic substrate deposited at 280°C.

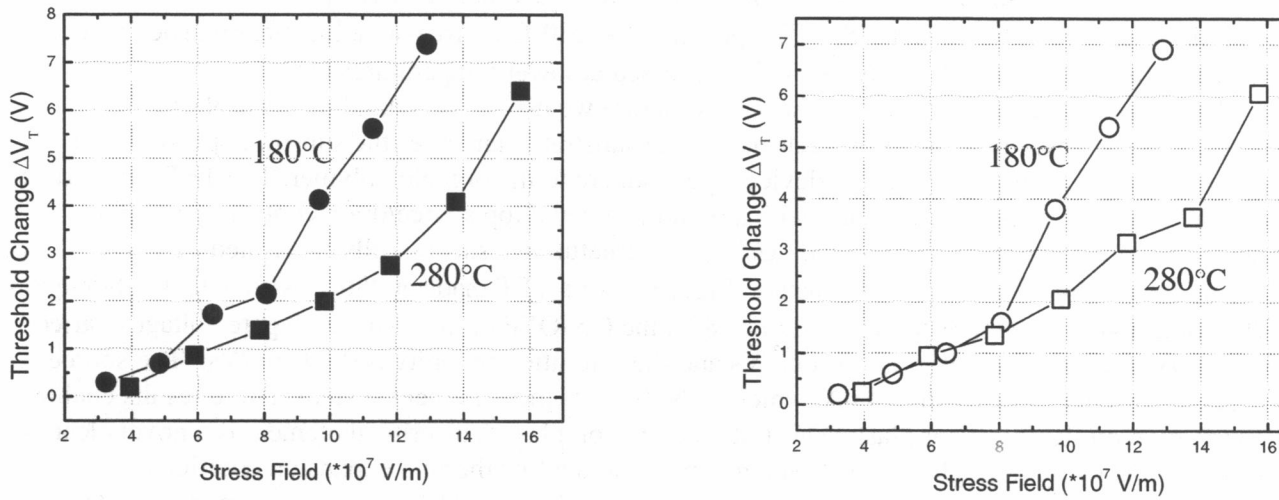

Figure 3. TFT threshold voltage change after gate stressing for10 minute. Left: TFT's on clear plastic substrates; Right: TFT's on glass substrates. Dots are for 180°C process, squares are for 280°C process.

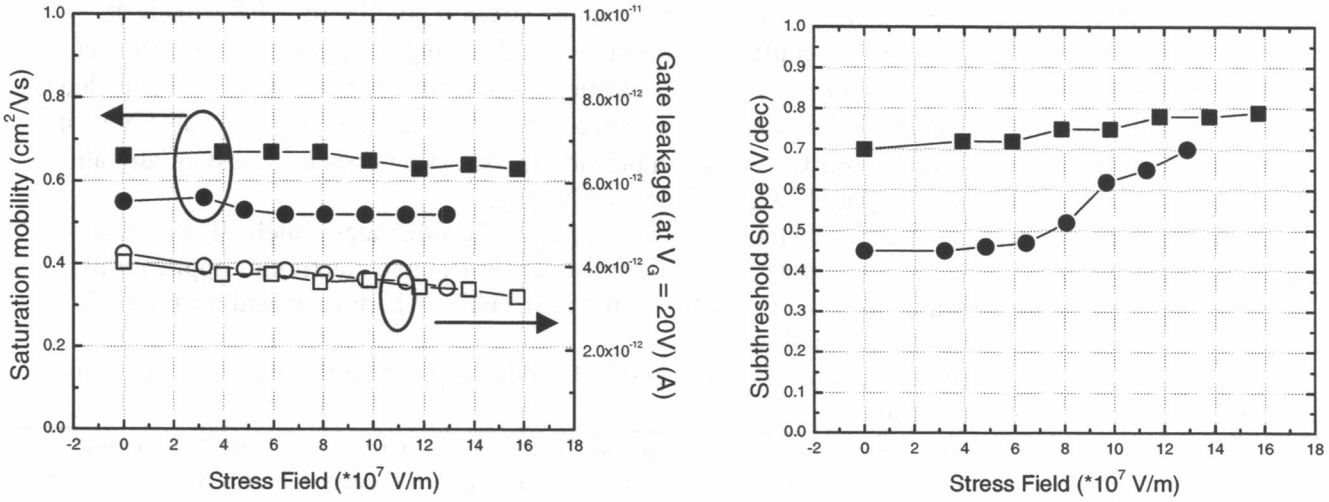

Figure 4. Mobility, gate leakage, and subthreshold slope after gate stressing for10 minute. Dots are for 180°C process, squares are for 280°C process. (TFT's on plastic substrates)