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Device, Circuit, and System Design for Enabling Giga-Hertz Large-Area Electronics

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ABSTRACT Recent progress has substantially increased the operating frequency of large-area electronic (LAE) devices. Their integration into circuits has enabled unprecedented system-level capabilities, toward future wireless applications for the Internet of Things (IoT) and 5G/6G. These exploit large dimensions and flexible form factors. In this work, we focus on giga-Hertz (GHz) zinc-oxide (ZnO) thin-film transistors (TFTs) as a foundational device for enabling GHz LAE circuits and systems. To further understand their operation and limits in the newly possible frequency regime, we incorporate the effects of temperature and of non-quasi-static (NQS) physics into the device models. We then analyze operation including these effects on a fundamental circuit block, the cross-coupled inductor-capacitor (LC) oscillator. It is used in representative LAE systems, namely, a 13.56-MHz radio-frequency identification (RFID) reader array for near-field energy transfer, and a 1-GHz phased array for far-field radiation beam steering. The co-design of devices, circuits, and systems is essential for achieving flexible and meter-scale monolithic-integrated LAE wireless systems. For these, understanding temperature limitations and the NQS effect is crucial.

INDEX TERMS 5G/6G, Internet of Things (IoT), large-area electronics (LAEs), thin-film transistor (TFT), wireless communication.

I. INTRODUCTION

LARGE-AREA electronics (LAE) is a large group of technologies that enable monolithic integration of semiconductors, metals, and dielectrics over large-area substrates, on the order of meters (in contrast to mainstream microcircuits). The core fabrication technology of LAE is thin-film processing of diverse functional materials at low temperature, on substrates of glass and plastic. This enables LAE to incorporate rich functionality and flexible/conformal form factors, at low cost.

Given these properties, LAE has been widely used in flat-panel displays, X-ray imagers, and solar panels [1], [2], [3]. More recently, LAE also has been envisioned for novel sensing applications in the domains of healthcare [4], [5], environment [6], agriculture [7], and structural health [8], with sensors for light [9], strain [10], perspiration [11], pressure [12], and gases [13].

Due to the low mobility caused by the low-temperature process and the smallest feature size limited by the large-area photolithography, LAE devices have reduced performance as compared to silicon (Si) CMOS and III-V devices and, thus, their operation frequency has been restricted to 1–10-MHz range. However, the potential of LAE devices is being actively explored, and recent research pushing LAE to the giga-Hertz (GHz) regime has begun to envision its potential for wireless applications, in particular the Internet of Things (IoT) and 5G/6G [14], [15], [16]. Future wireless systems will employ densely distributed

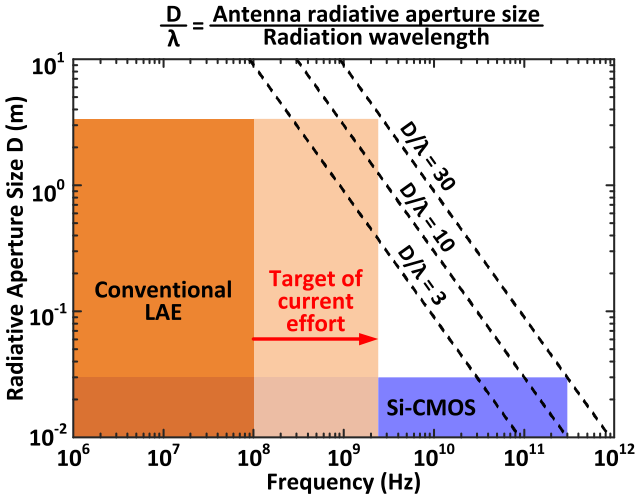

FIGURE 1. Comparison of antenna radiative aperture size and operating frequency achievable by LAE and Si-CMOS. The dotted lines correspond to $D/\lambda = 3$, 10, and 30. For LAE, the dark-shaded region shows the established frequency limit. The light-shaded region illustrates the target of recent research efforts to bring LAE to the GHz regime (adapted from [16]).

sensor nodes for rich contextual information and high-resolution measurements. Here, spatial addressing plays a key role, requiring antennas that steer radiation beams with high spatial control and resolution. The spatial resolution of radiated beams is determined by the ratio of the antenna-aperture size (D) to the radiation wavelength (λ). Larger D/λ values provide higher spatial resolution ($D/\lambda > 3$ is necessary for practical systems), and also enable the synthesis and control of diverse radiation patterns [16], [17].

Fig. 1 compares the D/λ values achievable with LAE and Si-CMOS. On the one hand, while the operating frequency of Si integrated circuits can reach hundreds of GHz ($\lambda \leq 1$ cm), their small size prevents monolithic integration over antenna dimensions for wireless systems in the GHz regime, which is of particular interest for low-power and long-range wireless communication (e.g., 2.4-GHz band for Wi-Fi/Bluetooth, UHF band for cellular/television communication). On the other hand, LAE benefits from large values of D, but its established frequencies of $<$ 100 MHz [2], [3] lead to λ of meters. Enabling the frequency band from several hundred MHz to several GHz with large D/λ, within a fully integrated, scalable, and conformal technology, has motivated research on boosting LAE-system frequencies.

We will show that moving LAE systems to this regime requires tight device, circuit, and system co-design, to fully leverage attributes of the technology toward operation close to the device limits. As an example, the actual circuit and system operating frequencies of today's mainstream crystalline-substrate integrated circuit technologies (Si-CMOS and III–V semiconductors) are $10-100\times$ lower than the device-level frequency limits, due to practical losses. In contrast, recent research shows that the achievable operating frequency of LAE-based circuits and systems can be very close to the device-level frequency limits, by appropriately leveraging the high-quality, low-loss passives and substrates enabled by LAE fabrication [15], [16], [18], and by properly aligning circuit topologies with the particular device attributes derived from LAE materials [19].

This article is motivated by the importance of understanding and modeling device-level physics, hence, limitations for such co-design, specifically associated with temperature-limit and non-quasi-static (NQS) effect. Section II of this article reviews recent progress in boosting LAE device frequency, and introduces readers to zinc-oxide (ZnO) thin-film transistors (TFTs) as representative GHz LAE devices. Structure, fabrication process, device characteristics, and high-frequency modeling of ZnO TFTs are discussed. Section III investigates the effect of temperature for thermally optimized TFT operation.

Section IV moves to the circuit level, beginning with high-quality, low-loss LAE passives as key enablers for LAE circuits and systems. Then, a case study of the recently demonstrated 1-GHz cross-coupled inductor-capacitor (LC) oscillator is presented, followed by the introduction of two high-frequency LAE systems based on the oscillator. One system is a 13.56-MHz radio-frequency identification (RFID) reader array for near-field energy transfer, and the other is a 1-GHz phased array for far-field radiation beam steering. The oscillator, which forms the basis of all the presented circuits, is revisited using the high-frequency ZnO TFT model developed in this article.

II. DEVICE ENGINEERING FOR GHz ZnO TFTS

Among the LAE devices demonstrated so far are TFTs, diodes, inductors, and capacitors. In this section, we focus on the TFT, since it provides critical active and passive operations for a broad range of circuits.

A. REVIEW OF RECENT PROGRESS IN TFT PERFORMANCE

Operation as an active device imposes stricter limits on TFT operation than operation as a passive device [15], [18]. For active-device operation, the TFT is typically biased in the saturation regime to provide current/power amplification. In this case, the TFT's unity-current-gain frequency f_T and unity-power-gain frequency f_{MAX} are the frequency-limit metrics of primary interest.

f_T and f_{MAX} from representative recent efforts on bringing LAE to the GHz regime [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37] are summarized in Fig. 2. The trend toward increasing the operating frequency is clear.

We note that raising the LAE device operating frequency does not necessarily preserve compatibility with large area, low cost/area, and flexibility. For example, electron-beam lithography (EBL) is used in [21] and [27]. In [29] and [30], the fabrication of flexible GHz single-crystal Si TFTs requires a release and transfer of the Si from a rigid substrate to a flexible substrate, which introduces additional complexity and cost to device fabrication. Post-deposition annealing

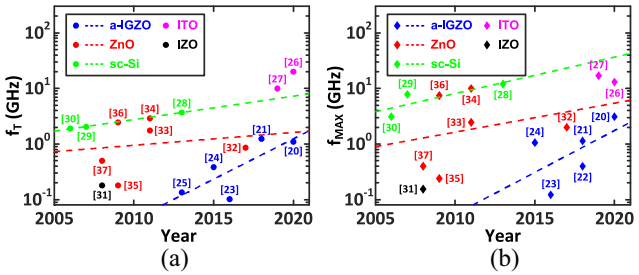

FIGURE 2. Summary of f_T and f_{MAX} achieved in recent work on bringing LAE devices to the GHz regime. a-IGZO, ZnO, sc-Si, ITO, and IZO stand for amorphous indium–gallium–zinc oxide, zinc oxide, single-crystal silicon, indium–tin oxide, and indium–zinc oxide, respectively.

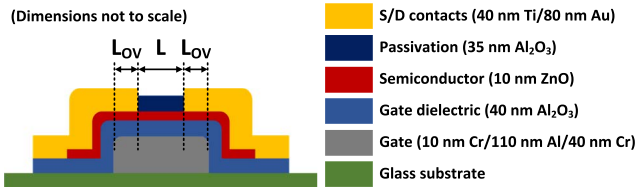

FIGURE 3. Schematic of a bottom-gate ZnO TFT's cross-section (L = channel length; L_{OV} = length of overlap between source/drain to gate). All the LAE devices for circuits and systems discussed in this article are fabricated on glass substrates, to ease system prototyping and testing.

at elevated temperature (500°C) is required in [35], which precludes most flexible plastic substrates.

On the other hand, fabrication processes reported in [20] and [32] preserve large-area and flex compatibility by using photolithography with micron-scale linewidths, limiting process temperatures to 200 °C − 250 °C, and avoiding other possibly complicating processing (such as thin-film release and transfer).

The devices reported in [20] and [32] both have operating frequencies in the GHz range. In the rest of this article, we employ ZnO TFT technology similar to that reported in [32]. Of course, the circuit and system co-design concepts will apply to other device technologies as well.

B. FABRICATION OF BOTTOM-GATE STAGGERED ZnO TFTS

Fig. 3 shows the cross-section of the typical bottom-gate staggered ZnO TFT studied in further detail in this article. The gate electrode consists of a composite metal stack of 10-nm Cr/110-nm Al/40-nm Cr. The first 10-nm Cr layer provides necessary adhesion to the glass substrates. The thick Al layer provides low gate resistance, which is essential for high frequency operation [32]. The top 40-nm Cr layer protects the Al from forming hillocks and sets the appropriate work function [38]. The gate dielectric (40-nm Al_2O_3), the active semiconducting layer (10-nm ZnO), and the passivation layer (35-nm Al_2O_3) are deposited in a single PEALD run. Al_2O_3 and ZnO are selectively etched in aqueous pH-controlled solutions of NaOH (pH = 12 − 13) and H_3PO_4 (pH = 3 − 4), respectively, [39]. Source/drain (*S/D*) contacts are 40-nm Ti/80-nm Au bilayers. Critical dimensions are the channel length (L) and the length of *S/D* to gate overlap (L_{OV}).

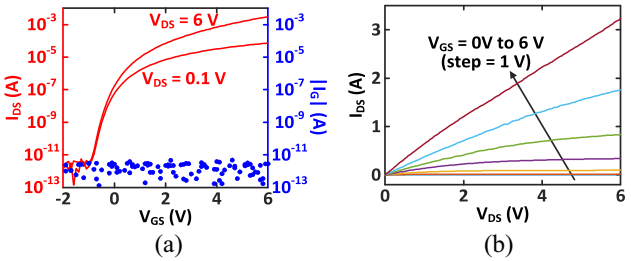

FIGURE 4. (a) Typical transfer curves of short-channel ZnO TFTs (W/L = 150 μm/1.0 μm). (b) Typical output curves of short-channel ZnO TFTs (W/L = 150 μm/1.0 μm).

This in-house fabrication is designed to be compatible with standard industrial processes. Its key features are: 1) a maximum process temperature of 200 °C; 2) a minimum linewidth of ∼1 μm, defined by contact optical lithography; and 3) self-alignment of the source and drain to gate (for details see Section II-C). Processing at low temperature provides compatibility with plastic/flexible substrates, which many of the demonstrated circuits and systems in Section IV would ultimately require for future applications.

Due to limitations of the in-house fabrication facilities for research, the maximum substrate size for devices covered in this article is 7.5 cm × 7.5 cm. Furthermore, we note that glass is used as a substrate to facilitate large-area circuits and systems demonstrations, based on dicing and wire bonding to carrier printed circuit boards (PCBs). Previous experiences on developing systems (based on amorphous Si [40], [41] and ZnO [42] TFTs) have shown this to be a prudent approach for improving yield and robustness for system-level demonstrations. Subsequent transition to flexible substrates has been successfully achieved [41], [43], via additional procedures for substrate passivation and observing temperature ceilings, which can limit yield and system performance at early stages but are ultimately readily incorporated. Such transition to flexible substrates has also enabled detailed study on the effect of substrate mechanical properties on device performance. For example, Afsar et al. [43] studied ZnO TFT performance under bending, showing that ultrathin 3.5-μm polyimide substrates preserve device performance better than 50-μm thick polyimide substrates.

C. DEVICE CHARACTERISTICS OF ZnO TFTS AT DC AND RADIO FREQUENCY

Typical transfer curves and output curves of short-channel ZnO TFTs (W/L = 150 μm/1.0 μm) measured at DC are shown in Fig. 4. Table 1 shows corresponding statistics of key device figures of merit extracted from ten ZnO TFTs.

For a typical ZnO TFT with W/L = 50 μm/1.0 μm, the high-frequency device characterization results, namely, $|H_{21}|$ and MAG, are shown in Fig. 5. f_T and f_{MAX} are 591 MHz and 2.12 GHz, respectively. They are among the highest f_T's and f_{MAX}'s reported so far obtained with a large-area compatible and flex-compatible device fabrication process [20], [32].

TABLE 1. Statistics (mean and standard deviation) of device figures of merit extracted from 10 ZnO high-mobility TFTs measured at DC. Transconductance g_m is extracted by fitting I_{DS} versus V_{GS} at $V_{GS} = 5 - 6$ V and $V_{DS} = 6$ V. Mobility μ_n and threshold voltage V_T are extracted by fitting $\sqrt{I_{DS}}$ versus V_{GS} at $V_{GS} = 5 - 6$ V and $V_{DS} = 6$ V. Small-signal output resistance r_o is extracted by fitting I_{DS} versus V_{DS} at $V_{DS} = 5 - 6$ V and $V_{GS} = 6$ V.

W/L (μm/μm)	150/1.0
Gate to S/D overlap L_{OV} (μm)	~0.5
Transconductance g_m (mS)	1.7 ± 0.2
Mobility μ_n ($cm^2/V{\cdot}s$)	21 ± 3
Threshold voltage V_T (V)	2.4 ± 0.2
Subthreshold slope SS (mV/dec)	149 ± 16
Output resistance r_o (kΩ)	2.4 ± 0.9

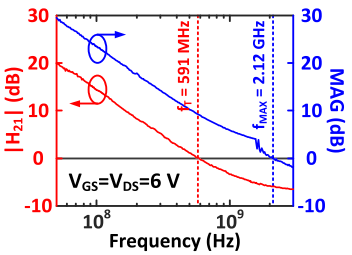

FIGURE 5. Measured small-signal current gain $|H_{21}|$ and maximum available power gain MAG of a typical ZnO TFT ($W/L = 50\ \mu m/1.0\ \mu m$ and $L_{OV} = \sim 0.5\ \mu m$), biased in the saturation regime with $V_{GS} = V_{DS} = 6$ V.

D. LIMITS TO F_T AND F_{MAX}

f_T and f_{MAX} of TFT can be estimated with the following equations [44], [45]:

$$f_T = \frac{g_m}{2\pi \cdot (C_{GS} + C_{GD})} \tag{1}$$

$$f_{MAX} = \frac{f_T}{2\sqrt{R_G \cdot \left(\frac{1}{r_0} + g_m \cdot \frac{C_{GD}}{C_{GS}+C_{GD}}\right)}}. \tag{2}$$

Transconductance g_m relates f_T and f_{MAX} to TFT geometry (TFT channel width W and length L, etc.), and to charge-carrier mobility μ_n, since $g_m = \mu_n C'_{OX}(W/L)(V_{GS} - V_T)$ (C'_{OX} is the gate oxide capacitance per unit area). With the TFT biased to saturation, the capacitance C_{GS} consists of the gate-to-channel capacitance and a parasitic overlap capacitance between source and gate [$C_{GS} = (2/3)C'_{OX}WL + C'_{OX}WL_{OV}$], while C_{GD} consists of the parasitic overlap capacitance between drain and gate ($C_{GD} = C'_{OX}WL_{OV}$). R_G represents the gate resistance in the direction of the channel width; it is determined by the gate electrode geometry and the resistivity of the gate metal.

The two most important factors in f_T and f_{MAX} (through g_m) are the channel length L and the electron mobility μ_n. Our experimental L is $\sim 1\ \mu m$, with a spread of $\sim 0.2\ \mu m$, caused primarily by nonuniformities in photoresist thickness and UV exposure. μ_n from our ZnO deposited by PEALD is typically $10 - 20\ cm^2/(V \cdot s)$, which is similar to those found in LAE production processes [46]. Fig. 6 shows representative statistical data for μ_n from 15 ZnO TFTs

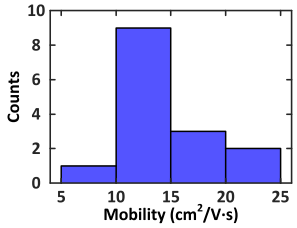

FIGURE 6. Representative statistics for electron mobility in 15 ZnO TFTs ($W/L = 150\ \mu m/1\ \mu m$) on one glass substrate. Mobility is extracted by fitting $\sqrt{I_{DS}}$ versus V_{GS} at $V_{GS} = 5 - 6$ V and $V_{DS} = 6$ V. The average mobility is 14 $cm^2/(V \cdot s)$, with a standard deviation of 4 $cm^2/(V \cdot s)$.

($W/L = 150\ \mu m/1\ \mu m$, a set of TFTs different from those evaluated for Table 1) on one glass substrate. Nonuniform Al_2O_3 thickness, and device process variations, are the principal causes of mobility variation.

E. APPROACHES TO RAISING F_T AND F_{MAX}

Besides L and μ_n evaluated from (1) and (2), f_T and f_{MAX} are limited by the parasitic overlap capacitances C_{GS} and C_{GD} and the gate resistance R_G.

In large-area technology with a bottom-gate ("gate-first") structure, overlaps of a few micrometers between the source/drain mask and the gate mask are typically required to accommodate possible misalignment between the two layers over large area, especially for flexible substrates. Such overlaps increase C_{GS} and C_{GD}, hence, reduce f_T and f_{MAX}, as is evident from (1) and (2).

The overlap capacitances in C_{GS} and C_{GD} can be reduced by using the opaque gate electrode as the mask when defining the *S/D* contacts. This self-alignment becomes possible when the substrate (glass), the gate dielectric (Al_2O_3) and the channel semiconductor (ZnO) are transparent to the UV light used for photolithographic exposure [20], [32], [47], [48]. This process can reduce the overlap to $\sim 0.5\ \mu m$, which results in an overlap capacitance of $\sim 0.9\ fF/\mu m$.

The aluminum in the composite metal stack described in Section II-B provides low resistivity. The sheet resistance of this composite metal stack measured at DC is $\sim 0.4\ \Omega/sq$. A multifinger layout is employed [15] to divide the total width of the TFT into multiple fingers, thereby reducing the resistance in the direction of the channel width.

By applying these improvements of device materials, geometry, and fabrication process, the TFT operating frequency can be brought into the GHz regime. The expressions for f_T and f_{MAX} also reveal fruitful approaches to device-circuit co-design. f_T depends primarily on g_m hence field-effect mobility, which is low in LAE materials (but whose upper limits are not yet known). f_{MAX} additionally depends on device-level losses like gate metal resistance, which can be reduced as just described. Thus, through careful device engineering to reduce losses, f_{MAX} is demonstrated to be considerably higher than f_T, motivating circuit topologies that are limited by f_{MAX} rather than f_T.

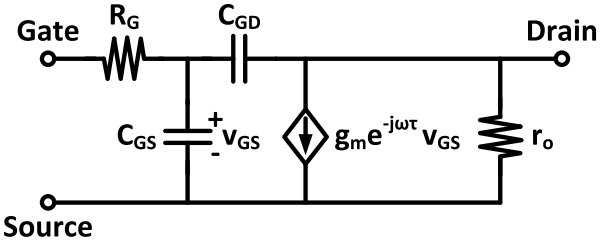

FIGURE 7. Small-signal model of ZnO TFT proposed for high-frequency modeling. τ describes the channel current delay due to the NQS effect.

F. NON-QUASI-STATIC EFFECT IN ZnO TFTS OPERATING IN THE GHz REGIME

As the operating frequency of TFTs moves to the GHz regime, NQS effect must be considered, as experience with Si-CMOS technologies has shown [49], [50], [51]. For example, at a channel length $L = 1$ μm and a mobility $\mu_n = 10$ cm$^2/(V \cdot s)$, the "transit time" for an electron traveling from source to drain, in a typical ZnO TFT biased at $V_{GS} = V_{DS} = 6$ V, can be estimated as $t_{tr} = (L^2/\mu_n \cdot V_{DS}) \approx 170$ ps. The drain current does not change instantly when the gate voltage changes. This delay affects the relative phase of the drain current that emerges from the channel, an effect that will become significant when the frequency reaches the GHz range.

So far, only limited high-frequency modeling has been pursued for LAE TFTs [52], [53], [54]. These existing methods have the following limitations: 1) the analytical approaches are difficult to implement for the simulation of complex circuits and systems and 2) the large number of model parameters makes model tuning and interpretation infeasible. Therefore, it is necessary to develop a compact, accurate, and easy-to-use small-signal model of TFTs for high-frequency circuit and system design in the GHz range.

Using our ZnO TFT as an example, the small-signal model of Fig. 7 is proposed. It is adapted from those used for high-frequency modeling in Si-CMOS, e.g., [50] and [55]. Here, τ describes the delay of the current through the channel due to the NQS effect. The rest of the circuit components follow the definitions covered in previous sections. (Note that this is only a first-order model of the NQS effect in transistors. Also, the delay time τ of the current source in Fig. 7 can differ significantly from the simple calculation of transit time t_{tr} shown above. A more rigorous physics-based model of the behavior of electrons in the channel will lead to a more realistic but complex circuit model [56], [57].)

To facilitate the following discussion of the NQS effect on high-frequency TFT performance, the current gain and the maximum available power gain of a two-port network defined using scattering parameters (S-parameters) are shown in (3) and (4) [58], where the stability factor k is defined as

$$\frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12} \cdot S_{21}|}.$$

In the following discussion, the ZnO TFT is treated as a two-port network. Port 1 is between TFT gate and source, while port 2 is between drain and source

$$|H_{21}| = \left| \frac{-2S_{21}}{(1 - S_{11}) \cdot (1 + S_{22}) + S_{12} \cdot S_{21}} \right| \tag{3}$$

$$\text{MAG} = \begin{cases} \left| \frac{S_{21}}{S_{12}} \right|, & \text{when } k < 1 \\ \left| \frac{S_{21}}{S_{12}} \right| \cdot \left(k - \sqrt{k^2 - 1} \right), & \text{when } k \geq 1 \end{cases} \tag{4}$$

With the device model shown in Fig. 7, the admittance parameters (Y-parameters) are calculated as follows:

$$Y_{11} = \frac{j\omega(C_{GS} + C_{GD})}{j\omega(C_{GS} + C_{GD}) \cdot R_G + 1} \tag{5}$$

$$Y_{12} = -\frac{j\omega C_{GD}}{j\omega(C_{GS} + C_{GD}) \cdot R_G + 1} \tag{6}$$

$$Y_{21} = \frac{g_m e^{-j\omega\tau} - j\omega C_{GD}}{j\omega(C_{GS} + C_{GD}) \cdot R_G + 1} \tag{7}$$

$$Y_{22} = \frac{j\omega C_{GD} \cdot \left(1 + g_m e^{-j\omega\tau} \cdot R_G + j\omega C_{GS} \cdot R_G\right)}{j\omega(C_{GS} + C_{GD}) \cdot R_G + 1} + \frac{1}{r_0}. \tag{8}$$

Similar to the procedure described in [55], the model parameters, namely, C_{GS}, C_{GD}, R_G, g_m, τ, and r_o, can be extracted using (5)–(8) as follows:

$$C_{GS} = -\frac{1}{\omega \cdot \text{Im}\left(\frac{1}{Y_{11}}\right)} - \frac{1}{\omega \cdot \text{Im}\left(\frac{1}{Y_{12}}\right)} \tag{9}$$

$$C_{GD} = \frac{1}{\omega \cdot \text{Im}\left(\frac{1}{Y_{12}}\right)} \tag{10}$$

$$R_G = \text{Re}\left(\frac{1}{Y_{11}}\right) \tag{11}$$

$$g_m = \left| j \cdot \left(1 - \frac{Y_{21}}{Y_{12}}\right) \cdot \frac{1}{\text{Im}\left(\frac{1}{Y_{12}}\right)} \right| \tag{12}$$

$$\tau = -\frac{1}{\omega} \cdot \angle \left[j \cdot \left(1 - \frac{Y_{21}}{Y_{12}}\right) \cdot \frac{1}{\text{Im}\left(\frac{1}{Y_{12}}\right)} \right] \tag{13}$$

$$r_o = \frac{1}{\text{Re}\left\{Y_{22} + Y_{12} \cdot \left(1 + g_m e^{-j\omega\tau} \cdot R_G + j\omega C_{GS} \cdot R_G\right)\right\}}. \tag{14}$$

Some key symbols used in (13) are defined as follows.

1) τ is the TFT channel current delay in NQS operation (in seconds).
2) $\angle$ takes the phase of a complex number (in radians).
3) Y_{12} and Y_{21} are defined in (5) and (6).

The model's accuracy is evaluated using the device measured for Fig. 5 (biased in saturation with $V_{GS} = V_{DS} = 6$ V). First, model parameters (9) through (14) are calculated from high-frequency measurements conducted with a vector network analyzer (VNA). The extracted model parameters are listed in Table 2.

From the device geometry ($W/L = 50$ μm/1.0 μm and $L_{OV} = \sim 0.5$ μm), C_{GS} and C_{GD} are estimated to be 103 fF and 44 fF, matching (with error less than $\pm 11\%$) the values shown in Table 2. The extracted g_m is lower and the extracted

TABLE 2. Model parameters extracted from high-frequency measurement results of a ZnO TFT with the device characteristics shown in Fig. 5.

C_{GS} (fF)	92
C_{GD} (fF)	49
R_G (Ω)	102
g_m (μS)	445
τ (ps)	34
r_o (kΩ)	15

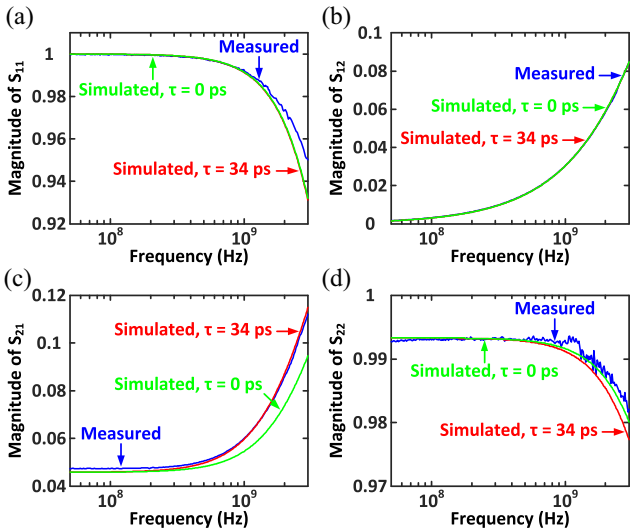

FIGURE 8. Comparison of the magnitudes of (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}, between measurement and simulation. Simulation is done with either $\tau = 34$ *ps* (NQS effect) or $\tau = 0$ *ps* (no NQS effect).

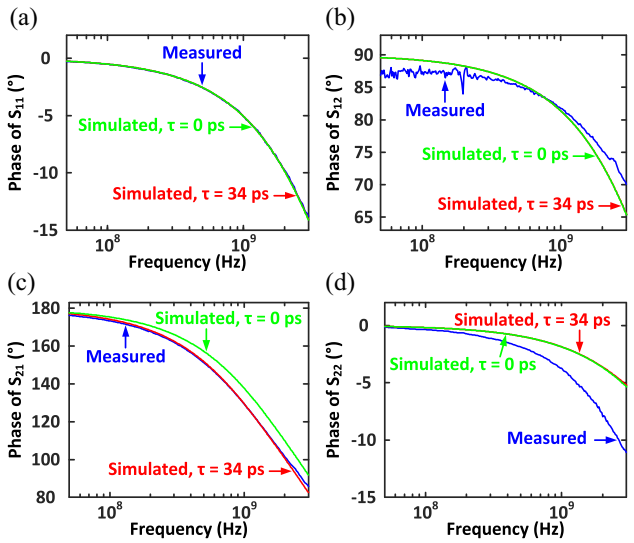

FIGURE 9. Comparison of the phases of (a) S_{11}, (b) S_{12}, (c) S_{21}, and (d) S_{22}, between measurement and simulation. Simulation is done with either $\tau = 34$ ps (NQS effect) or $\tau = 0$ ps (no NQS effect).

r_o is higher than the corresponding values listed in Table 1 (from scaling of the numbers reported in Table 1 for the different channel width, g_m and r_o are expected to be ∼ 570 μS and ∼7.2 kΩ, versus the extracted 445 μS and 15 kΩ). These differences are primarily due to the fact that in our high-frequency measurements using a VNA (Table 2), ZnO TFTs are biased with pulsed signals of short duration (on the order of 0.1–1 ms, depending on the measurement setup), rather than DC signals. The differences between device characteristics shown in Tables 1 and 2 result from self-heating, as discussed in Sections III-A.

The gate resistance R_G is estimated as ∼20 Ω, based on measured sheet resistance and gate electrode geometry [note that aluminum, the dominant conductor in the TFT's gate electrode, has a radio frequency (RF) skin depth of ∼2.6 μm at 1 GHz, much greater than the total gate thickness of ∼160 nm; therefore, we assume that R_G is independent of frequency].

The simulated S-parameters of the device, with and without the NQS effect, are compared to those from measurements. Figs. 8 and 9 indicate good agreement between S-parameters, when the NQS effect (with $\tau = 34$ ps) is included versus when it is not (with $\tau = 0$ ps). The most significant accuracy improvement in modeling is observed in S_{21}, especially in the GHz regime. Since S_{21} describes the ratio between the transmitted voltage at the output (drain of TFT) and the incident voltage at the input (gate of TFT), it is a critical parameter for circuit operation, as captured by $|H_{21}|$ and MAG in (3) and (4).

The input voltage couples to the output voltage of the TFT in two ways: 1) the input signal directly couples to the output through TFT parasitics (including R_G and C_{GD}) and 2) the input voltage generates a small-signal current through g_m, which converts to a part of the output voltage through the output load. With τ introducing a frequency-dependent phase shift to the second component, the phases of these two components become closer as frequency increases. Therefore, with the NQS effect, the resulting modeled output voltage and, thus, the modeled S_{21} are closer to measurement [Figs. 8(c) and 9(c)] than without the NQS effect, which is essential for accurately predicting $|H_{21}|$ and MAG, hence, circuit operation at high frequency.

Moving now to the critical device-level frequency-limit metrics, f_T and f_{MAX} are predicted from the simulated S-parameters to be 579 MHz and 1.75 GHz, respectively, which do match the measured f_T and f_{MAX}. Fig. 10 compares $|H_{21}|$ and MAG between simulations (with $\tau = 34$ ps and $\tau = 0$ ps) and measurements. Simulations with both $\tau = 34$ ps and $\tau = 0$ ps estimate f_T and f_{MAX} fairly well. Still, including the NQS effect results in better overall shape approximation to the measured curves, especially in the GHz range. As seen in Fig. 10(a), the measured and NQS simulated (with $\tau = 34$ ps) $|H_{21}|$ curves are indistinguishable, while the curve simulated with $\tau = 0$ ps lies significantly lower than that measured in the GHz regime (e.g., by ∼2 dB at 3 GHz).

Similarly, in Fig. 10(b), the MAG curve simulated with $\tau = 34$ ps is indistinguishable from the measured curve up to ∼1 GHz. Above ∼1.3 GHz, MAG drops sharply since the stability factor k changes from $k < 1$ to $k \geq 1$ and, thus,

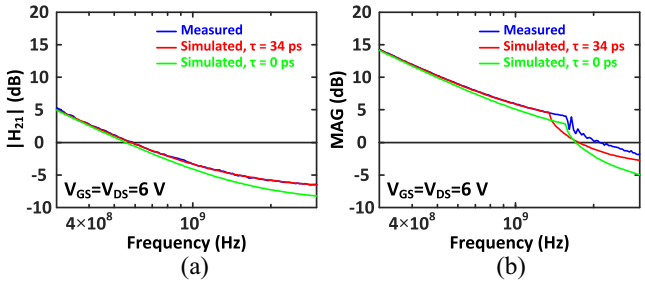

FIGURE 10. Comparison of (a) current gain $|H_{21}|$ and (b) maximum available power gain MAG. Simulation is done with either $\tau = 34$ ps (NQS effect is included) or $\tau = 0$ ps (NQS effect is excluded).

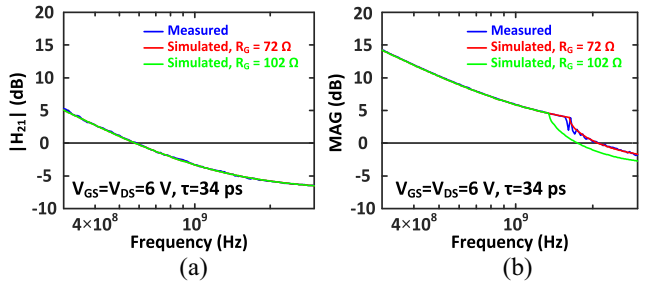

FIGURE 11. Comparison of (a) current gain $|H_{21}|$ and (b) maximum available power gain MAG. Simulation is done with either $R_G = 102\ \Omega$ or $R_G = 72\ \Omega$, while τ is fixed to 34 ps.

a different MAG expression is adopted [as predicted in (4)], whose onset is related to R_G [59]. As the original extraction of $R_G = 102\ \Omega$ may have been inaccurate, we tuned R_G to 72 Ω, which resulted in nearly perfect agreement of MAG between simulation and measurement all the way to 3 GHz, as shown in Fig. 11(b). Tuning R_G does not affect $|H_{21}|$ as shown in Fig. 11(a), since $|H_{21}|$ is independent of R_G.

In summary, as indicated by the trends in Figs. 8–11, the device-level impact of the NQS effect sets in at high frequencies, specifically near f_T and f_{MAX} of ZnO TFTs. As shown in Section IV, this frequency range is of interest when the performance of LAE circuits and systems is pushed to the TFT limits. In Section IV-D, we will show the corresponding impact on circuit operation. The overall conclusion is that the NQS effect must be properly incorporated in high-frequency device modeling, to enable TFT circuit design near the frequency limits. As the NQS effect is expected to be more pronounced for TFTs with even higher cutoff frequencies, the presented work will serve as a guidepost to further work on high-frequency LAE.

III. THERMAL CONSIDERATIONS FOR ZNO TFTS

With f_T and f_{MAX} in the GHz regime, ZnO TFTs show the potential for application to high-frequency circuits and systems as active devices. This section introduces device-level considerations for ZnO TFTs, specifically, the effect of temperature on device characteristics and temperature limits imposed by thermally induced breakdown.

In various application scenarios, ZnO TFTs are biased with different DC voltages and durations. In most of our system

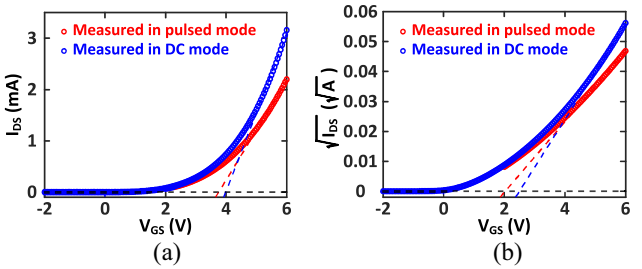

FIGURE 12. (a) Transfer curves of a typical short-channel ZnO TFT ($W/L = 150\ \mu$m/1.0 μm) measured at $V_{DS} = 6$ V, in DC mode and in pulsed mode. The dashed lines show the extraction of transconductance by fitting I_{DS} versus V_{GS} at $V_{GS} = 5 - 6$ V. (b) Extraction of mobility based on curves shown in (a), by fitting $\sqrt{I_{DS}}$ versus V_{GS} at $V_{GS} = 5 - 6$ V.

examples, ZnO TFTs are biased in the saturation regime ($V_{DS} > V_{GS} - V_T$) to provide signal amplification, where a large I_{DS} runs through the device. Combined with a high V_{DS}, this leads to large power consumption ($P = V_{DS} \cdot I_{DS}$) and, thus, self-heating. Because of the poor thermal conductance of LAE substrates (glass in our work) compared to that of silicon substrates, "self-heating" effects can become pronounced in LAE.

A. EFFECT OF TEMPERATURE ON DEVICE CHARACTERISTICS AND RELIABILITY

Many previous studies identify the effect of temperature on carrier transport in ZnO thin films. For example, the trap-release mechanism suggests that the mobility of electrons in a ZnO thin film increases with temperature [60]. Because of the thermally stimulated emission of electrons from traps, the density of mobile electrons increases with the rising temperature. This density increase is captured as an increase in effective electron mobility and, thus, an increase in I_{DS} through the TFT. Therefore, the higher the TFT power dissipation ($V_{DS} \cdot I_{DS}$), the higher the effective electron mobility and I_{DS}. Thus, this study focuses primarily on the regime with large power dissipation, for example, the high V_{GS} regime in Fig. 12, and the high V_{DS} and V_{GS} regime in Fig. 13.

As an experimental demonstration, Fig. 12 shows the transfer curves of a typical ZnO TFT ($W/L = 150\ \mu$m/1.0 μm), measured in the DC mode and the pulsed mode. In the DC mode, each data point (I_{DS} at given V_{DS} and V_{GS}) is collected with voltage duration of 88 ms, while in the pulsed mode, each data point is collected with voltage duration of 50 μs. As shown, transconductance and mobility are extracted as 1.5 mS and 19.2 $cm^2/(V \cdot s)$ from the DC mode measurement, while they are 1.0 mS and 10.5 $cm^2/(V \cdot s)$ from the pulsed mode measurement. The DC mode leads to higher transconductance and electron mobility because the longer voltage duration in the DC mode raises the temperature of the TFT. Fig. 13 shows the output curves of the same ZnO TFT ($W/L = 150\ \mu$m/1.0 μm) measured in DC mode, and pulsed mode. The output resistance extracted at $V_{DS} = 5 - 6$ V and at $V_{GS} = 6$ V are 2.1 kΩ in DC mode and 5.7 kΩ in pulsed mode.

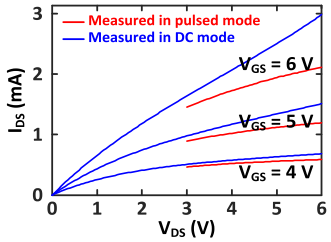

FIGURE 13. Output curves of a typical short-channel ZnO TFT ($W/L = 150\ \mu m/1.0\ \mu m$) measured in DC mode and pulsed mode. The output resistance is extracted by fitting at I_{DS} versus V_{DS} at $V_{DS} = 5 - 6$ V.

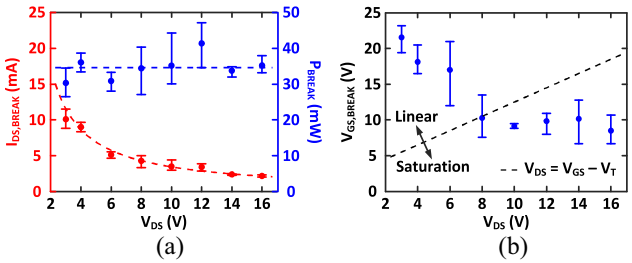

FIGURE 14. (a) Measured breakdown current $I_{DS,BREAK}$ versus V_{DS} and breakdown power P_{BREAK} versus V_{DS}. (b) Measured breakdown gate-to-source voltage $V_{GS,BREAK}$ versus V_{DS} (adapted from [15]).

These results suggest a possible reason for the difference in g_m and r_o between DC and high-frequency extraction shown in the previous section. Even more generally, we note that device parameters (such as transconductance, output resistance, etc.) extracted from DC mode measurement should not be directly applied to high-frequency device modeling, when devices are operated in the pulsed (duty-cycled) mode that typically is desired for raising device stability.

These results also highlight the need for careful design and implementation of biasing conditions (such as biasing voltages, and voltage duration) if it is desired to accurately estimate device parameters and to operate TFTs at the frequency limit.

B. THERMALLY INDUCED BREAKDOWN

Having explored the effect of temperature on device parameters, we turn to its impact on limiting device operating frequency. Higher f_T and f_{MAX} can be achieved by biasing TFTs with higher V_{GS} and V_{DS}. However, our experiments show that raising V_{GS} and V_{DS} causes ZnO TFTs to breakdown, which restricts their achievable frequency. It is thus essential to understand the limits to raising V_{GS} and V_{DS} as they pertain to device breakdown.

We perform experiments at different V_{DS} values where V_{GS} is raised until device breakdown occurs. Fig. 14 shows drain-to-source current at breakdown $I_{DS,BREAK}$, and the breakdown power P_{BREAK} ($P_{BREAK} = I_{DS,BREAK} \cdot V_{DS}$) versus V_{DS}. Regardless of the TFT biasing and operation regime (saturation or linear), a roughly constant breakdown power is observed for all V_{DS} values, which suggests thermally induced breakdown [15].

The breakdown mechanism sets the upper limit for biasing voltages and, thus, the achievable f_T and f_{MAX}, when ZnO TFTs are biased in the saturation regime as active devices. This has motivated circuit and system topologies where ZnO TFTs are used as passive devices, biased in the linear regime (i.e., with smaller V_{DS} and I_{DS} and, thus, lower power dissipation $V_{DS} \cdot I_{DS}$) [15]. Though, in this way, higher frequencies have been achieved for LAE systems, in the present article, we keep our focus on the important regime of active-device TFT operation for circuits and systems.

IV. CASE STUDY OF HIGH-FREQUENCY LAE CIRCUITS AND SYSTEMS BASED ON ZNO TFTS

Following the TFT-level discussions, this section will show how high-frequency LAE circuits and systems operating near the TFT limits can be achieved, particularly by leveraging the high-quality, low-loss passive components (inductors and capacitors) possible in LAE. We start with a discussion of these passives, and then overview the system-prototyping methodology pursued. Then, we describe three circuit and system case studies: a 1.25-GHz cross-coupled inductor-capacitor (LC) oscillator [18]; a 13.56-MHz RFID reader array [61]; and a 1-GHz phased array [16]. With the LC oscillator serving as the foundational block for all three case studies, we then revisit its design and analysis considering the NQS effect, illustrating its importance for future efforts pushing to higher-frequency LAE systems.

A. PASSIVE COMPONENTS IN LAE TECHNOLOGY

Previous sections describe TFT operation and modeling up to the GHz frequency range in detail. The LAE system demonstrations presented in the next sections, which include but are not limited to resonant circuit operation, require high-quality inductors and capacitors, in addition to TFTs. To show the feasibility of monolithic LAE circuits fabricated without conventional discrete passive components, in this section, we describe the performance of integrated inductors [15] and capacitors [16] fabricated in LAE technology up to the GHz range.

1) LAE INDUCTORS

Compared to inductors integrated on conventional IC's, integrated LAE inductors benefit from the large available area and, thus, large loop dimensions, wide metal traces, and low-loss substrates, all contributing to a high quality (Q) factor. On the other hand, the typical metal thickness on a PCB is $\sim$35 μm, using methods such as plating to achieve thick metal layers for low resistance and, thus, high Q factor. If we restrict LAE technology to "thin film" metal layers deposited by sputtering or evaporation such that all inductors might be integrated on a meter-sized substrate with conventional LAE process equipment, an upper limit to metal layer thickness would be only a few micrometers, leading to higher resistance and possibly lower Q factor.

Fig. 15 shows the simulation results of Q factor versus frequency for inductance of $L = \sim$14 nH in two cases,

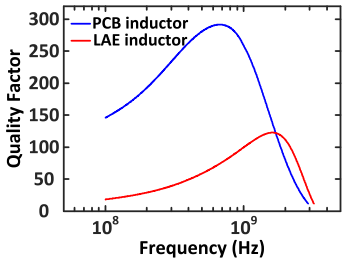

FIGURE 15. Simulated quality factors of PCB inductor and LAE inductor, with inductance $L = \sim 14$ nH. For both inductors, the inner loop radius is 3.55 mm, and the trace width is 0.9 mm. To replicate the experimental implementations, the PCB inductor is simulated with 35-μm thick Cu on a FR-4 substrate (1.6-mm thick), while the LAE inductor is simulated with 2.5-μm thick Au on a glass substrate (0.5-mm thick).

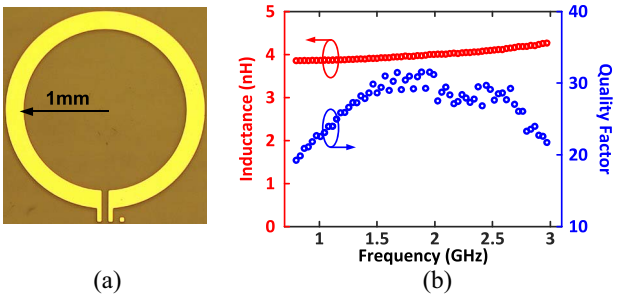

FIGURE 16. (a) Microscope image of the loop inductor fabricated on a glass substrate. (b) Measured inductance and quality factor of the gold loop inductor, with 1-mm radius, 200-μm trace width, and 2.5-μm thickness (adapted from [15]).

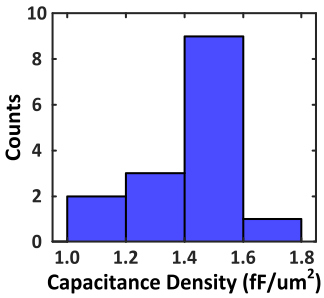

FIGURE 17. Statistics of capacitance density across the 7.5 cm×7.5 cm glass substrate. The average capacitance density is 1.4 fF/μm^2, with a standard deviation of 0.2 fF/μm^2.

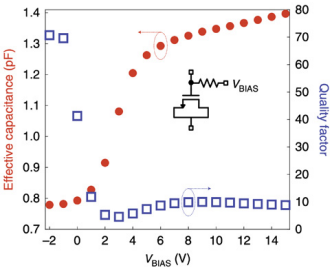

FIGURE 18. Inset: schematic of ZnO TFT ($W/L = 480$ μm/1 μm) with source and drain shorted together to function as a gate-to-TFT channel capacitor. Measured capacitance (dots) and corresponding quality factor (squares), versus the biasing voltage V_{BIAS} (adapted from [16]).

comparing a PCB thick-film (35 μm) copper inductor and an LAE thin-film (2.5 μm) gold inductor. Below 1 GHz, the PCB inductor has a clearly superior Q factor, due to its lower resistance. However, the skin-depth effect becomes an important factor in the GHz range. For example, at 2 GHz, the skin depth of a gold conductor and a copper conductor are $\sim$1.7 and $\sim$1.5 μm, respectively and, thus, the LAE inductor has a Q factor similar to that of the PCB inductor.

Such an LAE inductor has been implemented in [15]. Fig. 16 shows the experimental inductance and Q factor of a $\sim$4-nH single-loop inductor made by thermally evaporated gold with 1-mm radius, 200-μm trace width, and $\sim$2.5-μm thickness. The $\sim$2.5-μm thickness was chosen as a rough upper limit of what might be achieved using "large-area" fabrication technology. In summary, integrated LAE inductors in the nH range with Q factor greater than 20 in the GHz range appear feasible, with a performance similar to those made with PCB thick-film technology.

2) LAE CAPACITORS

Two kinds of LAE capacitors are relevant for the following case studies. The first is a fixed-value metal-dielectric-metal parallel-plate capacitor. In our experiments, the dielectric material is $\sim$45-nm thick Al_2O_3 deposited by PEALD, a thickness on the same order as that used for gate dielectrics. As shown in Fig. 17, this leads to an average capacitance density of 1.4 $fF/\mu m^2$, enabling efficient integration given the large area available for circuits. For example, in a resonant application of inductor and capacitor at 1 GHz, assuming an inductance of $\sim$1 nH, an area of $\sim$150 μm $\times \sim$150 μm would be required for the capacitor, which is not especially demanding in LAE technology.

The second kind of large-area integrated capacitors is a controllable-value gate-to-TFT channel capacitor, made without any extra process steps beyond TFTs [16]. The TFT source and drain are shorted together to provide the counter electrode to the gate. Fig. 18 shows the tunable capacitance characteristics by sweeping the gate-to-source/drain voltage. This structure enables phase tuning in the demonstrated GHz phased array (details provided in Section IV-D).

B. SYSTEM-DEMONSTRATION METHODOLOGY

As mentioned in Section II-B, a system-prototyping methodology is adopted beginning with TFT fabrication on glass substrates, followed by dicing and wire bonding to a large-area PCB carrier. This is due to limitation of the in-house fabrication equipment to 7.5 cm $\times$ 7.5 cm substrates. However, a key focus of the work is maintaining process compatibility with current state-of-the-art display manufacturing, based on low-temperature, large-area materials deposition and lithography.

To further facilitate system prototyping, PCB passives are used, either as discrete components (capacitors) or by direct patterning (inductors). This enables post-fabrication tuning to optimize circuit parameters. However, an important

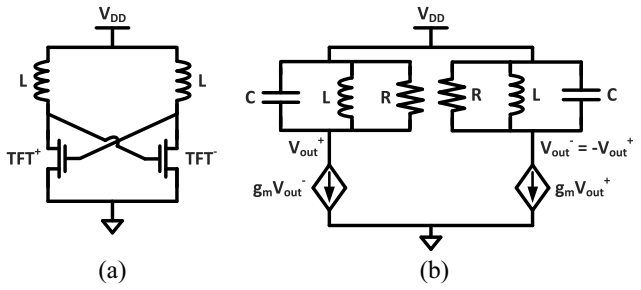

FIGURE 19. (a) Schematic and (b) equivalent small-signal model of the cross-coupled LC oscillator.

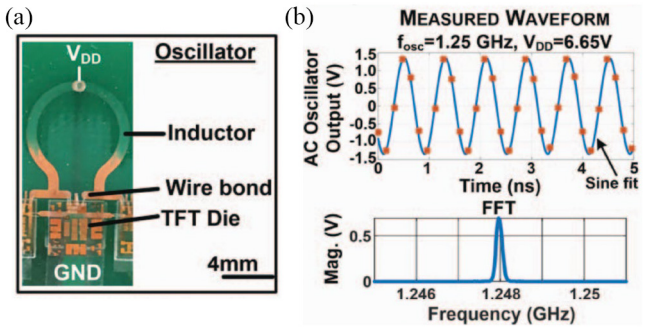

FIGURE 20. Cross-coupled LC oscillator demonstrated in [18]. (a) TFT die is wire bonded to PCB with planar loop inductor, for test. (b) Measured waveform and associated spectrum results after fast Fourier transform, confirming the oscillation frequency of 1.25 GHz.

aim for system evaluation is ensuring performance representative of monolithically integrated LAE passives. For capacitors, the primary consideration is feasibility of dimensions, based on LAE capacitance density and required values. For inductors, the primary consideration is comparable Q factor, particularly with PCB inductors having much thicker traces ($\sim$35 μm) than LAE inductors ($\sim$2.5 μm). As discussed in Section IV-A, in the GHz range the Q factor of PCB inductors converges to that of LAE inductors due to the skin-depth effect. This was critical to the demonstration in [15], which transitioned to monolithically fabricated inductors and TFTs for a 2.4-GHz LAE reconfigurable antenna.

C. GHz CROSS-COUPLED LC OSCILLATOR BASED ON ACTIVE ZnO TFTS

Oscillators are important circuit blocks for applications in wireless transceivers, near-field communication, and sensor read-out circuitry. A GHz cross-coupled LC oscillator based on active ZnO TFTs is demonstrated in [18]. Its key enabling factors are: 1) f_{MAX}-limited (instead of f_T-limited) circuit structure due to resonant operation and 2) high-quality-factor LAE-compatible inductors (thanks to the large dimensions, thick metal traces, and low-loss substrates available in the LAE domain).

Fig. 19 shows the schematic and the equivalent small-signal model of the cross-coupled LC oscillator. It consists of two ZnO TFTs in common-source configuration, connected back-to-back to provide positive feedback. Each of the two ZnO TFTs can be modeled as a transconductor loaded with a small-signal RLC tank.

Based on the analysis shown in [18], the resistive component R is a parallel combination of TFT gate resistance $R_{G,P}$ (after series-to-parallel transformation, $R_{G,P} \approx (1/[\omega^2(2C_{GD}+C_{GS})^2 R_G])$, where R_G is the series resistance to gate), TFT output resistance r_o, and inductor parasitic resistance $R_{IND,P}$ (after series-to-parallel transformation, $R_{IND,P} \approx (\omega^2 L^2/R_{IND})$, where R_{IND} is the series resistance of the inductor L). The capacitive component C is a parallel combination of the TFT's parasitic capacitance C_{TFT} (including TFT gate-to-drain capacitance C_{GD} and TFT gate-to-source capacitance C_{GS}, $C_{TFT} \approx 4C_{GD}+C_{GS}$), and the self-capacitance of the inductor C_{IND}. The inductive component L is contributed by the inductor, chosen to resonate with C at a targeted oscillation frequency.

At the designed oscillation frequency $f_{osc} = (1/2\pi\sqrt{LC})$, the RLC networks provide a total phase shift of 0° through the loop. Under this condition, an open-loop gain of $(g_m R)^2 > 1$ is necessary to sustain oscillations. Accordingly, the oscillation criterion $g_m R$ must be greater than 1. We note that g_m, R, L, and C depend on the TFT's channel width (the TFT channel length is assumed fixed to the smallest achievable feature size). Therefore, to realize maximal $(g_m R)^2$ or $g_m R$ at f_{osc}, the TFT's width must be scaled.

In the oscillator prototyped on a PCB [18], the inductor is implemented as a planar copper loop (radius of 4 mm, trace width of 1 mm, and thickness 35 μm). The ZnO TFTs on glass are diced and wire-bonded to the PCB. The circuit parameters are chosen such that the open-loop gain is estimated to be $\sim$2.6. Fig. 20(a) shows the oscillator. At $V_{DD} = 6.65$ V, the measured oscillation frequency is 1.25 GHz, as shown in Fig. 20(b).

D. RFID READER ARRAY

RFID is a foundational technology for IoT [62], [63]. Based on oscillators employing ZnO TFTs, a large-area 5 × 5 active-matrix RFID reader array was demonstrated to read from distributed commercial ISO14443 13.56-MHz tags [61]. In the system architecture shown in Fig. 21(a), each reader pixel (RDR-PIXEL) is a 13.56-MHz oscillator controlled by row/column selection signals. When a pixel is selected, the corresponding oscillator generates the tag-powering signal through inductive coupling to the tag. Readout is achieved via current demodulation on the shared V_{DD}. Major benefits of this architecture include: 1) the active-matrix structure reduces connections between a centralized readout IC and the distributed array of readers and 2) the architecture avoids the conventional active-matrix use of TFTs as switches in the high-frequency signal pathway, which would be infeasible since TFT parasitics keep the switch off-to-on impedance ratio small and, thereby, cause excessive coupling between rows and columns.

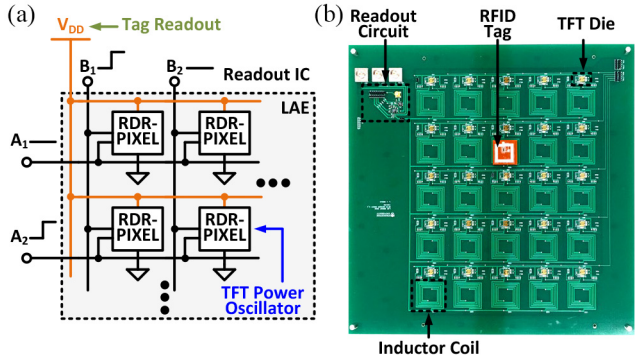

FIGURE 21. (a) System architecture of the RFID reader array demonstrated in [61]. The active-matrix structure reduces connections between the centralized readout IC and the distributed array of readers. The oscillations are generated locally by RDR-PIXELs, to interact with RFID tags. (b) Photograph of prototype 5 × 5 reader array (adapted from [61]).

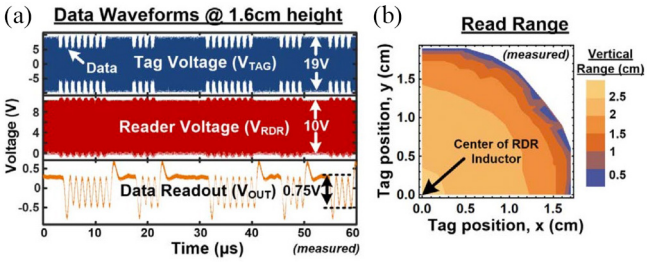

FIGURE 22. Tag readout details adapted from [61]. (a) Waveforms showing proper powering and readout of the RFID tag. (b) Lateral and vertical read ranges.

In this RFID application, the small-signal modeling and analysis of the oscillator is similar to that described in the previous section. However, due to inductive tag coupling for near-field power transfer, the resistive component R in the RLC tank includes an additional component contributed by the loading of the RFID tag. Oscillator design for this application requires: 1) an oscillation frequency of 13.56 MHz; 2) a minimum tag voltage for reading the tag; 3) an open-loop gain greater than 1 to sustain the oscillation; and 4) a margin for safe operation of the ZnO TFTs, below their breakdown limit.

The ZnO TFTs used in this system employ a non-self-aligned fabrication process (yielding f_T and f_{MAX} of 35 MHz and 100 MHz, respectively, as compared to 566 MHz and 2.7 GHz for self-aligned TFTs in Section IV-B). This enables a free running frequency with a deviation of up to 0.7 MHz from the standard-compliant frequency. The precise frequency of 13.56 MHz is then achieved by adding an external capacitance of roughly 80 pF, implemented as a discrete component, but which could readily be achieved via a ∼250 μm ×∼250 μm monolithically fabricated LAE capacitor, as shown in Section IV-A.

After properly sizing the width of the ZnO TFTs and the diameter of the planar inductor in the oscillator, a pixel density of 730 pixels/m^2 is reached. After filtering and amplification, demodulated data with an amplitude of $>$ 350 mV and a maximum power consumed by the reader array of $<$ 280 mW are obtained [Fig. 22(a)]. With a standard 2.4 cm × 2.4 cm tag, the reader array achieves a vertical read range of 3 cm and a lateral read range of 1.6 cm, with a readout speed of 5 ms per element [Fig. 22(b)]. From the application perspective, this system can be implemented to cover a work surface (a desk, a counter, etc.) on the order of 1–3 m^2. Such substrate sizes can be readily achieved with current state-of-the-art display manufacturing capabilities (where the maximum substrate size is on the order of ∼3 m × ∼3 m [64]).

E. PHASED ARRAY

Phased arrays are key components for the IoT and 5G/6G applications [65], [66]. A three-element LAE-based phased array operating at ∼1 GHz has been demonstrated [16]. Its system architecture is shown in Fig. 23(a). The system consists of a linear array of radiative elements at $d = \lambda/2$ spacing, where $\lambda = 30$ cm is the wavelength of the electromagnetic wave at 1 GHz in free space. Each radiative element consists of a GHz cross-coupled LC oscillator as described above, plus a tunable capacitor bank.

Injection locking is employed to synchronize oscillation frequency and establish deterministic phase differences among all radiative elements in the array. Injection locking sidesteps the use of f_T-limiting LAE circuits for synchronization and buffering, thereby enabling operation at the higher f_{MAX} limit. An external periodic differential signal with a fixed frequency (the reference frequency) is directly coupled to the drains of the two ZnO TFTs in the oscillator. According to Adler's equation [67], under the condition that the natural frequency of the oscillator and the reference frequency are close to each other, the oscillation frequency will be locked to the reference frequency, with the phase difference between the oscillator output and the injection signal determined by the difference between the oscillator's natural frequency and the reference frequency. Therefore, the tunable capacitor bank's control of the oscillator's natural frequency enables phase-controllable synchronization across all the radiative elements in the array, relative to the common reference.

As shown in the upper frame of Fig. 23(b), the size of the TFT dies, diced and wire-bonded to the PCB, is ∼0.5 cm × ∼0.5 cm. The size of the overall system (including the PCBs and the spacing between them) is ∼7 cm × ∼40 cm.

As shown in Fig. 24, given proper phase setting for each individual radiative element, the measured radiation patterns from the prototyped phased array show beam steering over ∼60° and a maximum half-power beamwidth of ∼38°.

F. NON-QUASI-STATIC EFFECT ON OSCILLATOR DESIGN

The oscillator-based systems described in previous sections operate very close to the TFT limits. They are both enabled and restricted by the LAE technology: enabled by high-quality passives and low-loss substrates, while restricted by

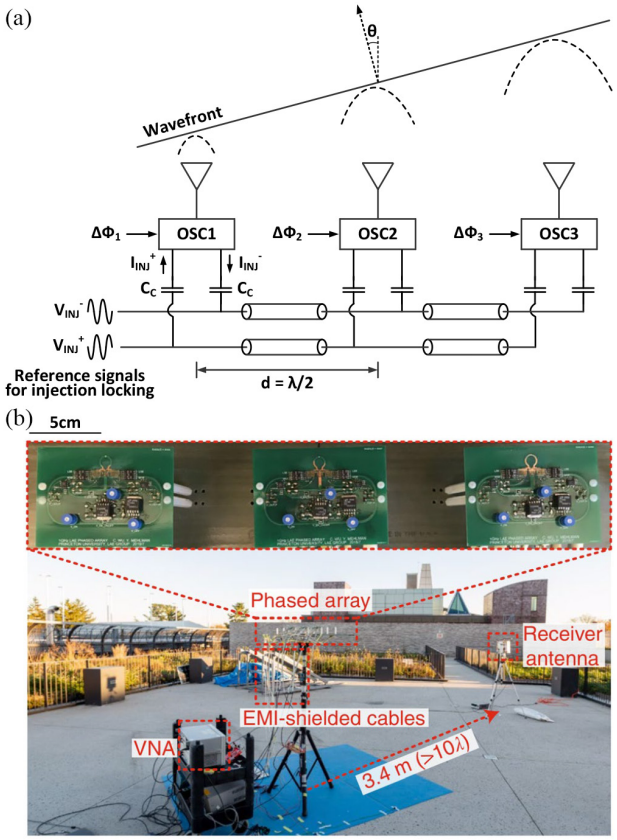

FIGURE 23. (a) System architecture of the phased array demonstrated in [16]. The system consists of an array of radiating elements at $\lambda/2$ spacing. Each radiating element is driven by a local oscillator (*OSCi*, $i = 1, 2, 3$), which generates a sinusoidal voltage signal for excitation. Differential reference signals ($V_{INJ}^{\pm}$) are coupled to each oscillator for injection locking. $\Delta\Phi_i$ ($i = 1, 2, 3$) is the phase difference between oscillation in the i-th oscillator and the reference signal. $\Delta\Phi_i$ is tuned individually, such that the direction of a far-field beam θ is determined by $\Delta\Phi_i - \Delta\Phi_{i-1} = \pi \cdot sin\theta$ ($i = 1, 2, 3$). (b) System test setup adapted from [14]. The upper frame shows the three-element phased array. The phased array is mounted on a rotating rigid base and the receiver antenna is placed 3.4 m away, in the far-field range. The reference signal for injection locking is provided by the VNA.

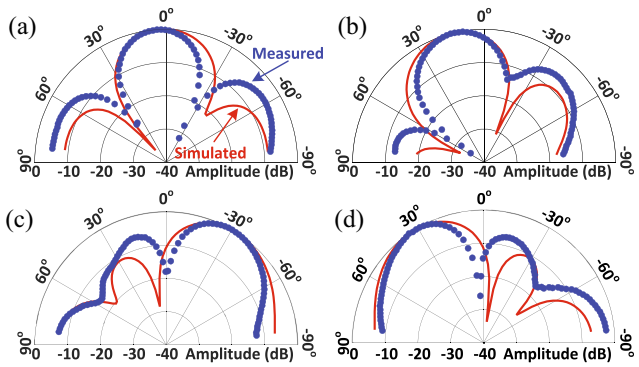

FIGURE 24. Measured and simulated far-field radiation patterns at 982 MHz when the beam is steered to (a) $\theta = 0^{\circ}$, (b) $\theta = 15^{\circ}$, (c) $\theta = -30^{\circ}$, and (d) $\theta = 30^{\circ}$. Measured radiation patterns are plotted as blue dots, while simulated patterns are plotted as red solid lines (adapted from [16]).

thermal breakdown due to insulating substrates. Motivated by the importance of accurate device modeling and of understanding operation so close to the TFT limits, we now incorporate the NQS effect and analyze its impacts.

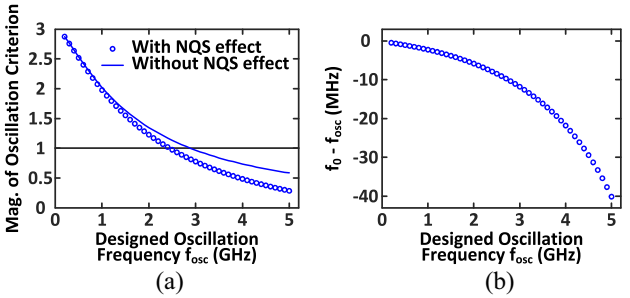

FIGURE 25. (a) Magnitude of maximum achievable oscillation criterion with and without NQS effect, in function of designed oscillation frequency f_{osc}. (b) Difference between the actual oscillation frequency f_0 and the designed oscillation frequency f_{osc}, versus f_{osc}.

We denote the impedance of the RLC network in cross-coupled LC oscillators as $Z_{\text{TANK}} = R\|(1/j\omega C)\|j\omega L = |Z_{\text{TANK}}(\omega)| \cdot e^{j\theta_{\text{TANK}}}$, following the notation in Fig. 19. To enable positive feedback via a total phase shift of 0° through the loop, the phase shift $-\omega\tau$ due to delay in the TFT's channel current must be compensated by the phase in Z_{TANK}. By achieving that, the actual oscillation frequency f_0 ($\omega_0 = 2\pi f_0$) is shifted from the designed oscillation frequency $f_{\text{osc}} = (1/2\pi\sqrt{LC})$, and the open-loop gain degrades from $(g_m R)^2$ to $(g_m|Z_{\text{TANK}}(\omega_0)|)^2$. Here $|Z_{\text{TANK}}(\omega_0)| < R$, since the oscillator operates at a frequency off f_{osc}.

We conduct an analysis similar to that presented in [18]. First we pick, for each designed oscillation frequency, the width of the TFT and the inductance in the RLC tank such that the maximum oscillation criterion ($g_m R$) at that frequency is achieved. Then the value of this maximally achievable oscillation criterion ($g_m R$) is plotted versus the designed oscillation frequency. The frequency where the maximum achievable oscillation criterion falls to 1 corresponds to the oscillation frequency limit.

To study the NQS effect on the achievable oscillation frequency, we again use the optimal design parameters, including the width of the TFT, the inductance in the RLC tank, etc., that we have identified without the NQS effect. Then, the value of the oscillation criterion is calculated with the NQS effect included.

For simplification, the ZnO TFT (with channel length $L = 1$ μm and overlap $L_{\text{OV}} = 0.5$ μm) is assumed to have 1 finger. The self-capacitance of the inductor is ignored (in the example of [16], the self-capacitance of the inductor is $\sim$15% of the TFT's parasitic capacitance). An extra parasitic capacitance of 2 pF observed in experiment is contributed by coupling between metal traces in the layout and, therefore, we add it in parallel to the capacitance in the RLC tank. The quality factor of the inductor is assumed to be 200 at the designed oscillation frequency (for the 1-GHz oscillator presented in [16], the inductor's quality factor is $\sim$224 at 1 GHz).

In Fig. 25(a), the blue line shows the maximum achievable oscillation criterion without the NQS effect, which would

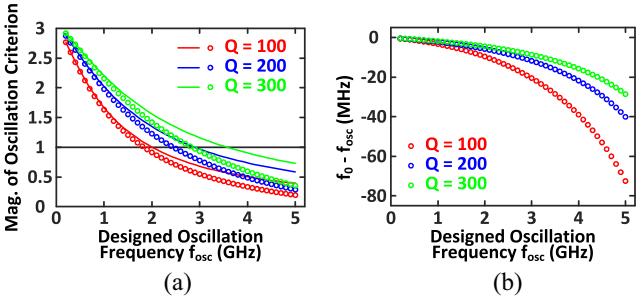

FIGURE 26. (a) Magnitude of the maximum achievable oscillation criterion in function of designed oscillation frequency f_{osc}, for three different quality factors of the inductor Q. Dots show the results when the NQS effect is included, while solid lines show the results when it is not included. (b) Difference between the actual oscillation frequency f_0 and the designed oscillation frequency f_{osc} in function of f_{osc}, for three different quality factors of the inductor Q. The NQS effect is included.

bring the oscillation frequency limit to ∼2.9 GHz. The blue dots correspond to the oscillation criterion for each design point when the NQS effect is incorporated. That reduces the oscillation frequency limit to ∼2.4 GHz (∼17% reduction from 2.9 GHz). Fig. 25(b) shows by how much the actual oscillation frequency is shifted from the designed oscillation frequency, by the NQS effect. The shift becomes more pronounced as the frequency increases. This example makes us advocate that the NQS effect should be incorporated in the design of practical high-frequency LAE circuits and systems, for operation near the device limit.

In our approach to device-circuit co-design, we leverage the high-quality passives available in LAE to enable operation near the device limits. This also requires evaluating the sensitivity to the co-design parameters, most notable the inductor's quality factor in an LC oscillator. To result in a valid oscillator design, near-frequency-limit operation necessitates the accurate analysis of loss sources. The parasitic resistance in series with the inductor, evaluated by the inductor's quality factor, is an important loss source. With lower Q factor, the overall impedance of the RLC tank will have a smaller magnitude at the oscillation frequency, thereby reducing the oscillation-condition margin. As shown in Fig. 26(a), while a higher Q factor improves the oscillation condition, the NQS effect has a greater impact, which highlights its importance when leveraging co-design approaches.

Moreover, with lower Q, the phase of the RLC tank impedance will have a smoother transition between $+90^{\circ}$ and -90°, around $f_{osc} = (1/2\pi\sqrt{LC})$. As shown in Fig. 26(b), this will cause a greater shift, by the NQS effect, of the actual oscillation frequency.

V. CONCLUSION

The goal of the work reported here was to demonstrate GHz operation of systems implemented with LAE technology. Optimizing for high frequency required taking a holistic approach to co-designing TFTs, passives, and circuits that function near the TFT frequency limit. This necessitated raising the TFT performance: by reducing channel length and parasitic capacitances; by leveraging high-quality, low-loss LAE passives in specialized circuit topologies; and by understanding the onset of the NQS effect. In particular, our work showed that the NQS effect, widely considered in high-frequency Si-CMOS systems, will be critical for further pushing LAE systems to the TFT frequency limit. We analyzed this for an LAE oscillator, which serves as a prototypical circuit for high-frequency LAE systems. Complete system demonstrations, while in this work not integrated due to the restricted fab scale, provide compelling evidence for the applicability of LAE technology in Wi-Fi, IoT, and 5G/6G communications.

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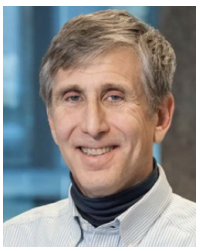
Dr. Wagner received the Nevill Mott Prize for his groundbreaking research, both fundamental and applied, on amorphous semiconductors and chalcopyrites, and the ITC Anniversary Prize for pioneering research on flexible and stretchable large-area electronics, and the comprehensive study of its mechanical behavior. He is a Fellow of the American Physical Society and a Member of the Austrian Academy of Science.



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Prof. Verma is the recipient of numerous teaching and research awards, including several best-paper awards, with his students. He has served as a Distinguished Lecturer for the IEEE Solid-State Circuits Society, and for a number of conference program committees and advisory groups.