

Self-Aligned Amorphous-Silicon TFTs on Clear Plastic Substrates

I-Chun Cheng, Alex Z. Kattamis, Ke Long, *Student Member, IEEE*, James C. Sturm, *Fellow, IEEE*, and Sigurd Wagner, *Fellow, IEEE*

Abstract—We fabricated the first bottom-gate amorphous silicon (a-Si:H) thin-film transistors (TFTs) on a clear plastic substrate with source and drain self-aligned to the gate. The top source and drain are self-aligned to the bottom gate by backside exposure photolithography through the plastic substrate and the TFT tri-layer. The a-Si:H channel in the tri-layer is made only 30 nm thick to ensure high optical transparency at the exposure wavelength of 405 nm. The TFTs have a threshold voltage of ~ 3 V, subthreshold slope of ~ 0.5 V/dec, linear mobility of ~ 1 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, saturation mobility of ~ 0.8 $\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, and on/off current ratio of $>10^6$. These results show that self-alignment by backside exposure provides a solution to the fundamental challenge of making electronics on plastics: overlay misalignment.

Index Terms—Amorphous-silicon (a-Si:H), plastic substrates, thin-film transistors (TFTs), self-aligned process.

I. INTRODUCTION

ELECTRONICS on plastic substrates are attracting much attention, because they are lightweight, rugged, flexible and even deformable [1], [2], and possibly transparent and inexpensive. However, plastic substrates have lower process temperatures, higher coefficients of thermal expansion, lower elastic moduli, and lower dimensional stability than conventional glass substrates. These characteristics pose challenges during the fabrication of amorphous-silicon (a-Si:H) thin-film transistors (TFTs). A particularly serious challenge for large-area fabrication is poor overlay registration [3].

When the stiff a-Si:H TFT device layers are deposited sequentially on a compliant plastic substrate, the dimensions of the substrate change from step to step. This change in size produces errors in overlay registration between consecutive mask levels. The misalignment can be reduced by stress compensation in the device layers [3], by laminating or electrostatically bonding the substrate to a stiff carrier plate [4], by clamping the substrate into a rigid frame [5], or by digitally compensating the masks for substrate distortion [6], [7]. More desirable would be a universally applicable technique that automatically compensates for local or large-area misalignment. A fundamental approach to eliminating overlay misalignment on plastic substrates would be self-alignment, most importantly of source and drain to the gate.

Manuscript received December 16, 2005. This work was supported by the DuPont Company and the New Jersey Commission for Science and Technology. The review of this letter was arranged by Editor J. Sin.

The authors are with the Department of Electrical Engineering and Princeton Institute for the Science and Technology of Materials, Princeton University, Princeton, NJ 08544 USA (e-mail: iccheng@princeton.edu).

Digital Object Identifier 10.1109/LED.2006.870247

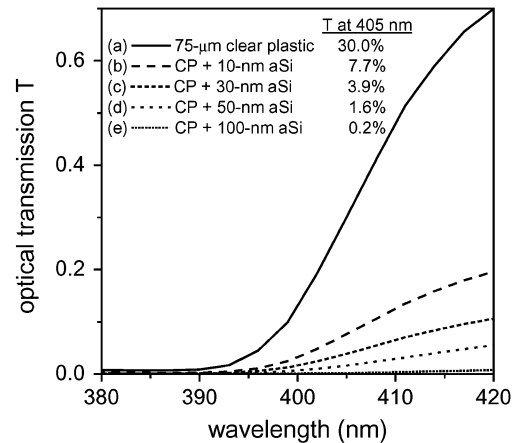


Fig. 1. Optical transmission in the violet and near-UV region of (a) bare 75- μm -thick clear plastic foil, and of clear plastic coated only with (b) 10-nm, (c) 30-nm, (d) 50-nm, and (e) 100-nm-thick i a-Si:H layers. The transmission values at $\lambda = 405$ -nm are (a) 30%, (b) 7.7%, (c) 3.9%, (d) 1.6%, and (e) 0.2%, respectively.

Self-aligned a-Si:H TFTs have been previously demonstrated on glass substrates [8]–[10]. Self-alignment of source and drain to the gate minimizes feedthrough capacitance and facilitates the fabrication of the short-channel TFTs needed for high circuit performance. The self-alignment technique is not widely adopted at present in the display industry, which uses plate glass substrate, because self-alignment needs more steps than the standard back-channel etch process. However, overlay registration will become an important issue in the processing of free-standing substrates of sheets and rolls of plastic. Here we demonstrate that self-alignment is possible on plastic substrates as well. We fabricated conventional inverted a-Si:H TFTs on a clear plastic substrate foil, with the top n^+ a-Si:H source and drains self-aligned to the bottom gate metal.

II. EXPERIMENTS

The TFTs are fabricated on a 75- μm thick experimental clear plastic foil. As shown in Fig. 1, the substrate has an optical transmission T of $\sim 88\%$ in the visible region and an optical absorption edge at $\lambda \cong 400$ nm. The backside exposure photolithography in step 6 of the process sequence of Fig. 2 requires sufficient optical transmission through the substrate and the $\text{SiN}_x/\text{a-Si:H}/\text{SiN}_x$ tri-layer stack at a wavelength available for photoresist exposure. We selected the mercury line at $\lambda = 405$ nm, which is widely used in photolithography. Fig. 1 shows that the clear plastic substrate transmits adequately at $\lambda = 405$ nm. Because the a-Si:H channel layer absorbs strongly, we ex-

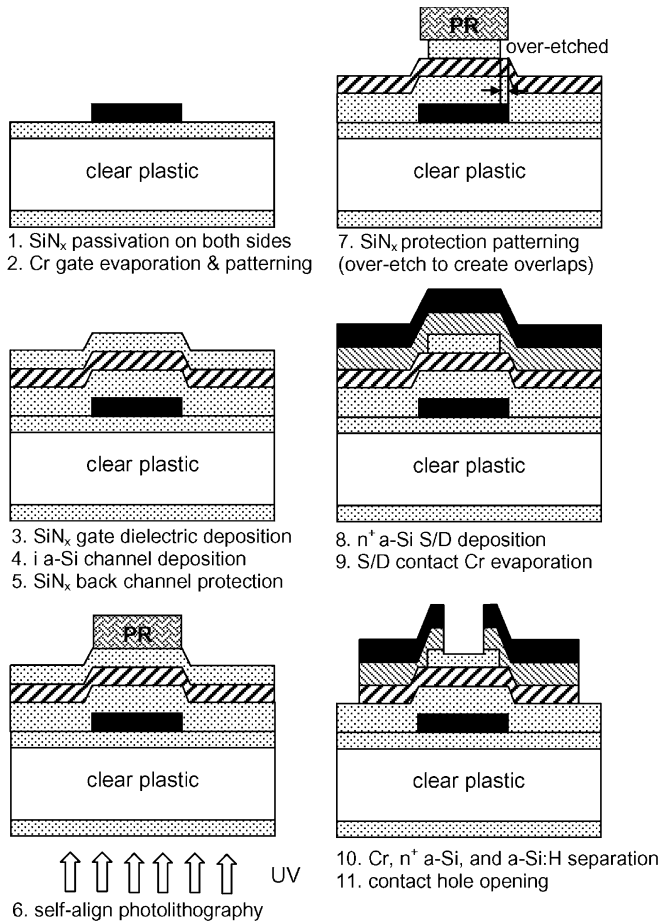


Fig. 2. Process sequence for bottom-gate, back-channel passivated a-Si:H TFTs on clear plastic substrate, with the n^+ a-Si:H S/D self-aligned to the gate. “PR” in steps 6 and 7 denotes “photoresist.”

perimented with a range of a-Si:H thickness, as shown in Fig. 1. To keep the exposure time short, ensure adequate layer uniformity, and prevent interaction with back-channel defects, we made the i a-Si:H layer 30 nm thick. The optical absorption at 405 nm by SiN_x is negligibly small. The exposure time in step 6 of the process sequence of Fig. 2 is ~ 7 min at a UV-light intensity of 2 mW/cm^2 . By using commercially available high-intensity UV sources, this time can be reduced to a few seconds.

The $70 \text{ mm} \times 70 \text{ mm}$ substrate is kept free-standing throughout the entire process, except that it is precisely flattened for photolithography by temporary bonding to a glass plate. We start by coating both sides of substrate with $\sim 300\text{-nm}$ SiN_x passivation layers by plasma-enhanced chemical vapor deposition (PECVD) from a mixture of SiH_4 , NH_3 , and H_2 at a substrate temperature of 150°C [11]. The SiN_x coats seal the substrate against process chemicals and against contaminating the vacuum, and they provide reliable adhesion of the subsequent device layers to the plastic. An 80-nm Cr film is sputtered and patterned into the bottom gate electrode (first mask level). Next, a blanket tri-layer of 300-nm SiN_x / 30-nm i a-Si:H/ 150-nm SiN_x is deposited for gate dielectric/channel/back-channel protection by PECVD as well, at substrate temperatures of $150^\circ\text{C}/180^\circ\text{C}/150^\circ\text{C}$. The i a-Si:H was deposited from a mixture of SiH_4 and H_2 [11]. By backside exposure photolithography using the bottom gate

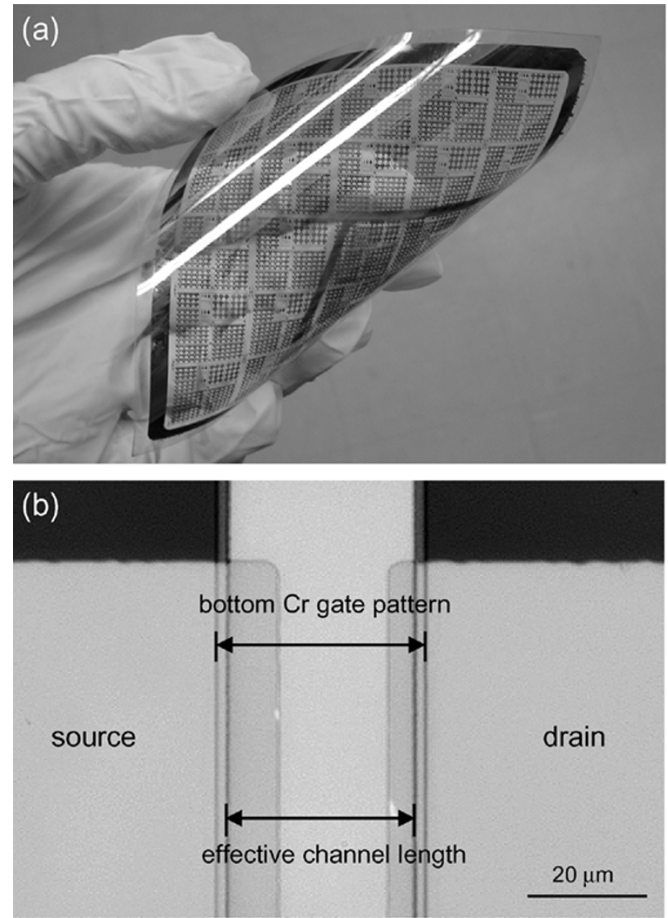


Fig. 3. (a) Arrays of bottom-gate a-Si:H TFTs with self-aligned S/D on a $70 \text{ mm} \times 70 \text{ mm}$ clear plastic substrate. (b) Optical micrograph of one of the TFTs, with S/D-gate overlap of $\sim 1.5 \mu\text{m}$ and an effective channel length of $L_{\text{eff}} \approx 32 \mu\text{m}$. The asymmetric S/D contacts result from overlay misalignment in the second mask level. This misalignment can be eliminated by additional back-side photolithography [9].

electrode as the mask, self-aligned source/drain (S/D) openings are patterned into the photoresist and then wet etched into the top SiN_x layer. A piranha clean ($\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$) and buffered HF ($\text{H}_2\text{O} + \text{NH}_4\text{F} + \text{HF}$) dip ensure clean interfaces between the i a-Si:H channel layer and the subsequently deposited S/D layer. Next, 50-nm n^+ a-Si:H and 100-nm Cr film are deposited and patterned for S/D contacts (second mask level). By slightly overetching the back-channel SiN_x protection layer during the n^+ patterning, the thin blanket i a-Si:H layer outside the TFT region is dry etched as well, to form islands. Finally, holes are opened to contact the bottom gate (third mask level). Fig. 3(a) demonstrates the flexibility of the self-aligned a-Si:H TFT arrays on a $70 \text{ mm} \times 70 \text{ mm}$ clear plastic foil. Because the substrate and the device layers are thin, they do not break when bent [12].

The extent of S/D-gate overlap is determined by the combined effects of; 1) overexposure of the photoresist in process step 6; 2) overdevelopment of the photoresist in step 6; and 3) overetch of the back-channel SiN_x protection layer in step 7. Among these techniques, overexposure of the photoresist provides best control of the degree of overlap on a large surface area. We intentionally overetched the SiN_x protection layer, to create a large overlap for easier study. As illustrated by Fig. 3(b),

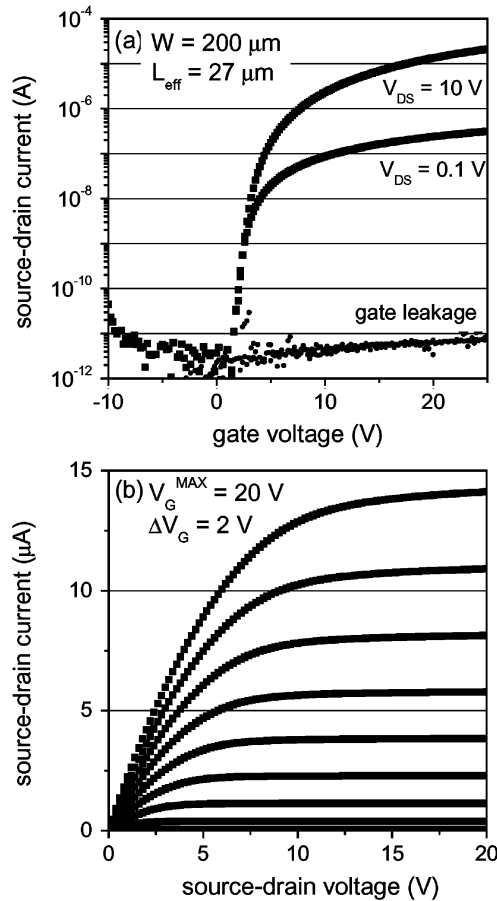


Fig. 4. (a) Transfer and (b) output characteristics of a self-aligned a-Si:H TFT on the clear plastic substrate. The off and gate leakage currents are apparent values set by the sensitivity of the parameter analyzer.

an overetch for 1 min in 10:1 buffered HF produces approximately 1.5- μm overlap.

III. RESULTS AND DISCUSSION

Transfer and output characteristics of a TFT, evaluated with an HP4155A parameter analyzer, are shown in Fig. 4(a) and (b). The electron field-effect mobilities in the linear and saturated regimes are calculated from the transfer characteristics at $V_{DS} = 0.1$ V and 10 V, respectively. We obtain a threshold voltage of ~ 3 V, subthreshold slope of ~ 0.5 V/dec, linear mobility of ~ 1 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, and saturation mobility of ~ 0.8 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$. Both the off current and the gate leakage current are less than the sensitivity of the parameter analyzer of 10^{-11} A. This satisfactory performance shows that self-aligned a-Si:H TFTs can be successfully integrated with plastic substrates.

While gate/S/D self-alignment represents an important step toward a-Si:H TFTs backplanes on free-standing plastic substrates, we view it as only one of several techniques that will be needed to align the critical levels of a large-area flexible display. The gate/(n⁺/Cr) S/D contact alignment in the TFT can

be made precisely by additional back-side photolithography [9]. However, the precise overlay registration of the (n⁺/Cr) layers when used for interconnects remains a challenge.

IV. CONCLUSION

Self-alignment is a very attractive approach to compensating changes in local and large-area dimensions during TFT fabrication on plastic substrates. Self-alignment by backside exposure requires that the plastic substrate plus silicon tri-layer stack be sufficiently transparent at the photoresist exposure wavelength. This requirement can be met if a clear plastic substrate is combined with a very thin a-Si:H channel layer. The performance of the self-aligned TFTs on plastic is equal to the typical TFT performance obtained on glass substrates. a-Si:H TFTs with very thin channel layers perform as well on a plastic substrate as on glass. Our experiments are an important step toward the drop-in replacement of glass plates by plastic foil substrates for a-Si:H TFT based active-matrix backplanes.

REFERENCES

- [1] A. Constant, S. G. Burns, H. Shanks, C. Gruber, A. Landin, D. Schmidt, C. Thielen, F. Olympie, T. Schumacher, and J. Cobbs, "Development of thin film transistor based circuits on flexible polyimide substrates," in *Proc. Electrochem. Soc.*, vol. 94-35, 1995, pp. 392-400.
- [2] P. I. Hsu, M. Huang, Z. Xi, S. Wagner, Z. Suo, and J. C. Sturm, "Spherical deformation of compliant substrates with semiconductor device islands," *J. Appl. Phys.*, vol. 95, pp. 705-712, 2004.
- [3] I.-C. Cheng, A. Kattamis, K. Long, J. C. Sturm, and S. Wagner, "Stress control for overlay registration in a-Si:H TFTs on flexible organic-polymer-foil substrates," *J. Soc. Inf. Disp.*, vol. 13/7, pp. 563-568, 2005.
- [4] F. Lemmi, W. Chung, S. Lin, P. M. Smith, T. Sasagawa, B. C. Drews, A. Hua, J. R. Stern, and J. Y. Chen, "High-performance TFTs fabricated on plastic substrates," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 486-488, 2004.
- [5] A. Kattamis, I.-C. Cheng, K. Long, J. C. Sturm, and S. Wagner, "Dimensionally stable processing of a-Si TFTs on polymer foils," in *Proc. 47th Ann. TMS Electron. Mater. Conf.*, 2005, p. 73.
- [6] W. S. Wong, K. E. Paul, and R. A. Street, "Digital-lithographic processing for thin-film transistor array fabrication," *J. Non-Cryst. Sol.*, vol. 338-340, pp. 710-714, 2004.
- [7] K. Jain, M. Klosner, M. Zemel, and S. Raqhanandan, "Flexible electronics and displays: high-resolution, roll-to-roll, projection lithography and photoablation processing technologies for high-throughput production," *Proc. IEEE*, vol. 93, pp. 1500-1510, 2005.
- [8] Y. Kuo, "A self-aligned, tri-layer, a-Si:H thin film transistor prepared from two photo masks," *J. Electrochem. Soc.*, vol. 139, pp. 1199-1204, 1992.
- [9] D. B. Thomasson and T. N. Jackson, "Fully self-aligned tri-layer a-Si:H thin-film transistors with deposited doped contact layer," *IEEE Electron Device Lett.*, vol. 19, no. 2, pp. 124-126, Feb. 1998.
- [10] C. S. Yang, W. W. Read, C. Arthur, E. Srinivasan, and G. N. Parsons, "Self-aligned gate and source drain contacts in inverted-staggered a-Si:H thin-film transistors fabricated using selective area silicon PECVD," *IEEE Electron Device Lett.*, vol. 19, no. 2, pp. 180-182, Feb. 1998.
- [11] H. Gleskova, S. Wagner, V. Gasparik, and P. Kovac, "150 °C amorphous silicon thin-film transistor technology for polyimide substrates," *J. Electrochem. Soc.*, vol. 148, pp. G370-G374, 2001.
- [12] Z. Suo, E. Y. Ma, H. Gleskova, and S. Wagner, "Mechanics of rollable and foldable film-on-foil electronics," *Appl. Phys. Letters*, vol. 74, pp. 1177-1179, 1999.