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Self-Aligned Amorphous Silicon Thin Film Transistors With Mobility Above 1 $cm^2V^{-1}s^{-1}$ Fabricated at 300°C on Clear Plastic Substrates

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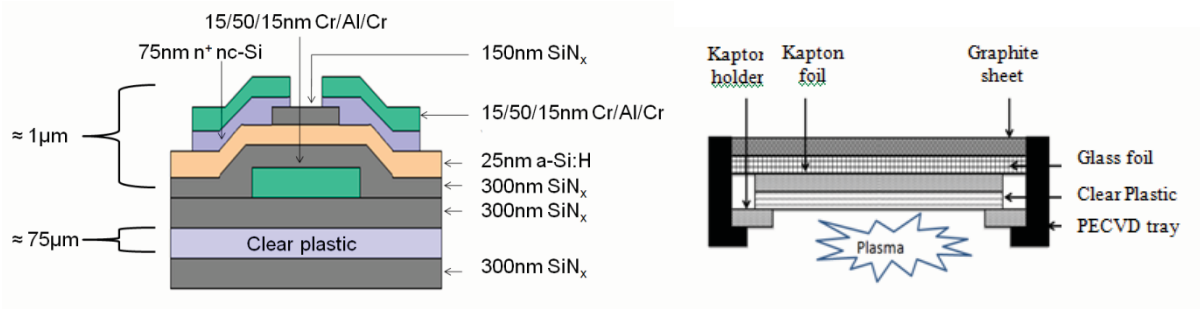
ABSTRACT

We have developed a fabrication process for amorphous-silicon thin-film transistors (a-Si:H TFTs) on free-standing clear plastic substrates at temperatures up to 300°C. The 300°C fabrication process is made possible by using a unique clear plastic substrate that has a very low coefficient of thermal expansion (CTE < 10ppm/°C) and a glass transition temperature higher than 300°C. Our TFTs have a conventional inverted-staggered gate back-channel passivated geometry, which we designed to achieve two goals: accurate overlay alignment and a high effective mobility. A requirement that becomes particularly difficult to meet in the making of TFT backplanes on plastic foil at 300°C is minimizing overlay misalignment. Even though we use a substrate that has a relatively low CTE, accurately aligning the TFTs on the free-standing, 70-micrometer thick substrate is challenging. To deal with this immediate challenge, and to continue developing processes for free-standing web substrates, we are introducing techniques for self-alignment to our TFT fabrication process. We have self-aligned the channel to the gate by exposing through the clear plastic substrate. To raise the effective mobility of our TFTs we reduced the series resistance by decreasing the thickness of the amorphous silicon layer between the source-drain contacts and the accumulation layer in the channel. The back-channel passivated structure allows us to decrease the thickness of the a-Si:H active layer down to around 20nm. These changes have enabled us to raise the effective field effect mobility on clear plastic to values above 1 $cm^2V^{-1}s^{-1}$

INTRODUCTION

Thin-film transistor backplanes made on optically clear plastic substrate foils could find universal use in flexible displays, because they may be employed with any kind of display frontplane, be it transmissive, emissive or reflective. Transistors [1] and displays [2,3,4] on clear plastic substrates have been demonstrated in the past. However, in order to accommodate the low process temperatures of commercial clear polymers [5], the deposition of the a-Si:H TFT stack has been reduced from ~ 300ºC on glass [6,7] to as low as 75ºC [8]. While the initial electrical performance of a-Si:H TFTs fabricated at such ultra-low temperatures is satisfactory, recent experiments have shown poor stability under gate-bias stress [9-12]. In response we have been raising the a-Si:H TFT process temperature on clear plastic [13, 14, 15, 16] to develop a "glass-like" process at 300ºC. This enabled us to achieve "glass-like" TFT stability on plastic.

Our long-term goal is to enable roll-to-roll fabrication – therefore we are working with free-standing substrates. To obtain functional transistors on free-standing plastic foil substrates, the mechanical stress needs to be designed carefully, especially at high processing temperatures [17, 18]. We have used stress control to develop a crack-free TFT fabrication process at 300°C on a clear plastic substrate. However, even if the device layers are crack-free, the stress in the TFT stack causes the substrate to expand or contract (depending on the nature of the combined strain of the total structure), leading to misalignment between consecutive mask layers. After deposition at high process temperatures the subsequent misalignment between mask layers can be very large, causing the TFTs at the edges of the substrate to malfunction. If it is not possible to reduce the total strain in the substrate by engineering the strain, as mentioned above, it becomes necessary to investigate alternative methods to reduce strain-induced misalignment between mask layers. The misalignment can be reduced by laminating or electrostatically



(a) (b)

Figure 1 (a) Schematic of transistor geometry (b) Cross-sectional view of face-down substrate mount for plasma-enhanced chemical vapor deposition.

bonding the substrate to a stiff carrier plate [19], by clamping the substrate into a rigid frame [20], or by digitally compensating the masks for substrate distortion [21].

In our work we focused on developing a self-alignment method which would serve to eliminate overlay misalignment completely. One requirement necessary to implement self-alignment is the ability to expose the photoresist through the back of the substrate. Since the amorphous silicon layer in the TFT stack is very absorptive in the UV wavelength used to develop the photoresist during photolithography, we needed to reduce the thickness of our amorphous silicon channel region as much as possible. Therefore we chose the back-channel passivated TFT geometry shown in Figure 1(a) that allowed us to reduce the a-Si:H layer thickness from our conventional thickness of ~300nm down to ~25nm while still maintaining a rugged TFT fabrication process. In this self-aligned process, the self-alignment is therefore achieved between the gate (mask 1) and the channel passivation (mask 2). An additional benefit of this TFT geometry is that a thinner amorphous silicon layer also results in a lower contact resistance at the source/drain terminals, and therefore a higher measured TFT mobility. We also reduced the source/drain contact resistance by replacing the standard n^+ amorphous silicon (a-Si) in the source/drain contacts with a n^+ nano-crystalline silicon (nc-Si) layer using a layer-by-layer deposition method [22].

In this paper we discuss the fabrication of self-aligned a-Si:H TFTs at 300°C on a clear plastic substrate, the performance of these self-aligned TFTs and the improved alignment that was achieved between the gate and the channel passivation using our self-aligned process.

EXPERIMENT

Substrate preparation

The 7.5x7.5 cm^2 and 75-μm thick optically clear plastic (CP) foil substrates that we use have a working temperature of ≥ 300ºC. Their in-plane coefficient of thermal expansion $\alpha_{substrate}$ is ≤ 10 ppm/ºC, which is sufficiently low to obtain intact device layers in a 300ºC process [23]. A rule of thumb for crack prevention is $(\alpha_{substrate} - \alpha_{TFT}) \times (T_{process} - T_{room}) \leq 0.3\%$. During PE-CVD deposition the substrate is placed in a frame facing downward, and is backed first with Kapton E polyimide foil, then with a glass slide and finally a graphite sheet, as shown in Figure 1(b). The graphite serves as black body absorber for radiative heating in the nominally isothermal PE-CVD pre-heat and deposition zones. This mount lets the substrate expand and contract to some extent during PE-CVD. Following an outgassing anneal at 200ºC in the load lock, the substrate is transferred to the SiN_x deposition-chamber for deposition at 280ºC of a 300-nm thick SiN_x passivation layer on the future device side (front) of the substrate, at an RF (13.56 MHz) power density of 20 mW/cm^{-2}, which puts the SiN_x under tensile stress. The substrate is transferred back to the load lock and flipped to expose its back side. It is then returned to the SiN_xchamber and a 300-nm thick SiN_x passivation layer is deposited at 280ºC on the back side of the substrate at a high plasma power density (90 mW/cm^{-2}), producing compressive stress in the SiN_x.

Transistor Fabrication

Throughout the process the substrate is kept free-standing except that is precisely flattened for photolithography by temporary bonding to a glass plate with water. After our usual substrate preparation, a thermally evaporated tri-layer of 15 nm Cr, 50 nm Aℓ, and 15 nm Cr. is deposited. This bottom metal layer is patterned using conventional photolithography (first mask level). Then the sample is loaded into the PE-CVD system and the following depositions are carried out: (i) a 300 nm thick SiN_x gate dielectric at 300ºC at a power density of 90 mW/cm^{-2}, (ii) a 25nm a-Si:H channel layer deposited at 17 mW/cm^{-2} and (iii) a 150nm thick SiN_x layer as the channel passivation. Now the sample is removed from the PE-CVD system and we carry out the self-alignment step:

First a layer of photoresist is spin-coated onto the sample. Then we then expose the substrate through the back in our mask aligner for 15 minutes at a power density of 3.5mW/cm^2. In this step the bottom gate electrode acts as the mask to self-align the channel passivation to the gate. The SiN_x layer is now wet etched in buffered oxide etch ($HF:NH_4F: H_2O$) for 50 seconds. By slightly over-etching the back-channel SiN_x protection layer during the patterning, the required overlap over the gate is created. A piranha clean (H_2O_2:H_2SO_4) and followed by a short buffered oxide etch dip ensure clean interfaces between the exposed a-Si:H channel layer and the subsequently deposited S/D layer. This concludes the self-alignment step.

Next, a 75-nm n^+ nc-Si:H and a tri-layer of 15/50/15-nm Cr/Al/Cr film are deposited and patterned to form the source/drain contacts (second mask level). This is followed by etching the a-Si:H to isolate individual devices (third mask level). Finally, holes are opened to contact the bottom gate (fourth mask level) completing the TFT process. Details of this process are given in [23]

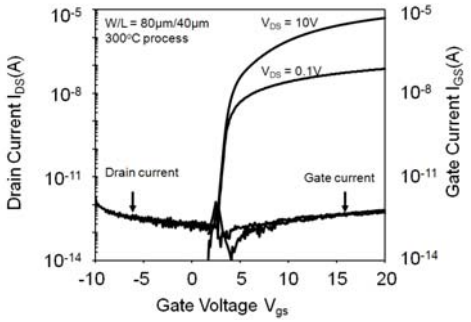


Figure 3 Transfer characteristics of a self-aligned a self-aligned a-Si:H TFT made on clear plastic at 300°C.

DISCUSSION

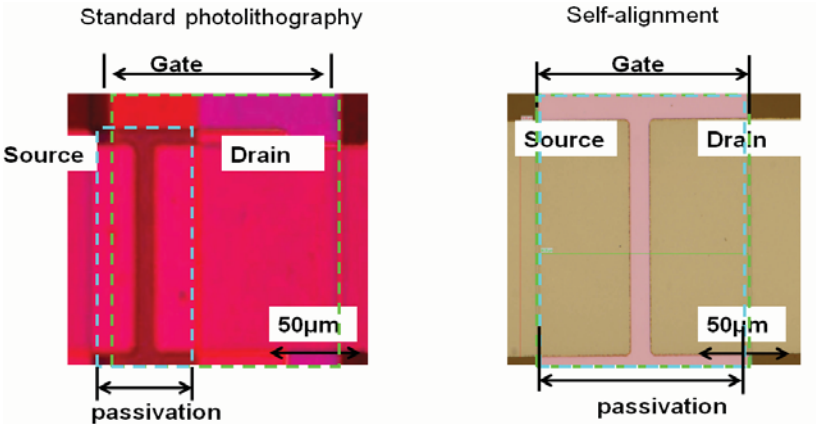
Transistor Evaluation

After fabricating the samples (as described in the previous section) the samples are annealed at 135°C for 30 minutes in air. The TFTs are evaluated and gate-bias stressed using an HP4155A parameter analyzer. For transfer characteristics the gate voltage is swept from 20V to -10V, at 10V drain-source voltage. During gate bias stressing the source and drain are grounded and a positive voltage is applied to the gate for 600 seconds. Then the transfer characteristic is measured again by sweeping the gate voltage from 20V to -10V. This is done for gate bias voltages of 30V to 60V, corresponding to electric fields of (0.9 to 1.8) x 10^8 V/m. The shift in the threshold voltage was determined on the subthreshold slope of the transfer curves at the drain current value of 1 x 10^{-10} A. We use TFTs with a W/L ratio of 80µm/40µm.

Self-aligned TFT measurements

Typical transfer characteristics for back-channel passivated a-Si:H TFTs made using the self-aligned process are shown in Figure 3. On clear plastic the linear mobility is 1.11cm^2/Vs, the saturation mobility 1.08cm^2/Vs, the threshold voltage ~4V, the on/off current ratio > 1x10^7, and the subthreshold slope 350mV/decade. Using a standard photolithography process we achieved linear mobilities of ~ 0.95cm^2/Vs, and saturation mobilities of ~0.96cm^2/Vs mobilities. Clearly the self-aligned process results in high-quality TFTs with higher mobilities compared to the standard photolithographic process.

Figure 4 (a) shows a close-up view of the channel-region is shown for a TFT made with the standard process at the edge of the plastic work-piece - and Figure 4(b) shows another TFT where the channel passivation is patterned using self-alignment. In each picture the gate area is indicated by a green square and the channel passivation area is indicated by a light blue square. In Figure 4(a) the channel passivation has shifted partially off the gate, and the TFT is not functional, while in Figure 4(b) the squares overlap perfectly - showing how the misalignment between the gate and the channel passivation layers has been eliminated. The effective over-etch of the channel passivation (the distance from the edge of the passivation layer to the edge of the gate) is 2µm.



(a) (b)

Figure 4 Optical micrographs showing the alignment between the gate and subsequent layers for (a) a TFT 3cm away from the center of the substrate fabricated using standard patterning, and (b) a TFT which the channel passivation patterned using self-alignment.

CONCLUSIONS

Misalignment between the gate and channel passivation in a back-channel passivated TFT geometry is eliminated by using a self-alignment method. The back-channel passivated TFT geometry allowed us to reduce the amorphous silicon channel resistance down to 25nm, resulting in TFTs with an improved measured mobility. However, since flexible displays will ultimately be fabricated using roll-to-roll fabrication on free-standing web substrates we still need to develop new techniques for aligning the gate with the source/drain contact and the interconnects.

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