Optimum Low-Gate-Field and High-Gate-Field Stability of Amorphous Silicon Thin-Film Transistors with a Single Plastic-Compatible Gate Nitride Deposition Process

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The threshold voltage stability of a-Si thin-film transistors (TFT's) is important both at low and high gate electric fields. Low gate voltage operation is required to drive OLEDs in pixels with low TFT power loss with the TFT in saturation. High gate voltages are needed for maximum gate switching speed [1], as desired for integrated display peripheral drivers. At low gate electric fields, the TFT threshold voltage shift is dominated by breaking of weak Si-Si bonds and electron trapping by the resulting dangling bonds, while at high gate field, electron trapping in the gate nitride dominates [2]. Therefore, different gate nitride processes are conventionally required for the best TFT stability at high and low gate voltages. In this abstract, (i) we demonstrate a single gate nitride deposition process (using standard PECVD growth) which is optimum for stability for both low-field driving and high-field switching applications. Furthermore, (ii) the nitride deposition temperature is limited to 300°C which is compatible with high-temperature clear plastic substrates[3], unlike the previous best low-field results which required 350°C [4].

The degradation of the TFT current at low and high gate electric fields were measured for TFTs grown with either standard or "improved" a-Si (i.e. a-Si grown with hydrogen dilution during PECVD to remove weak Si-Si bonds [4]), and gate nitride grown at either a low (5W) or high (48W) plasma power, grown at 350°C (Fig. 2 and 3). Low field and high field correspond to 7.5V and 80V on a 300-nm nitride, respectively. While using the improved a-Si and the 5W nitride increases the low-field TFT half-life from lower than a month to over 100 years, it does not improve the high-field stability. This is because the high-field stability is limited by charge-trapping in the nitride regardless of the a-Si channel. On the other hand, while the 48W nitride improves the high-field stability, it limits the low-field half-life to lower than a month. We believe the dependence of the low-field stability (a-Si defect formation) on the underlying nitride condition is due to the fact that the nitride microstructure, and thus the a-Si microstructure just above it, depends on the nitride growth condition [4]. Therefore the goals is to improving the nitride quality (fewer electron traps for high field stability) without compromising the quality of the a-Si/nitride interface for low-field stability. We show that this can be achieved by hydrogen dilution during the PECVD growth of the gate nitride.

Si-based defects (dangling bonds) are responsible for deep trapping of carriers in amorphous nitride while the N-based defects mainly contribute to the band-tails [5]. The infra-red absorption spectra of the standard nitride grown at 5W and 48W and the "improved" nitride (grown with hydrogen dilution) at 5W is given in Fig. 4. The presence of Si-H bonds (i.e. passivated Si dangling bond) in the 5W nitride is an indication of a possibly high trap concentration (e.g. Si dangling bonds which require H passivation). The Si-H peak is highly suppressed by increasing the nitride deposition power to 48W as expected [6]. As can be seen, hydrogen dilution has a similar suppressing effect on the density of Si-H bonds. We believe this is because hydrogen radicals can remove the weakly bonded Si atoms during PECVD and result in a lower density of silicon dangling bonds. Stress measurements of the TFT's grown with this "improved" gate nitride (Fig. 5 and 6) show a high-field stability comparable with that of the 48W nitride and a low-field half-life of matching record results of 100 years. The deposition temperature of the improved nitride (300°C) is compatible with high-temperature clear plastic substrates [3].

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Symbol:				
Standard SiNx (5W, 350°C) Standard a-Si	Standard SiNx (48W, 350°C) Standard a-Si	Standard SiNx (5W, 350°C) Improved a-Si	Standard SiNx (48W, 350°C) Improved a-Si	Improved SiNx (5W, 300°C) Improved a-Si

Table I: Description of samples for symbols used in Fig. 2, 3, 5 and 6.

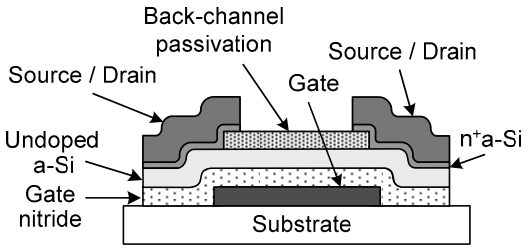

Fig. 1. Schematic cross-section of standard bottom-gate a-Si TFT's.

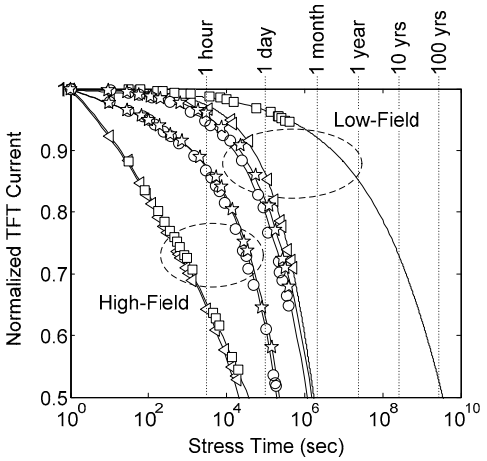

Fig. 2. TFT current decay vs. time at a high (2.5×10^6 V/cm) and a low (2.5×10^5 V/cm) gate electric field.

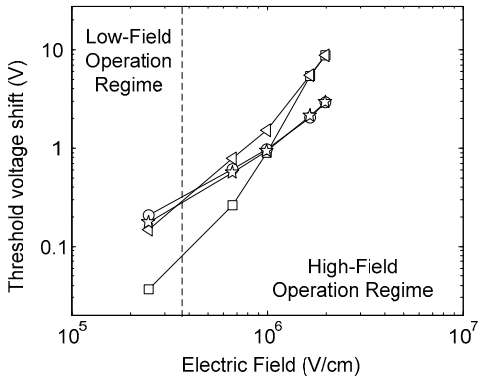

Fig. 3. TFT threshold voltage shift vs. gate stress field after 600 seconds of DC bias stress.

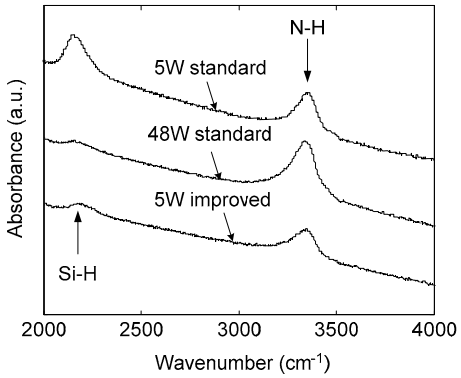

Fig. 4. Infra-red absorption spectra of the nitride films grown at different conditions.

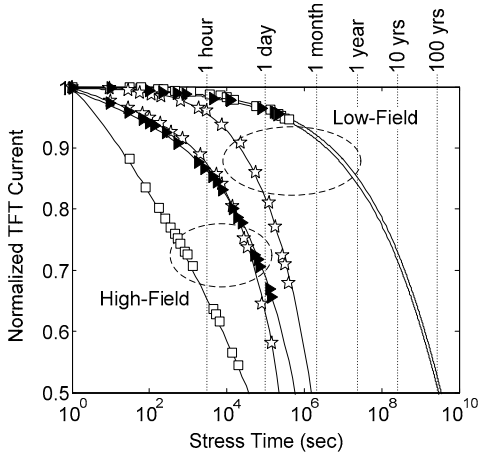

Fig. 5. TFT current decay vs. time at a high (2.5×10^6 V/cm) and a low (2.5×10^5 V/cm) gate electric field. Note that the "improved" nitride condition (►) has optimum reliability at both high and low electric fields.

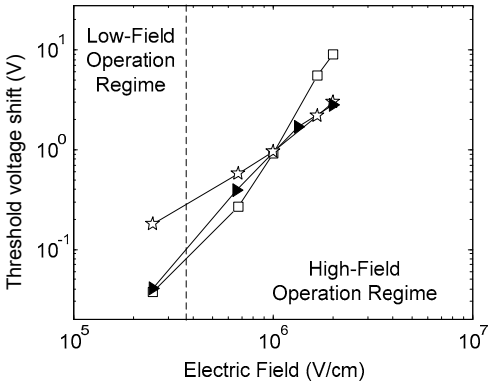

Fig. 6. TFT threshold voltage shift vs. gate stress field after 600 seconds of DC bias stress. Note that the "improved" nitride condition (►) has optimum reliability at both high and low electric fields.

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