Hybrid LAE-CMOS Force-Sensing System Employing TFT-Based Compressed Sensing for Scalability of Tactile Sensing Skins

Levent E. Aygun, *Student Member, IEEE*, Prakhar Kumar, *Student Member, IEEE*, Zhiwu Zheng, *Student Member, IEEE*, Ting-Sheng Chen, *Student Member, IEEE*, Sigurd Wagner, *Fellow, IEEE*, James C. Sturm, *Fellow, IEEE*, and Naveen Verma, *Member, IEEE*

***Abstract*—Tactile sensing requires form-fitting and dense sensor arrays over large-areas. Hybrid systems, combining Large-Area Electronics (LAE) and silicon-CMOS ICs to respectively provide diverse sensing and high-performance computation/control, enable a platform for such sensing. A key challenge is that hybrid systems require a large number of interfaces between the LAE and CMOS domains, particularly as the number of sensors scales. This paper presents an architecture that exploits the attribute of signal sparsity, commonly exhibited in large-scale tactile-sensing applications, to reduce the interfacing complexity to a level set by the sparsity rather than the number of sensors. This enhances scalability compared to sequential-scanning and active-matrix approaches. The architecture implements compressed sensing via thin-film-transistor (TFT) switches, and is demonstrated in a force-sensing system with 20 force sensors, a TFT die (with 161 ZnO TFTs) per sensor, and a custom CMOS IC for system readout and control. Acquisition error of 0.7 $k\Omega_{RMS}$ is achieved over a 100 kΩ-20 kΩ sensing range, at energy and rate of 2.46 μ J/frame and 31 fps.**

***Index Terms*—Compressed sensing, Hybrid Systems, large-area electronics (LAE), sensing systems, thin-film transistor (TFT), ZnO TFTs.**

I. Introduction

TACTILE sensing involves sensing by direct contact or interaction with embedded signals. It has a wide range of applications, such as touch sensitive displays [1], high-resolution structural monitoring [2], and electronic skins for prostheses and robotics [3]–[6]. As an example, electronic skins emulate the sensing capabilities of mechanoreceptors in the human somatosensory system [7], [8]. Prostheses can be used to mimic the mechanical movements of body parts, controlled by electrophysiological signals encoding human movement intentions (e.g., electromyographic signals [9], [10], peripheral/central nervous system action/field potentials [11], [12]). In such systems, closed-loop feedback going beyond just the human visual system [13], is showing increasing value for dexterous grasping [14], [15] and elimination of phantom pain following a limb loss [16]. For instance, electronic skins restore the sense of touch to users. Fig. 1(a) shows such a system where pressure signals from a prosthetic hand are converted to neuromorphic signals and fed back to a transhumeral amputee via transcutaneous electrical nerve stimulation [3]. Although only three pressure sensors were integrated per finger, the user was able to distinguish objects with different curvature and feel pain when touching sharp objects.

Fig. 1(b) shows the advancement to a tactile force-sensing glove, integrating an array of 548 force sensors which enables

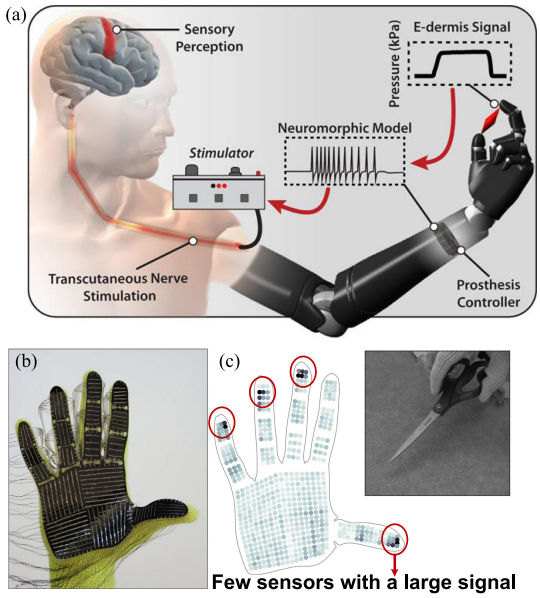


Fig. 1. Electronic skin demonstrations, including: (a) prosthesis with tactile sensor feedback, which sends pain and touch signals to user [3]; (b) smart glove with 548 force sensors for identifying objects handled by robots [6]; (c) sensor array response map when scissors are held as shown in inset. In these demonstrations only a few sensors in contact with the object are excited.

Manuscript received July 13, 2019; revised September 12, 2019; accepted October 10, 2019. Date of publication October 21, 2019; date of current version December 31, 2019. This work was supported by the Semiconductor Research Corporation (SRC), DARPA, Princeton Program in Plasma Science and Technology, and Princeton University. IC Fab provided by MOSIS. TFT circuits fabricated at the cleanroom of the Princeton Institute for the Science and Technology of Materials (PRISM) at Princeton University. This paper was recommended by Associate Editor Prof. P. Mohseni. *(Levent E. Aygun, Prakhar Kumar, and Zhiwu Zheng contributed equally to this work.) (Corresponding author: Levent Aygun.)*

The authors are with the Princeton University, Princeton, NJ 08544 USA (e-mail: laygun@princeton.edu; prakhark@princeton.edu; zhiwuz@princeton.edu; tsc@access.ee.ntu.edu.tw; wagner@princeton.edu; sturm@princeton.edu; nverma@princeton.edu).

Color versions of one or more of the figures in this article are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TBCAS.2019.2948326

classification of touched objects [6]. An example case of holding a pair of scissors shows sensors in direct contact with the object generate large response, thus giving high sensitivity, while sensors even a few millimeters away generate small response, thus giving high spatial selectivity. This substantially enhances the ability to discriminate between objects and object types during touch classification.

We note a general requirement benefiting tactile sensing systems, namely the need for dense spatial sensing over the potentially large areas the embedded signals are distributed. This in turn implies the need for a large number of sensors. However, we also note a typical attribute of such tactile-sensing applications. Namely, the data over all the sensors is often sparse [17]. As seen in Fig. 1(b), a small number of the force sensors is excited during contact with objects. The sensors are deployed for spatial resolution and high sensitivity, not because signals are expected on all sensors at any given time. While a technology for large-scale sensing is thus required, the attribute of sparsity can be exploited to address architectural complexity.

For large-scale form-fitting sensing, Large-Area Electronics (LAE) is a distinctive technology. LAE is based on low-temperature processing ($\leq 200\ ^{\circ}$C) of thin films, enabling compatibility with a wide range of materials for forming diverse transducers and for fabricating such transducers on large and flexible substrates. LAE is currently driven by display applications employing 10 m^2 substrates during fabrication, with the industry steadily reducing cost per area [18] and moving to flexible substrates [19].

Recently, there has been interest in expanding to broader sensing applications [21]–[24], which require control and computation functionality over the many sensor channels. For this, low-temperature thin-film transistors (TFTs) are possible in LAE based on various semiconductors, and a range of TFT circuits for sensing applications have thus been demonstrated [25]–[29]. However, compared to Si-CMOS transistors, LAE TFTs exhibit orders-of-magnitude lower performance and energy efficiency, having much larger feature sizes (channel lengths of 1–10 μm) and much lower cutoff-frequencies (f_T and f_{MAX} of 1–100 MHz [30]–[34]).

Therefore, this work focuses on a hybrid-systems approach [35], wherein LAE, for large-area form-fitting sensing, is combined with Si-CMOS ICs, for centralized control and computation. As shown in Fig. 2, the key challenge that emerges with hybrid systems is the large number of interfaces required between the LAE and CMOS domains, especially as the number of sensors scales. Thus, TFTs are used selectively to address the interfacing. This has also been the approach in today's displays [36], where a TFT-based active matrix is used for pixel accessing.

In this paper, which is an extended version of [37], the attribute of signal sparsity in tactile sensing is exploited to efficiently achieve much greater reduction in the interface complexity. Section II overviews the approach, based on compressed sensing. Section III describes the system architecture, design of sensing, compression, and readout sub-blocks. Section IV presents the tactile-sensing system prototype for a force-sensing application, consisting of 20 array elements, in-house fabricated

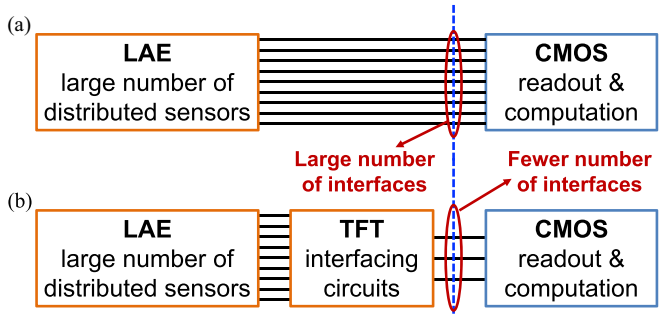


Fig. 2. Illustration of hybrid-system approach, showing: (a) primary integration challenge due to large number of LAE-CMOS interfaces; and (b) use of LAE TFTs to mitigate interfacing challenge.

TFT-based compression blocks, and a custom CMOS IC for readout and control. Finally Section V concludes.

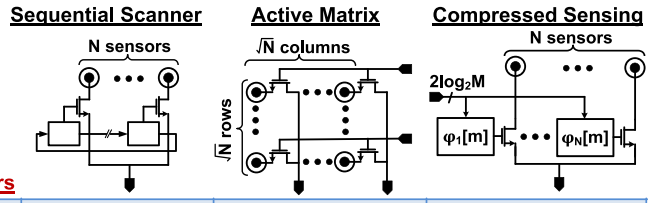
II. System Overview and Rationale

Fig. 3 illustrates previous and the proposed interface-reduction approaches, and compares their scaling behaviour with respect to the number of sensors N and each sensor's bandwidth B, based on the following critical system metrics of interest. The number of access cycles required determines the latency to readout the sensor array, or, relatedly, sets the required cycle speed to accommodate the sensors' bandwidth. The number of interfaces between LAE and CMOS domains sets the hybrid-system complexity. The dynamic range of each interface sets the CMOS-readout complexity. Finally, the number of TFTs required per sensor sets the LAE complexity. The following subsections analyze the previous and proposed approaches, with respect to the number of sensors N.

A. Previous Interface-Reduction Approaches

The simplest previous approach is a sequential scanner, where each sensor is selected one at a time via access-TFTs and a TFT-based scan chain [20]. This reduces the interface complexity to a single output and a few input control signals. However, the number of cycles required to readout all sensors is on the order of the number of sensors N. The most common previous approach is an active matrix, typically used in displays, where row (gate) control lines are enabled one at a time, and thus $\sqrt{N}$ sensors are accessed at once on parallel vertical (data) lines. This reduces LAE complexity to just the access-TFTs and reduces the number of access cycles by a square-root factor. But, it requires $2\sqrt{N}$ row and column interfaces.

Recently, an interface-reduction architecture was demonstrated [38] that uses TFT-based digitally-controlled oscillators (DCOs), where each sensor modulates the amplitude of a DCO in the selected frequency channel and each DCO follows a unique frequency-channel hopping sequence set by an input code from CMOS. From this, the individual sensor outputs can be separated, and the number of accessible sensors (i.e. unique hopping patterns) exhibits combinatorial scaling with the number of interfaces. Thus, compared to an active matrix, the number of interfaces and access cycles is significantly reduced.



System Metrics for N sensors	Sequential Scanner	Active Matrix	Compressed Sensing
# Cycles	N	$\sqrt{N}$	M (<<N)
Required Cycle Speed (for Sensor Bandwidth B)	N×B	$\sqrt{N}$×B	M×B
# LAE/CMOS Interfaces	~4	$2\sqrt{N}$	$1 + 2\times\log_2 M$
Required Dynamic Range (a.u.)	1	1	K
# TFTs per Sensor	~5	1	$1 + M\times\log_2 M$

Fig. 3. Consideration of system metrics, with respect to number of sensors N, for different interface-reduction architectures, including sequential scanner [20], active matrix, and compressed sensing (this work).

While superposition of sensors within the frequency channels increases the dynamic range, the increased CMOS complexity is a preferred trade-off, given the relative efficiency of processing in the CMOS domain. Rather, the primary challenge is that the frequency channels required within the TFT DCOs raise the need for specialized TFT design and processing to achieve high frequency [38].

Importantly, none of the previous interface-reduction approaches exploits sparsity in tactile sensing data. While previously, compressed sensing has been leveraged in a hybrid system to meet signal sampling-rate requirements [25], the proposed approach described next aims to more broadly address the set of hybrid-system metrics outlined.

B. Interface Reduction Based on Compressed Sensing

Consider a tactile sensor array with N elements and K-sparse data, meaning that only K sensors have non-zero values ($K \ll N$). Under specific conditions, the theory of compressed sensing says it is possible to determine the K values by taking M measurements, where M is $\mathcal{O}(K \log N/K)$ [39], scaling primarily with sparsity K and only weakly with the number of sensors, N. This means the sparse sensor data to the CMOS domain can be significantly compressed. A particularly important advantage is that these M measurements can be obtained by taking random binary superpositions. As shown in Fig. 4(a), this simply requires matrix multiplication of sensor data represented as a vector $\vec{x}$ by a measurement matrix Φ, where the matrix entries are Bernoulli random variables. Such matrix multiplication can be implemented using simple TFT switches, readily within the performance limitations of the technology.

Fig. 4(b) shows a block-level diagram of such an implementation. Each sensor is connected via an access TFT to a common node, yielding the output $y[m]$. When on, the access-TFTs superimpose their sensor currents, yielding an element y_m of the vector $\vec{y}$. Acquisition of all vector elements, then simply requires M measurement cycles, turning each access TFT ON/OFF according to the M matrix-column entries φ_n for the corresponding sensor x_n. For example, during the first measurement cycle ($m = 1$), $\varphi_1[1] = 0$ and $\varphi_N[1] = 1$, so the

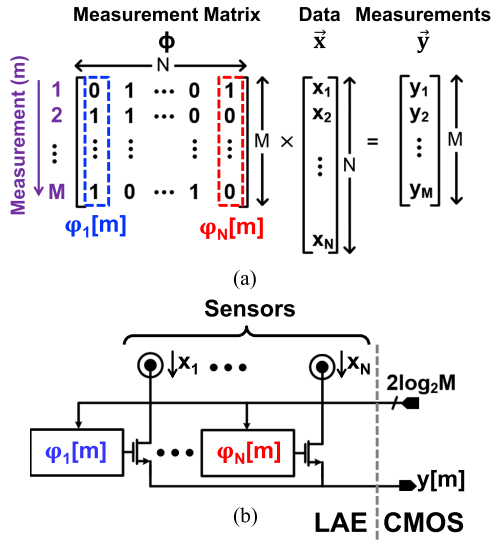


Fig. 4. Compressed-sensing-based interface-reduction approach, involving: (a) simple measurement matrix Φ to take random superpositions from sensor data $\vec{x}$ to reduce data size from dimensionality of N to M ($M \ll N$); and (b) implementation of measurement matrix in LAE domain, simply by switching access-TFTs on/off, depending on corresponding column of Φ to superimpose sensor currents at output node to CMOS domain.

corresponding access-TFTs are turned off and on, respectively. Repeating this for all m measurement cycles, implementing Φ simply requires controlling each access-TFT according to the corresponding columns of φ_n (implementation of this control circuit will be described in Section III-B).

Fig. 5 compares the scaling behaviours of interface-reduction approaches for two key system metrics: (1) number of LAE/CMOS interfaces; and (2) number of access cycles. Points near the bottom-left are preferred, as the number of sensors N scales. For a sequential scanner, the number of access cycles scales with N. For an active matrix, both the access cycles and the number of interfaces scale with $\sqrt{N}$. On the other hand, with the compressed-sensing approach, these both scale just with the sparsity K, which can be very small in applications, leading to a small number of access cycles and interfaces. In fact, even as

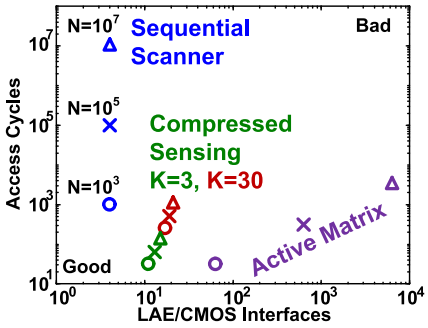


Fig. 5. The number of LAE-CMOS interfaces and acquisition cycles for various interface-reduction architectures as the number of sensors N scales from 10^3 to 10^7 (shown with different markers). A "good" technology has a low number of access cycles and a low number of interfaces.

the sparsity increases from 3 to 30, these metrics increase only very modestly, as shown, remaining small compared with the previous approaches.

The system metrics are summarized in Fig. 3. The number of interfaces and acquisition cycles are small, scaling with M ($\ll N$), related to the level of sparsity K, not the potentially large number of sensors. Further, the reduced number of acquisition cycles can be leveraged to enable slower cycle speed, based on Nyquist-sampling considerations for a given sensor bandwidth B. However, the next two metrics expose challenges. First, taking superpositions causes the output dynamic range to go up with the level of sparsity (i.e., non-zero sensor values). In practice, small K makes this tolerable, and further it pushes readout complexity to the CMOS domain, which is more efficient and thus preferred. Second, as will be quantified in Section III-B, a significant number of TFTs are needed for controlling the access-TFTs, according to the columns of Φ. This raises system-yield concerns. However, as will be shown in Section III-B, the statistical nature of compressed sensing affords substantial tolerance to TFT faults, alleviating such concerns in sensing applications.

Two aspects of our proposed system raise power consumption. One, increasing the number of TFTs increases the switched capacitance, hence raises power consumption in the LAE domain. Two, a higher readout dynamic range requirement leads to a corresponding increase in the energy per readout operation. However, prototype measurements (Section IV-D) highlight the importance of analyzing power consumption at the full system level, which includes the significant CMOS readout energy. Because compressed-sensing substantially reduces the number of readout operations from N in the other approaches to M (determined by sparsity) in our case. the overall power consumption of the system will be substantially reduced. Estimates made using the prototype energy numbers support this expectation.

III. System Design

Fig. 6 shows the system architecture, composed of three blocks: (1) the large-area sensor array, based on 20 off-the-shelf thin-film force sensors; (2) compressed-sensing block, based on in-house fabricated zinc-oxide (ZnO) TFTs; (3) readout-and-control block, based on a custom CMOS IC. The system is designed for a level of sparsity $K = 3$, and can support up to

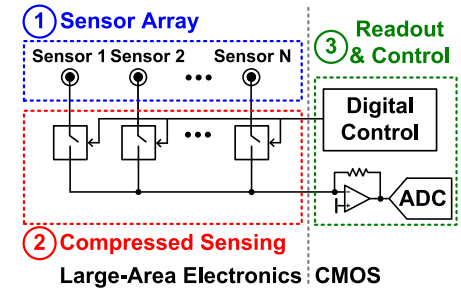


Fig. 6. System architecture where random binary superpositions of sensor currents are taken in LAE domain and fed to CMOS domain for readout and sparse data reconstruction.

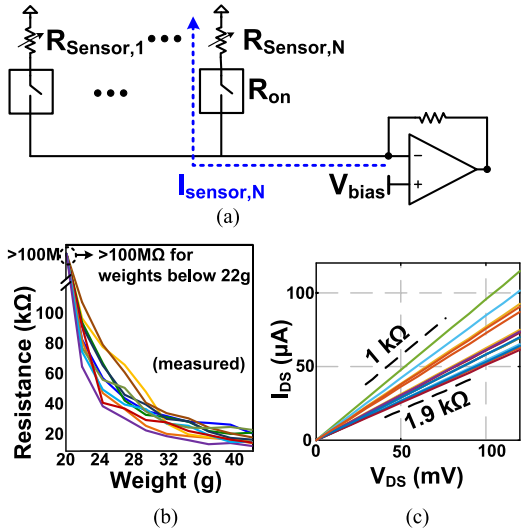


Fig. 7. Sensor analysis, based on (a) architecture wherein currents from selected sensors are read out by transimpedance amplifier, with $I_{\text{Sensor},\,N} = V_{\text{Bias}}/(R_{\text{Sensor},\,N} + R_{\text{on}})$. (b) Measured responses from 10 force sensors show $R_{\text{Sensor,min}} \approx 20$ kΩ, establishing access-TFT design condition, where TFT on resistance should be much smaller than the force sensor resistance ($R_{\text{on}} \ll R_{\text{Sensor}}$). (c) This is verified by the measured I-V characteristics of ZnO access-TFTs ($W/L = 600/3$ μm), showing $R_{\text{on}} \leq 2$ kΩ $\ll R_{\text{Sensor, min}}$.

120 sensors by taking 32 measurements over a single output interface and 5-bit (differential) control interface. We chose $K = 3$, a value sufficient to demonstrate the interface-reduction benefits of the architecture without overly raising the prototypes complexity. Next, the details of each block are described.

A. Force Sensing Array

The sensor array consists of commercial thin-film piezo-resistive force sensors [40]. These have the measured response shown in Fig. 7 with resistance changing from 20 kΩ to 100 kΩ for weights in the range of interest of 24 g to 40 g. For masses below 22 g, the measured OFF resistance of the force sensors is >100 MΩ. This very high OFF resistance is important for unequivocally establishing data sparsity in tactile sensing. Though significant variation is observed across the different sensors shown, this is often tolerable thanks to the large responses expected in tactile sensing due to the proximity of sensors to the

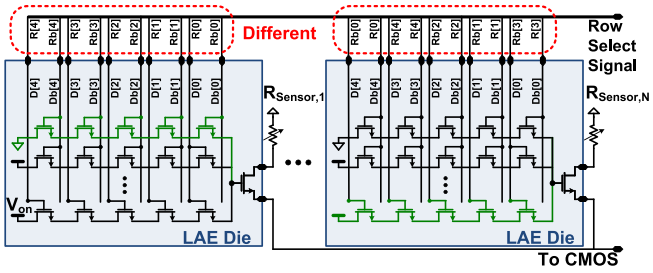


Fig. 8. Implementation of compressed sensing block on LAE die, consisting of an access TFT and matrix-TFT control circuit, to implement switching according to Φ via 32 TFT branches. The TFT block is the same on all die but the connection of the column lines to the row-select signal varies for each sensor.

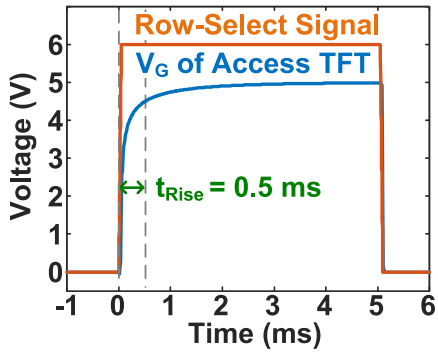


Fig. 9. Simulation showing speed of matrix TFTs switching access-TFT's gate voltage.

embedded signals. The system performs readout via a CMOS transimpedance amplifier (TIA) circuit, whereby sensors are selected by access-TFTs and their currents are superimposed. The sensor response sets the access-TFT requirements. The TFT on-resistance (R_{on}) should be well below the sensor resistance (R_{Sensor}), to ensure the sensed current is set by the sensor and not the TFT. Based on this, ZnO TFTs with channel width/length of 600/3 μm are used, which keeps R_{on} below 2 kΩ, as shown in the measured $I_{\text{DS}} - V_{\text{DS}}$ curves.

B. Compressed Sensing Circuit

Compressed-sensing acquisition is achieved via the circuit shown in Fig. 8. In a future product technology, the TFT compression circuit for each sensor would be directly fabricated on a large-area flexible backplane hosting the sensors. However, in this research-scale project, the TFT compression circuit for each sensor was fabricated on a separate glass die (10 mm $\times$ 6 mm). Each LAE die is associated with a sensor, and comprises 32 branches of NMOS pass-transistor-logic TFTs, referred to as matrix TFTs, which provide a gate bias to an access TFT. A differential row-select control signal $R[4:0]$ from CMOS is used to sequentially cycle through the 32 branches. In this way, each LAE die implements a column of Φ with 32 rows, invoking the matrix elements one row at a time. Such a Bernoulli measurement matrix enables over 1000 sensors with the target sparsity of $K = 3$.

To implement the different columns required for each sensor, the gate-bias enabled by each row could be configured accordingly in the LAE die. However, to enhance modularity and minimize system-assembly complexity, each die is kept identical and the bias as well as control signals are provided by distribution and bonding on a PCB. In this case, 32 bonds would be required for the gate-bias. Instead, an approach is adopted where the gate-biases are kept fixed between die, and instead the control-signal $R[4:0]$ connections are configured differently between die. In this case, different branches are selected in each die for a given control signal $R[4:0]$, yielding unique columns φ_n of Φ. This reduces the need for the 32 individual gate-bias bonds to 2, ground and V_{on}. Both approaches still require $5 \times 2 = 10$ row-select signal bonds and 2 bonds for connecting sensor to CMOS.

Illustration of two different column implementations φ_1 and φ_N are shown in Fig. 8. For $R[4:0] = 00000$, in die 1 the first branch is enabled, feeding ground to the access TFT, while in die N the last branch is enabled, feeding V_{on} to the access-TFT. The measurement matrix Φ can in general have many unique columns and support over 1000 sensors (as observed from reconstruction algorithms for $M = 32$ and $K = 3$). Here, to ease prototype design and testing, a fixed matrix-TFT die is employed for all sensors. The unique access-TFT control sequence required is then achieved by varying the connections between the bits of the row-control signal $R[4:0]$ and the bits of the die-control signal $D[4:0]$. This fixed-die scheme can support only $5! = 120$ unique connection schemes, corresponding to 120 unique columns, still much greater than the number required for a conclusive prototype system demonstration.

Next, design details are analyzed, included the acquisition rate possible with the pass-transistor circuits and the susceptibility to faults with the larger number of TFTs (160 matrix TFTs and 1 access TFT) per die.

1) Sensor Acquisition Rate: For the implementation described, a measurement frame comprises 32 readout cycles, one for each row of Φ. Due to self-compensation of native defects in ZnO technology [41], it lacks p-type channels, only NMOS-circuitry can be implemented with ZnO TFTs. The period of each readout cycle is limited by how fast a branch of NMOS matrix-TFTs can charge up the gate capacitance of an access TFT, with the reduced over-drive voltage during charge-up. For the chosen sizing of the access TFT (600 μm/3 μm, from the analysis in Fig. 7) and the typical gate-source overlap of 5 μm, the gate capacitance is roughly 7 pF. From the simulation shown in Fig. 9, the worst-case rise time is specified as 0.5 ms. This contributes to the eventual acquisition frame rate (62.5 frames/sec.).

2) TFT Faults: The large number of TFTs required for compressed sensing raises a yield concern. However, analysis should be based on the algorithms for sparse reconstruction used in compressed sensing, whose statistical nature enables substantial tolerance to TFT faults. Fig. 10 shows typical TFT faults that occur in fabrication, as well as their effects on Φ and our application metric of interest, namely data-reconstruction signal-to-noise ratio (RSNR). High RSNR, above 15 dB is often targeted in tactile-sensing applications.

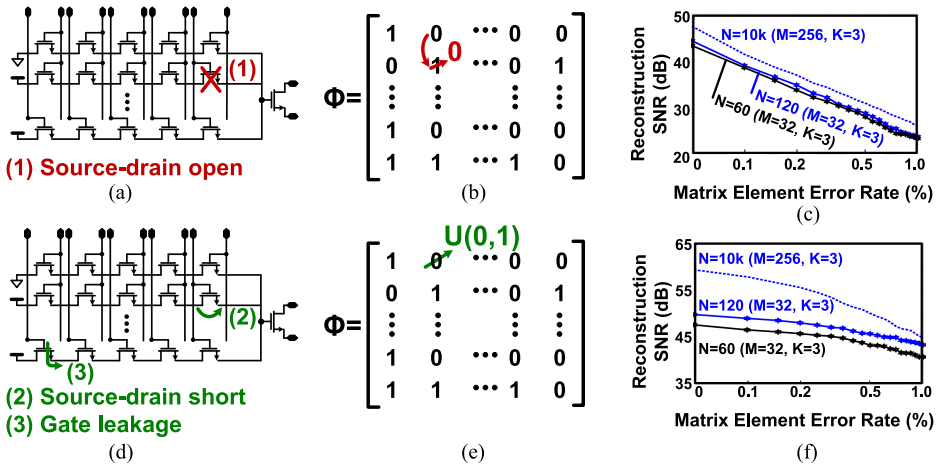


Fig. 10. Matrix TFT fault models, their effects on the Φ matrix, and analysis of impact on sparse data reconstruction performance.

The first fault is source/drain open [Fig. 10(a)], which essentially causes failure of a TFT to turn on, resulting in a high-impedance connection. This is modeled as an element of Φ erroneously retaining its value from the previous readout cycle [Fig. 10(b)]. In this case, we see that high RSNR, above 15 dB, is maintained to very high matrix-element error rates [Fig. 10(c)]. Two other typical TFT faults are source-drain short and gate short [Fig. 10(d)], where TFTs cannot be turned off completely. These are modelled as a corresponding Φ element to erroneously take an intermediate value [Fig. 10(e)]. Again we see that high RSNR is maintained to very high matrix-element error rates [Fig. 10(f)]. However, it should be noted that gate shorts with high levels of current can additionally degrade the logic level of a row-select control-signal bit $R[4:0]$, potentially affecting all LAE dice in the system. Thus, avoiding high-current gate-stack failures of this type is critical, and forms a focus of TFT optimization and yield monitoring. These simulations show that the access-TFT fault requirements, which are the same as those for typical active matrices, would likely dominate the overall yield requirements, despite the large number of matrix TFTs.

The fundamental thermal noise from TFT operation is expected to be negligible compared to practical noise sources such as leakage currents, faults, and reconstruction (Section III-B2). An ON access TFT introduces thermal noise equivalent to a 2 kΩ resistor. Assuming low sensor resistance (worst case), the introduced noise is $26nA_{\mathrm{RMS}}$ over the TIA bandwidth, which would cause a $30\Omega_{\mathrm{RMS}}$ error, much less than that measured from reconstruction noise (Section IV-D).

C. CMOS Readout and Control

Fig. 11 shows a block diagram of the CMOS readout channel implemented in this work. There are 8 such channels, to support system scalability via parallel compressed-sensing subarrays, where each channel can support ∼120 sensors. Each channel includes an opamp-based TIA and 10-bit successive-approximation-register (SAR) ADC, as well as digital control to generate the row-select control signal to LAE. In addition,

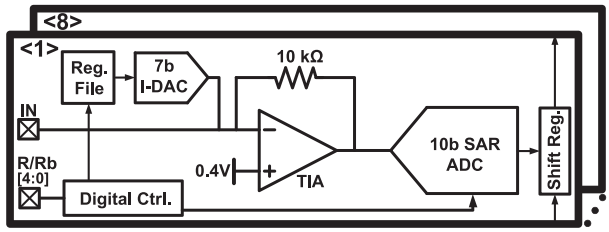


Fig. 11. Block diagram of the CMOS readout channel, with 8 parallel channels supporting 120 sensors each.

there is an offset-cancellation current DAC at the input, to cancel systematic input currents that would otherwise affect the assumption of signal sparsity.

1) Transimpedance Amplifier: Fig. 12 shows the 2-stage opamp design used to implement the TIA. The opamp is a standard differential pair with single-ended output, followed by a common-source stage. Series RC-based pole splitting is employed for opamp stability. Stability of the TIA is a crucial system-design consideration when it is interfaced with the LAE subsystem. A large capacitance at the TIA input can potentially cause it to become unstable by reducing the phase margin, even though the opamp may be unity-gain feedback stable. Specifically, Fig. 12 shows that each LAE die interfaces to the CMOS TIA via an access TFT. Each access TFT's gate-to-source capacitance contributes 7 pF at the TIA input. Since the system can support up to 120 sensors, this implies a total of 840 pF load capacitance at the TIA input. In order to ensure TIA stability when 120 sensors are interfaced, a feedback capacitor, C_f is employed for compensation. Fig. 12 plots the loop gain and phase of the TIA with a feedback capacitance of 200 pF and resistance of 1 kΩ resistor, for varying load capacitance at the TIA input. An acceptable phase margin above 45° is maintained for loads up to 840 pF. We note that, as a general design principle in hybrid systems, it is critical to consider the capacitive loading from the LAE domain on CMOS readout circuitry. Moreover, the input-node parasitic capacitance seen by the TIA is relatively fixed. It is essentially set by the number of access TFTs (i.e., their

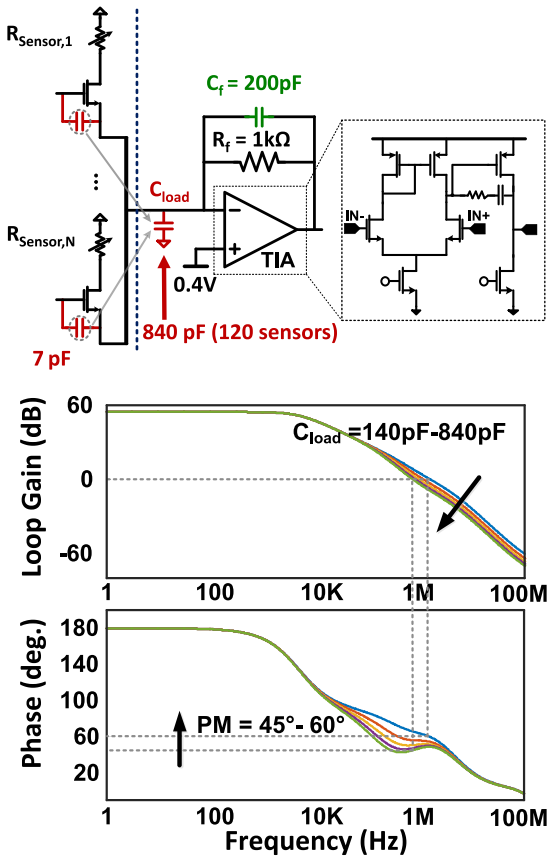


Fig. 12. Transimpedance amplifier design and stability analysis for 120 sensors.

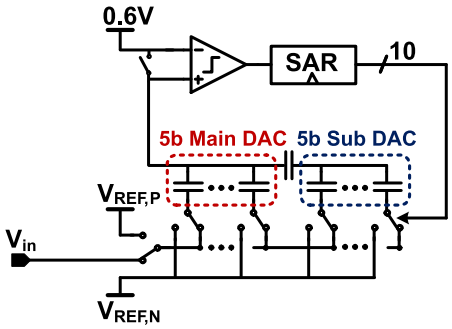


Fig. 13. SAR ADC with 200 fF unit capacitance.

gate-source capacitance). Thus, the TIA frequency response can be optimized for the desired number of sensors in a given system to ensure stability.

The large input capacitance causes noise gain at the output of the TIA. The measured input referred noise for the TIA for an input capacitance range of 140 pF - 840 pF varies from $3.8nA_{RMS}$ to $4.2nA_{RMS}$ over the TIA bandwidth, once again well below that measured from reconstruction error.

2) SAR ADC: The TIA is followed by a 10-bit SAR ADC, shown in Fig. 13. This employs a 5-bit main-DAC and 5-bit sub-DAC, with unit capacitance of 200 fF. ADC unit cap was

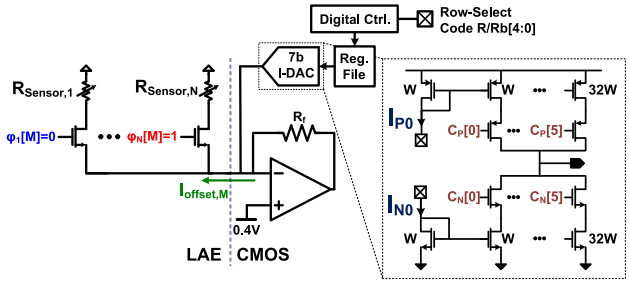


Fig. 14. Use of 7-bit I-DAC to cancel the offset current as a function of the row-select code.

chosen to minimize the INL by accounting for the foundry process spread in capacitance. The comparator is simply a clocked Strong-Arm latch.

3) Offset-Cancelling Current-DAC: For accurate sparse reconstruction, the ADC code should be zero except for the K-sparse sensors on which a force signal is explicitly present. In practice, readout and sensor-current offsets can cause non-zero codes, making an offset-cancelling current-DAC (I-DAC) necessary.

Three possible sources of offset in the system are considered, two related to non-idealities of the access-TFT characteristics, and a third related to the sensor characteristics. First, the access TFTs can have non-negligible gate-leakage currents. This can be especially problematic for a large sensor array, where the probability is increased that different numbers of access TFTs suffer from gate leakage, leading to significant offset current at the TIA input superimposed on the sensor currents. Note that, in this case, the offset current depends on the gate biases applied to the access TFTs, which are set by the row-select code. As a result, offset cancellation must be adjusted with the row-select code. Second, the access TFTs can have significant sub-threshold leakage current. Even when the access TFT is turned off by the matrix TFT logic for a particular row-select code, it has sub-Vt current through it. Though the TFT sub-threshold currents are generally small compared to their on-currents, this is once again problematic for a large sensor array due to the aggregate leakage arising from all the access TFTs, again leading to significant offset current. As with gate leakage, this source of offset depends on the gate biases applied to the access TFTs, which are set by the row-select code. Thus, offset cancellation must once again be adjusted with the row-select code. Third, the sensors, especially with the significant variations they exhibit, can have finite resistance with small or no force applied. Again, even with large resistances, the resulting offset current can be significant for a large sensor array. Once again, the offset current at the TIA input is a function of the access TFT states and thus the row-select code.

With all sources of offset thus requiring adjustment with the row-select code, the offset-canceling I-DAC is employed together with a calibration phase. During calibration, it is assumed that no force is applied to the sensors. Then, the row-select code is cycled to determine an I-DAC code that yields a zero-valued ADC output. As shown in Fig. 14, the corresponding I-DAC

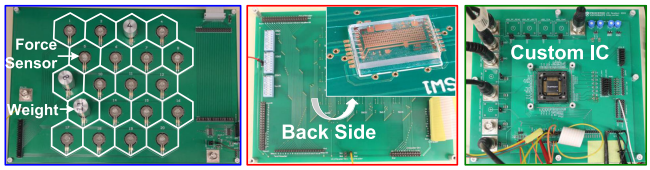


Fig. 15. System prototype implemented as three broads: (a) force-sensor array board. (b) TFT compression board, where LAE dice are wire-bonded to row-select signals. (c) Readout and control board, with custom CMOS IC.

code is then stored in an on-chip look-up table (register file). The overall bipolar I-DAC is 7 bits. It is composed of NMOS and PMOS current DACs which are each 6 bits. During sensor readout, the I-DAC code is fed from the register file for each row-select code.

D. Reconstruction Algorithm

For sparse reconstruction, the Sparsity Adaptive Matching Pursuit (SAMP) algorithm [42] is used. SAMP is a greedy algorithm, and thus has low complexity ($\mathcal{O}(MNK)$) compared with Basis Pursuit (BP), Basis Pursuit Denoising (BPDN), etc. [43] ($\mathcal{O}(M^2N^3)$). This makes it suitable for embedded sensing applications. At the same time, compared to other greedy approaches, such as Stochastic Gradient Pursuit (SGP) [44], Orthogonal Matching Pursuit (OMP) [45], Compressive Sensing Sampling Matching Pursuit (CoSaMP) [46], Subspace Pursuit (SP) [47], and Iterative Hard Thresholding (IHT) [48], SAMP has the benefit of theoretical guarantee on reconstruction accuracy.

The SAMP algorithm also has a number of practical benefits for tactile-sensing applications. First, it does not depend on tuning the step-size variables or the prior knowledge about the signal's distribution model in order to achieve high RSNR. Moreover, unlike CoSaMP and SP, which require knowing the precise sparsity K, SAMP needs only the maximum sparsity, not the precise sparsity, which is generally unknown in the tactile-sensing applications envisioned.

IV. System Prototype

To ease testing and characterization, the system prototype is implemented via three PCBs, as shown in Fig. 15. First, the force-sensor board has 20 force sensors placed at the center of each hexagon. Second, the sensor signals are connected to the TFT-compression board, which comprises wire-bonded LAE dice. Metal traces on this board distribute and appropriately connect the row-select control bits, so that each LAE die follows a unique switching pattern (i.e., a column of Φ). Next, the single output current signal from the TFT compression board is provided to a CMOS-IC board. Finally, the sparse-reconstruction algorithm is run on a PC to recover the sensor signals. As noted earlier, in an ultimate product, sensors and TFTs would be integrated into a single large-area substrate, onto which the CMOS IC might be locally bonded.

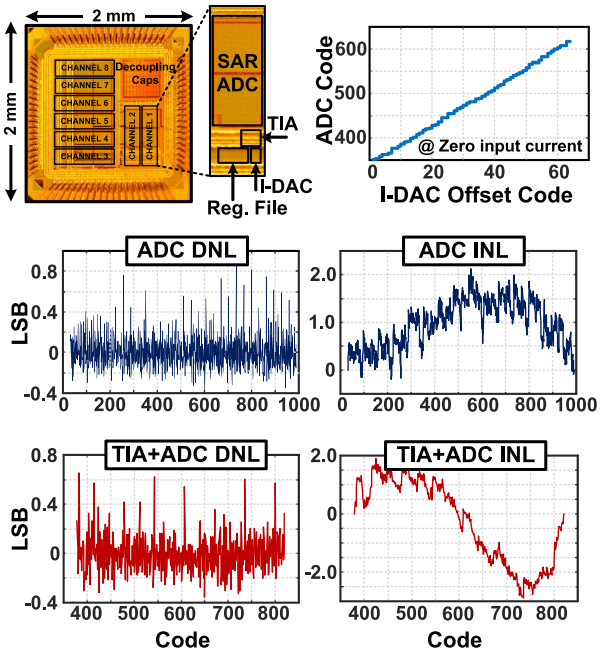


Fig. 16. CMOS die photograph and linearity measurements.

A. CMOS IC

Fig. 16 shows measurement results for a single channel of the CMOS readout IC, fabricated using GF 130 nm process. The SAR ADC operates at a full-scale voltage of 1.2 V. The ADC linearity is tested using the histogram method. A linear ramp input is applied and the resulting code distribution is used to characterize the DNL and INL. The ADC has a maximum DNL and INL of 0.85 and 2.0 LSB, respectively. The end-to-end linearity of a single channel is tested by applying a current ramp input to the TIA with the I-DAC disabled. The ADC output-code density yields maximum end-to-end channel DNL and INL of 0.65 and 2.0 LSBs respectively. The ADC SNDR is observed to be linear with the input voltage, reaching a maximum of 54 dB. The I-DAC linearity is tested by cycling through the I-DAC codes and performing readout with no input current applied. The linearity is measured from the I-DAC code, through the TIA and ADC. The maximum non-linearity is then measured as the DNL relative to the 6b I-DAC LSB. The maximum DNL for the I-DAC is measured to be 1.1 LSBs. Note that I-DAC linearity is not critical to system performance. What is important is adequate I-DAC resolution to compensate for the offset current at the TIA input, required to ensure the sparsity assumption.

B. LAE Die

LAE die consists of an access TFT, 160 matrix TFTs, and also yield-monitoring test structures, as shown in Fig. 17(a). The die are fabricated in-house on a glass substrate to ease system assembly and wire-bonding, but the processing employed is at 200 °C and fully flex compatible. 50 nm Cr is deposited and patterned as gate metal, then Al_2O_3(40 nm)/ZnO(10 nm)/Al_2O_3(35 nm)

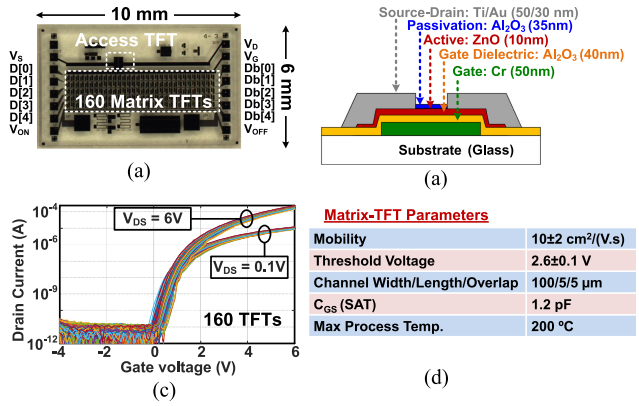


Fig. 17. Details of the LAE prototyping, including: (a) LAE die photograph; (b) TFT material stack (final metal interconnect is not shown); (c) I-V curves for 160 matrix-TFTs from one die; and (d) extracted matrix-TFT parameters.

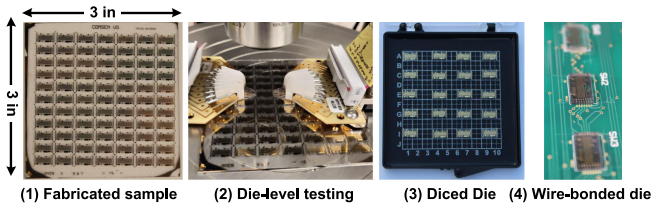


Fig. 18. Integration and testing steps of LAE die.

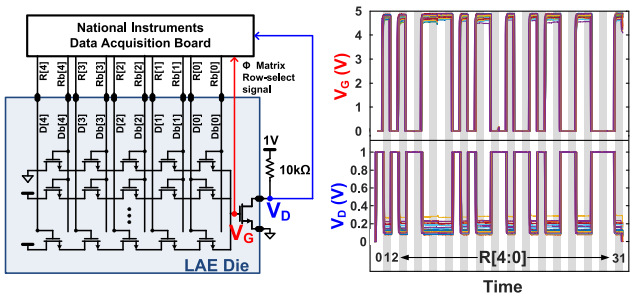


Fig. 19. LAE die test setup as well as V_G and V_D measurement results from 32 dice on a single sample, all of which show desired switching behaviour.

is deposited with plasma-enhanced atomic-layer deposition (PEALD) as gate dielectric, channel and passivation layer respectively, followed by deposition and patterning of Ti(50 nm)/Au(30 nm) as S/D, and then Cr(50 nm)/Au(100 nm) as final metal interconnect [30], [32]. Fig. 17(b). The I-V characteristics of the 160 matrix-TFTs from a single die are shown [Fig. 17(c)], exhibiting good uniformity and having the extracted TFT parameters given [Fig. 17(d)].

In order to integrate LAE dice for the system demonstration, the following procedure is pursued, shown in Fig. 18. First, TFT circuits are fabricated on 3" by 3" square glass, giving 77 dice. All dice are then tested via direct probing using a multi-contact wedge to ensure process control. Next, the sample is diced and previously working dice are tested again. Finally, working dice are wire bonded to the bottom side of the compression board.

Fig. 19 shows the die-level test setup. The row-select signal is provided by a National Instruments Data Acquisition Board (NI DAQ). The drain of the access TFT is connected to a 1 V supply through a 10 kΩ resistor, to emulate a force sensor. The first row-select code turns on the first branch of TFTs, and connects the access-TFT gate to ground. This turns the access TFT off, pulling up the drain voltage to 1 V. The second row-select code turns on the second branch, this time connecting the access TFT gate to 5 V. This turns the access TFT on, pulling the drain voltage near ground, set by the finite on-resistance of the access TFT and the sensor resistance. Fig. 19 plots 32 LAE dice tested from one sample for all 32 row-select codes, with the dice following the intended switching pattern.

C. TFT Yield Analysis and Enhancement

While compressed sensing enhances the system metrics associated with LAE-CMOS interfacing in hybrid systems, it requires a large number of TFTs (161 TFTs per sensor in this system), making TFT yield a concern. In addition to fault-tolerance analysis (Fig. 10), fabrication methods are employed, especially to mitigate problematic gate-short faults, which would affect the global row-select control signal. To characterize the intrinsic TFT-limited yield for the LAE die, on-die test structures for yield monitoring are employed. Most importantly, a MOS capacitor (stack under test is 40 nm Al_2O_3/10 nm ZnO), with width of 2220 μm and length of 440 μm is included, having equivalent gate-dielectric area of 550 matrix TFTs. The yield rate (no short) of this structure is measured to be 53% across 43 die, suggesting even greater gate-stack yield-rate for TFTs. The adequate yield achieved is attributed to PEALD deposition, which results in conformal and continuous deposition with low probability of pinholes through the deposited layers [49]. In addition to the MOS-capacitor test structure, a MOS transmission-line test structure and isolated TFTs are included. These confirmed adequacy and uniformity of saturation mobility, saturation threshold voltage, on/off ratio ($\sim 10^7$), and contact resistance, while enabling controlled extraction of TFT parameters and characterization of antenna effects due to interconnects.

Following the yield analysis, as described in [50], TFT yield and die yield were mainly limited by plasma damage and dicing electrostatic discharge because of the insulating substrate, plasma processing, and long metal traces. The yield was enhanced by preventing gate dielectric breakdown, via a gate isolation method (isolating TFT-gates from the common long gate lines for control signals) as well as temporary "shorting bars". With the gate isolation, the die yield during fabrication for representative samples increased from 2/98 to 40/77, while showing improved uniformity of the transistors performance.

D. System-Level Measurements

The complete system-level reconstruction-performance tests are conducted by placing three different weights on the sensor array at different positions, and repeating this for multiple times with the weights at different positions each time. Applying weights lowers the sensor resistance from high resistance (>100 MΩ) to a range between 20–100 kΩ, as illustrated in Fig. 20. In addition to system acquisition and reconstruction, the sensor resistances are measured directly using the NI DAQ.

TABLE I
SYSTEM PERFORMANCE SUMMARY

LAE (ZnO)		Custom IC (GF 130 nm)				Full-System (K=3)	
No. Sensors	20	Area	4 mm^2	ADC Resolution	10 b	No. Cycles per frame	32
Process Temp.	<200°C	No. Channels	8	ADC ENOB	8.7 b @50 kHz	Sensor R Range	100k-20kΩ
TFTs per Sensor	161	V_{DD}	1.2 V	TIA+ADC DNL/INL	0.65/2.0 LSB	Reconstruction Error	0.7 $k\Omega_{RMS}$
Matrix TFT Speed	1 kHz	I-DAC Res	7 b	ADC Energy	212 pJ/conv.	Frame Rate	31 fps
LAE E/frame	1.28 μJ	TIA Power/Ch	37 μW	CMOS E/frame	1.18 μJ	E/frame	2.46 μJ

TABLE II
COMPARISON TO THE STATE OF THE ART

Architecture	This Work Compressed Sensing	Sequential Scanner [51]	Passive Matrix [52]	Passive Matrix [6]	Active Matrix [53]	Active Matrix [54]
No. Sensors	20	10	8464	548	400	100
No. Cycles per frame	32	10	8464	548	20	10
No. LAE/CMOS Data Lines	1	1	92	32	20	10
Cycle Speed	1 kHz	500 Hz	100 Hz	4 kHz	15 Hz	-
Frame Rate	31 fps	50 fps	0.01 fps	7.3 fps	0.75 fps	-
LAE Energy per cycle	40 nJ/cycle	286 nJ/cycle	-	-	-	-
CMOS Energy per cycle	37 nJ/cycle	148 nJ/cycle	-	-	-	-
Total Energy per cycle (per frame)	77 nJ/cycle (2.46 μJ/frame)	434 nJ/cycle (4.34 μJ/frame)	-	-	-	-
Addressing Technology	ZnO TFTs	a-Si TFTs	-	-	SWCNT TFTs	Organic TFT
Readout Technology	130 nm CMOS	130 nm CMOS	-	-	-	-

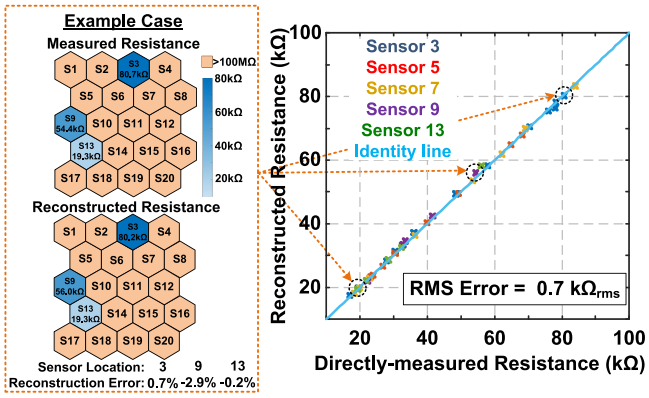


Fig. 20. Complete system reconstruction results, showing a strong correlation between measured and expected sensor data. Points are acquired with three different weights placed at different (random) sensor locations.

Finally, the system-acquired sensor data is reconstructed on a PC and corrected for the nominal access-TFT on resistance, of 1.5 kΩ.

As seen, the resistance directly measured from the sensors is well reconstructed by the system, with errors less than 3% across the three weights for the placement shown. Repeating the measurement with different weights and placements, always with a sparsity of $K = 3$, the high correlation between directly-measured and reconstructed resistance values is observed, giving an RMS error of 0.7 $k\Omega_{RMS}$ over the 13 placements measured. Given the large signals expected in tactile-sensing applications (due to proximity of sensors with embedded signals), such error is expected to address a broad range of applications. Table I reports the overall system performance summary, where the total readout frame rate (i.e., requiring 32 readout cycles) is 31 frames per second (fps). Each frame consumes 1.28 μJ in LAE domain and 1.18 μJ in CMOS, for a total of 2.46 μJ/frame, or 123 nJ/sensor. We noted in Section III-B, that our design could support up to 120 sensors. With 120 sensors, we expect the LAE power to scale by a factor of $120/20 = 6$, but the CMOS power to remain approximately constant. Thus with 120 sensors the frame energy would be 8.86 μJ and the energy per sensor would be 74 nJ.

Table II compares this work with the other recent state of the art tactile sensing systems. [51] is a scan chain architecture, in which a digital circuit at each sensor enables one sensor at a time to be read out through a single LAE-to-CMOS data interface, by turning on an access TFT attached to each sensor. Due to lower energy per cycle in both the LAE and CMOS domains, the compressed sensing approach of this paper consumes ~2× less energy per frame for twice as many sensors. The scan chain is operating at its maximum cycle speed, thus additional sensors would reduce its frame rate and increase energy consumption per frame. [52] and [6] describe passive matrices, in which only one sensor (one row and one column) can be read out at a time (cycle time). Cycle speeds are within a factor of 10 slower to 4 faster than our work, but unfortunately no power data is available. [53] and [54] use active matrix architectures. [53] has a low cycle speed due to the slow response time of the sensor used in the study. No power data for [53] and [54] is available.

V. CONCLUSION

This paper presents an interface-reduction architecture for LAE-CMOS hybrid systems, which exploits the attribute of sparsity exhibited in many tactile-sensing applications. Specifically, compressed sensing is employed to enable efficient interface reduction using simple TFT circuits, based on digital switches. With this, the system metrics associated with interfacing scale with the level of sparsity, rather than with the large number of total sensors as typically is required. The challenges include increased dynamic range for CMOS readout, though this is

readily tolerated given the higher energy efficiency and performance of transistors in the CMOS domain, and the need for a large number of TFTs, raising yield concerns. However, fault-tolerance analysis and yield monitoring show that high overall system yield is achievable.

The proposed architecture is demonstrated using a force-sensor array with 20 elements, ZnO-based TFT compressed-sensing circuits, as well as CMOS-based readout and control circuitry. The system is designed for a sparsity level of 3, it takes 32 measurements, uses a total of 11 interfaces, and can support scaling up to 120 sensors. The end-to-end sensor-data reconstruction error is 0.7 $k\Omega_{RMS}$, where activated sensor resistance values varied from 20-100 $k\Omega$.

REFERENCES

[1] J. Pickering, "Touch-sensitive screens: The technologies and their application," *Int. J. Man-Mach. Stud.*, vol. 25, no. 3, pp. 249–269, 1986.

[2] B. Glisic, Y. Yao, S. E. Tung, S. Wagner, J. C. Sturm, and N. Verma, "Strain sensing sheets for structural health monitoring based on large-area electronics and integrated circuits," *Proc. IEEE*, vol. 104, no. 8, pp. 1513–1528, Aug. 2016.

[3] L. E. Osborn *et al.*, "Prosthesis with neuromorphic multilayered e-dermis perceives touch and pain," *Sci. Robot.*, vol. 3, no. 19, p. eaat3818, 2018.

[4] A. Schmitz, P. Maiolino, M. Maggiali, L. Natale, G. Cannata, and G. Metta, "Methods and technologies for the implementation of large-scale robot tactile sensors," *IEEE Trans. Robot.*, vol. 27, no. 3, pp. 389–400, Jun. 2011.

[5] J. Byun *et al.*, "Electronic skins for soft, compact, reversible assembly of wirelessly activated fully soft robots," *Sci. Robot.*, vol. 3, no. 18, p. eaas9020, May 2018. [Online]. Available: http://robotics.sciencemag.org/content/3/18/eaas9020

[6] S. Sundaram, P. Kellnhofer, Y. Li, J.-Y. Zhu, A. Torralba, and W. Matusik, "Learning the signatures of the human grasp using a scalable tactile glove," *Nature*, vol. 569, no. 7758, p. 698, 2019.

[7] T. Someya and M. Amagai, "Toward a new generation of smart skins," *Nature Biotechnology*, vol. 37, no. 4, p. 382, 2019.

[8] V. Abraira and D. Ginty, "The sensory neurons of touch," *Neuron*, vol. 79, no. 4, pp. 618–639, 2013. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0896627313007101

[9] D. Farina *et al.*, "Man/machine interface based on the discharge timings of spinal motor neurons after targeted muscle reinnervation," *Nature Biomed. Eng.*, vol. 1, no. 2, p. 0025, 2017.

[10] K. Englehart and B. Hudgins, "A robust, real-time control scheme for multifunction myoelectric control," *IEEE Trans. Biomed. Eng.*, vol. 50, no. 7, pp. 848–854, Jul. 2003.

[11] C. E. Bouton *et al.*, "Restoring cortical control of functional movement in a human with quadriplegia," *Nature*, vol. 533, no. 7602, p. 247, 2016.

[12] L. R. Hochberg *et al.*, "Reach and grasp by people with tetraplegia using a neurally controlled robotic arm," *Nature*, vol. 485, no. 7398, p. 372, 2012.

[13] R. Kwok, "Neuroprosthetics: Once more, with feeling," *Nature News*, vol. 497, no. 7448, p. 176, 2013.

[14] E. Mastinu *et al.*, "Grip control and motor coordination with implanted and surface electrodes while grasping with an osseointegrated prosthetic hand," *J. Neuroengineering Rehabil.*, vol. 16, no. 1, p. 49, 2019.

[15] E. J. Earley, R. E. Johnson, L. J. Hargrove, and J. W. Sensinger, "Joint speed discrimination and augmentation for prosthesis feedback," *Scientific Rep.*, vol. 8, no. 1, 2018, Art. no. 17752.

[16] D. J. Tyler, "Neural interfaces for somatosensory feedback: Bringing life to a prosthesis," *Current Opinion Neurology*, vol. 28, no. 6, p. 574, 2015.

[17] B. Hollis, S. Patterson, and J. Trinkle, "Compressed learning for tactile object recognition," *IEEE Robot. Autom. Lett.*, vol. 3, no. 3, pp. 1616–1623, Jul. 2018.

[18] I. Hendy, "Gen-10 fabs will create upheaval in the display market," *Inform. Display*, vol. 34, no. 3, pp. 18–58, 2018. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/j.2637-496X.2018.tb01084.x

[19] E. Montbach and D. Davis, *Roll-to-Roll Manufacturing of Flexible Displays*. John Wiley & Sons, Ltd., 2018, ch. 10, pp. 285–323. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119163824.ch10

[20] T. Moy *et al.*, "Thin-film circuits for scalable interfacing between large-area electronics and CMOS ICs," in *Proc. 72nd Device Res. Conf.*, Jun. 2014, pp. 271–272.

[21] W. Gao *et al.*, "Fully integrated wearable sensor arrays for multiplexed in situ perspiration analysis," *Nature*, vol. 529, no. 7587, pp. 509–514, Jan. 2016. [Online]. Available: http://www.nature.com/articles/nature16521

[22] D.-H. Kim *et al.*, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, 2011. [Online]. Available: https://science.sciencemag.org/content/333/6044/838

[23] M. Kaltenbrunner *et al.*, "An ultra-lightweight design for imperceptible plastic electronics," *Nature*, vol. 499, no. 7459, pp. 458–463, Jul. 2013. [Online]. Available: http://www.nature.com/articles/nature12314

[24] H. Akkerman *et al.*, "393: Printed organic photodetector arrays and their use in palmprint scanners," *SID Symp. Dig. Tech. Papers*, vol. 49, no. 1, pp. 494–497, May 2018. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/sdtp.12609

[25] T. Moy *et al.*, "An EEG acquisition and biomarker-extraction system using low-noise-amplifier and compressive-sensing circuits based on flexible, thin-film electronics," *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 309–321, Jan. 2017.

[26] C. Garripoli, J. P. J. V. D. Steen, E. Smits, G. H. Gelinck, A. H. M. V. Roermund, and E. Cantatore, "15.3 An a-IGZO asynchronous delta-sigma modulator on foil achieving up to 43 dB SNR and 40 dB SNDR in 300 Hz bandwidth," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2017, pp. 260–261.

[27] K. Myny, E. V. Veenendaal, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "An 8-bit, 40-instructions-per-second organic microprocessor on plastic foil," *IEEE J. Solid-State Circuits*, vol. 47, no. 1, pp. 284–291, Jan. 2012.

[28] F. D. Roose *et al.*, "A thin-film, a-IGZO, 128b SRAM and LPROM matrix with integrated periphery on flexible foil," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3095–3103, Nov. 2017.

[29] K. Myny *et al.*, "15.2 A flexible ISO14443-A compliant 7.5 mW 128b metal-oxide NFC barcode tag with direct clock division circuit from 13.56 MHz carrier," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2017, pp. 258–259.

[30] Y. Afsar *et al.*, "18-2: Oxide TFT LC oscillators on glass and plastic for wireless functions in large-area flexible electronic systems," *SID Symp. Dig. Tech. Papers*, vol. 47, no. 1, pp. 207–210, 2016. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/sdtp.10638

[31] T. Zaki *et al.*, "S-parameter characterization of submicrometer low-voltage organic thin-film transistors," *IEEE Electron Device Lett.*, vol. 34, no. 4, pp. 520–522, Apr. 2013.

[32] Y. Mehlman, P. Kumar, M. Ozatay, S. Wagner, J. C. Sturm, and N. Verma, "Large-area electronics HF RFID reader array for object-detecting smart surfaces," *IEEE Solid-State Circuits Lett.*, vol. 1, no. 8, pp. 182–185, Aug. 2018.

[33] N. Mnzenrieder *et al.*, "Flexible a-IGZO TFT amplifier fabricated on a free standing polyimide foil operating at 1.2 MHz while bent to a radius of 5 mm," in *Proc. Int. Electron Devices Meeting*, Dec. 2012, pp. 5.2.1–5.2.4.

[34] M. Kitamura and Y. Arakawa, "High current-gain cutoff frequencies above 10 MHz in n-channel c60 and p-channel pentacene thin-film transistors," *Japanese J. Appl. Phys.*, vol. 50, no. 1S2, p. 01BC01, 2011.

[35] N. Verma *et al.*, "Enabling scalable hybrid systems: Architectures for exploiting large-area electronics in applications," *Proc. IEEE*, vol. 103, no. 4, pp. 690–712, Apr. 2015.

[36] W. d. Boer, "Operating principles of active matrix LCDs," in *Active Matrix Liquid Crystal Displays*, Burlington, VT, USA: Newnes, 2005, ch. 2, pp. 23–48.

[37] L. E. Aygun *et al.*, "Hybrid system for efficient LAE-CMOS interfacing in large-scale tactile-sensing skins via TFT-based compressed sensing," in *Proc. IEEE Int. Solid-State Circuits Conf.*, San Francisco, CA, USA, 2019, pp. 280–282.

[38] Y. Afsar, T. Moy, N. Brady, S. Wagner, J. C. Sturm, and N. Verma, "An architecture for large-area sensor acquisition using frequency-hopping ZnO TFT DCOs," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 297–308, Jan. 2018.

[39] D. L. Donoho, "Compressed sensing," *IEEE Trans. Inform. Theory*, vol. 52, pp. 1289–1306, 2006.

[40] InterlinkElectronics, "FSR 402 Short." [Online]. Available: https://www.interlinkelectronics.com/fsr-402-short

[41] U. Ozgur *et al.*, "A comprehensive review of ZnO materials and devices," *J. Appl. Phys.*, vol. 98, no. 4, 2005, Art. no. 041301.

[42] T. T. Do, L. Gan, N. Nguyen, and T. D. Tran, "Sparsity adaptive matching pursuit algorithm for practical compressed sensing," in *Proc. 42nd Asilomar Conf. Signals, Syst. Comput.*, Oct. 2008, pp. 581–587.
[43] S. Chen, D. Donoho, and M. Saunders, "Atomic decomposition by basis pursuit," *SIAM J. Scientific Comput.*, vol. 20, no. 1, pp. 33–61, 1998, doi: 10.1137/S1064827596304010.
[44] Y. Lin, Y. Chen, N. Huang, and A. Wu, "Low-complexity stochastic gradient pursuit algorithm and architecture for robust compressive sensing reconstruction," *IEEE Trans. Signal Process.*, vol. 65, no. 3, pp. 638–650, Feb. 2017.
[45] J. A. Tropp and A. C. Gilbert, "Signal recovery from random measurements via orthogonal matching pursuit," *IEEE Trans. Inform. Theory*, vol. 53, no. 12, pp. 4655–4666, Dec. 2007.
[46] D. Needell and J. Tropp, "CoSaMP: Iterative signal recovery from incomplete and inaccurate samples," *Appl. Comput. Harmon. Anal.*, vol. 26, no. 3, pp. 301–321, 2009. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1063520308000638
[47] W. Dai and O. Milenkovic, "Subspace pursuit for compressive sensing signal reconstruction," *IEEE Trans. Inform. Theory*, vol. 55, no. 5, pp. 2230–2249, May 2009.
[48] T. Blumensath and M. E. Davies, "Iterative hard thresholding for compressed sensing," *Appl. Comput. Harmon. Anal.*, vol. 27, no. 3, pp. 265–274, Nov. 2009. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1063520309000384
[49] D. A. Mourey, D. A. Zhao, and T. N. Jackson, "ZnO thin film transistors and circuits on glass and polyimide by low-temperature PEALD," in *Proc. IEEE Int. Electron Devices Meeting*, 2009, pp. 1–4.
[50] Z. Zheng, L. E. Aygun, S. Wagner, N. Verma, and J. C. Sturm, "Analyzing and increasing yield of ZnO thin-film transistors for large-area sensing systems by preventing process-induced gate dielectric breakdown," in *Proc. 77th Device Res. Conf.*, Jun. 2019.
[51] Y. Hu *et al.*, "A self-powered system for large-scale strain sensing by combining CMOS ICS with large-area electronics," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 838–850, Apr. 2014.
[52] W. Wu, X. Wen, and Z. L. Wang, "Taxel-addressable matrix of vertical-nanowire piezotronic transistors for active and adaptive tactile imaging," *Science*, vol. 340, no. 6135, pp. 952–957, 2013.
[53] C. Yeom, K. Chen, D. Kiriya, Z. Yu, G. Cho, and A. Javey, "Large-area compliant tactile sensors using printed carbon nanotube active-matrix backplanes," *Adv. Mater.*, vol. 27, no. 9, pp. 1561–1566, 2015.
[54] S. Wang *et al.*, "Skin electronics from scalable fabrication of an intrinsically stretchable transistor array," *Nature*, vol. 555, no. 7694, p. 83, 2018.

Levent E. Aygun received the B.Sc. and M.Sc. degrees in electrical and electronics engineering, from the Bilkent University, Ankara, Turkey, in 2011 and 2013, respectively, and the M.A. degree in electrical engineering from the Princeton University, Princeton, NJ, USA, in 2015, where he is currently working toward the Ph.D. degree.

His research interests include flexible sensor and circuit design, integration of thin-film, and CMOS VLSI domains to build large-scale sensor systems.

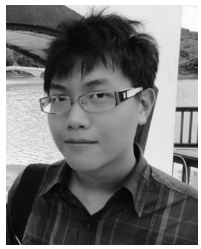
Prakhar Kumar received the B.E.(Hons) in electrical and electronics engineering from the Birla Institute of Technology and Science Pilani, Pilani Campus, India, in 2016.

His current research interests include developing hybrid sensing systems by bringing together large area electronics (LAE) and CMOS VLSI technologies. More specifically, he is interested in designing technology platforms that can enable machine learning algorithms to carry out inference and state estimation tasks effectively.

Zhiwu Zheng (S'19) received the B.S. degree in physics from the Nanjing University, Nanjing, China, in 2016, and the M.A. degree in electrical engineering from Princeton University, Princeton, NJ, USA, in 2019. He is currently working toward the Ph.D. degree in electrical engineering at Princeton University.

During his undergraduate study, he worked on nanoelectronic, photonic, and quantum devices for next-generation electrically controlled photonic computation systems. He was an Exchange Student working on 2-D-material electronic devices with the National University of Singapore, Singapore, during the Spring semester of 2015. His current research interests include machine learning and statistical signal processing algorithms, architectures, circuits, and devices for advanced sensing systems and robotics.

Mr. Zheng was the recipient of 2018–2019 and 2019–2020 Fellowships of the Program in plasma science and technology (PPST) at Princeton University, 2014 Shi Shi-Yuan Scholarship, 2014 Infineon Scholarship, 2013–2016 Fellowship of China National Innovational Undergraduates Program, Nanjing University 2013 Excellent Student, 2013 Scientific Innovation Scholarship, and 2013–2014, 2014–2015, 2015–2016 First-Place Talent Scholar Awards.



Ting-Sheng Chen received the B.S. degree in electrical engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 2014, and the Ph.D. degree from the Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, in 2018.

In 2018, he was a Research Assistant with the Department of Electrical Engineering, Princeton University, Princeton, NJ, USA. He is currently a Senior Engineer with MediaTek, Inc., Hsinchu, Taiwan, and worked on algorithm and architecture design for 5G wireless transceiver. His research interests include the areas of VLSI implementation of DSP algorithms and compressive sensing.

Dr. Chen was the recipient of VLSI-DAT Best Paper Award in 2017, Students Travel Grants of 2018 IEEE ICASSP, 2018 Macronix Golden Silicon Awards, 2018 CIC Outstanding Chip Design Award, and 2018 Taiwan Semiconductor Industry Association (TSIA) Award for doctoral graduate students.

Sigurd Wagner (Life Fellow) received the Ph.D. degree in physical chemistry from the University of Vienna, Austria, in 1968.

He was a Postdoctoral Fellow with The Ohio State University, Columbus, OH, USA, and has worked with Bell Labs from 1970 to 1978, and was the Founding Chief of the Photovoltaic Research Branch at the Solar Energy Research Institute (now NREL) from 1978 to 1980. At Princeton, he has been developing concepts and applications of large-area electronics, and has been an advocate of laboratory-based learning. He is a Professor Emeritus of electrical engineering and Senior Scholar at Princeton University, where he has been working since 1980. In collaboration with colleagues and students, he has introduced fundamentally new materials, concepts, devices, and structures to thin-film electronics: the first heterojunction solar cell with a ternary compound semiconductor, $CuInSe_2$, and a quaternary compound, Cu_2CdSnS_4, among others; the Fermi-level dependence of the density of recombination center in hydrogenated amorphous silicon; microfluidic fundamentals of forming device patterns by printing, and the design and fabrication of microfluidic devices; foundational experiments on flexible, rollable, elastically stretchable, and conformably shaped electronic surfaces, and their basic design rules and architecture. At present, he is working on the demonstration of complete large-area hybrid thin-film/CMOS-circuit systems for sensing applications with James C. Sturm and Naveen Verma.

Dr. Wagner is a Life Fellow of the IEEE, a Fellow of the American Physical Society, and a Corresponding Member of the Austrian Academy of Sciences. He was an Alexander von Humboldt Foundation Senior Fellow, received the 2009 Nevill Mott Prize, the 2014 ITC 10th Anniversary Prize, and the 2017 MRS David Turnbull Lectureship. A plaque in Princetons Electrical Engineering Undergraduate Laboratory honors his engagement in lab education.

James C. Sturm (S'81–M'85–SM'95–F'01) was born in Berkeley Heights, NJ, USA, in 1957. He received the B.S.E. degree in electrical engineering and engineering physics from the Princeton University, Princeton, NJ, USA, in 1979, and the M.S.E.E. and Ph.D. degrees in 1981 and 1985, respectively, both from the Stanford University, Stanford, CA, USA.

In 1979, he joined the Intel Corporation, Santa Clara, CA, USA, as a Microprocessor Design Engineer, and in 1981, he was a Visiting Engineer with the Siemens, Munich, Germany. In 1986, he joined the Faculty of Princeton University, where he is currently the Stephen R. Forrest Professor in electrical engineering. From 2003 to 2015, he was the Founding Director of the Princeton Institute for the Science and Technology of Materials (PRISM), and from 1994 to 1995, he was a von Humboldt Fellow with the Institut fuer Halbleitertechnik, University of Stuttgart, Stuttgart, Germany. He has worked in the fields of silicon-based heterojunctions, thin-film and flexible electronics, photovoltaics, the nano-bio interface, SOI, and three-dimensional (3-D) integration.

Dr. Sturm was a National Science Foundation Presidential Young Investigator. He has won over ten awards for teaching excellence. In 1996 and 1997, he was the Technical Program Chair and General Chair of the Device Research Conference, respectively. He served on the organizing committee of IEDM (1988–1992 and 1998–1999), having chaired both the solid-state device and detectors/sensors/displays committees. He has served on the boards of directors of the Materials Research Society and the Device Research Conference, and was a Co-Founder of Aegis Lightwave.

Naveen Verma received the B.A.Sc. degree in electrical and computer engineering from The University of British Columbia Vancouver, Canada, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, U.S., in 2005 and 2009, respectively.

Since July 2009, he has been working as a Professor of electrical engineering with Princeton University. His research interests include advanced sensing systems, exploring how systems for learning, inference, and action planning can be enhanced by algorithms that exploit new sensing and computing technologies. This includes research on large-area, flexible sensors, energy-efficient statistical-computing architectures and circuits, and machine-learning and statistical-signal-processing algorithms.

Dr. Verma has served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and currently serves on the technical program committees for ISSCC, VLSI Symposium, DATE, and IEEE Signal-Processing Society (DISPS). He is recipient or co-recipient of the 2006 DAC/ISSCC Student Design Contest Award, 2008 ISSCC Jack Kilby Paper Award, 2012 Alfred Rheinstein Junior Faculty Award, 2013 NSF CAREER Award, 2013 Intel Early Career Award, 2013 Walter C. Johnson Prize for Teaching Excellence, 2013 VLSI Symp. Best Student Paper Award, 2014 AFOSR Young Investigator Award, 2015 Princeton Engineering Council Excellence in Teaching Award, and 2015 Best Paper Award by IEEE TRANSACTIONS ON COMPONENTS, PACKAGING AND MANUFACTURING TECHNOLOGY Best Paper Award.