Gigahertz Zinc-Oxide TFT-Based Oscillators

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Introduction

A number of papers have been published over the past few years demonstrating metal-oxide thin-film-transistors (TFTs) with f_T and/or f_{MAX} over 1GHz [1-4]. However, these works have focused purely on device-level characterization and have not demonstrated gigahertz circuit operation. In this work, we demonstrate a large-area-compatible metal-oxide TFT-based cross-coupled LC oscillator operating at 1.25GHz, processed at flex-compatible temperatures (<200ºC). Achieving this required co-optimization of TFT and inductor dimensions/layouts, balancing device performance with parasitics (resistances, capacitances).

Device Optimization

Fig. 1 shows the ZnO-TFT technology used in this work, made by PEALD. The high mobility (15cm^2/V·s) enables sufficient performance for GHz operation when device geometries are properly scaled/sized. For cross-coupled LC oscillators, the frequency is limited by the unity-power-gain frequency (f_{MAX}), rather than the unity-current-gain frequency (f_T). f_{MAX} can typically be 2-4x higher than f_T for TFTs, since it is easier to make high-quality passives rather than high-mobility materials under a strict thermal budget. This gives f_{MAX}-limited circuits greater potential for high-frequency operation. We optimize TFTs for high f_{MAX} in four ways. (1) Reduction of parasitic source/drain-to-gate overlap (X_{OV}) capacitance through a self-aligned process shown in Fig. 2, enabling submicron overlaps [3]. (2) Scaling of channel length to both lower capacitance and increase transconductance. We scale to ~1µm, below which reduction of the output resistance r_0 begins to lower f_{MAX}. (3) Reduction of gate resistance through use of a thick Al gate (110nm) sandwiched between Cr to prevent hillocks (Fig 1a), achieving a sheet resistance $R_{G,SH} = 0.4\Omega/sq$. (4) Scaling of TFT finger width to reduce gate resistance further. With all of these techniques combined, we achieve up to 2.7GHz f_{MAX} at V_{GS}=V_{DS}=6V (Fig. 2c).

Circuit and Passive Optimization

Fig. 3 shows the cross-coupled LC-oscillator circuit, including device and inductor parasitics. For analysis, the circuit can be modeled as two common-source amplifier stages connected in feedback, each comprising a small-signal RLC tank driven by an ideal transconductor. In resonance, the impedance from the tank inductance L_{TANK} and capacitance C_{TANK} exactly cancel such that the gain of each stage is $A_{SS} = -g_m R_{TANK}$ for a total open-loop gain of $(g_m R_{TANK})^2$. Due to the positive feedback, if the absolute gain of a single branch exceeds 1, the circuit oscillates at the resonant frequency, $f_{osc} = 1/(2\pi\sqrt{L_{TANK}C_{TANK}})$, as dictated by the Barkhausen oscillation criterion. The optimization of f_{osc} therefore entails minimizing $L_{TANK} \cdot C_{TANK}$ under the constraint $g_m R_{TANK} > 1$.

We consider in Fig. 4 the optimization of TFT width W and inductance L_{TANK} (through varying the radius of a planar loop inductor with a fixed number of turns) for maximizing gain at a fixed frequency. Increasing the radius of the inductor causes its inductance, parasitic series resistance, and parallel capacitance to increase approximately linearly in our regime of interest (confirmed by EM simulations). Increasing L_{TANK} therefore necessitates a super-linear decrease in C_{GS}/C_{GD}, and thus TFT W, given a frequency constraint (Fig. 4a). While this improves R_{TANK}, it also decreases transconductance g_m, such that the overall gain reaches a maximum and then decreases (Fig. 4b). At each frequency, we can find the (W, L_{TANK}) pair which give the highest gain (Fig 5a). Eventually, as frequency is scaled, the maximum gain drops below unity and the oscillation criterion is not met. We estimate our technology limit at 2.6GHz. Lastly, the number of TFT fingers are optimized in conjunction with the inductor (Fig. 5b). Breaking a TFT into multiple fingers reduces gate length, but also increases routing overlaps (see Fig. 6a). Thus, the number of fingers presents a tradeoff between increased C_{GS} and reduced gate resistance. We find the optimum is 8 fingers.

Experimental Results

We fabricate transistors on 3"x3" glass (process temp.<200ºC) with a fixed finger width W_f= 25µm (Fig 6a). For ease of testing, we dice our TFT sample and wire bond the TFT die to a PCB with planar single loop inductors (Fig. 6b). Inductor radii and TFT W are chosen focusing on a design with gain $|A_{SS}| > 1.5$. A summary of the results (Fig. 6c) shows 1.25GHz oscillations were achieved with an inductor radius of 4mm and TFT width of 100µm (4 fingers). The corresponding oscilloscope waveform, with 2.8V swing, and FFT are shown, demonstrating robust oscillations and good spectral purity. For further increase in frequency, we identify that improvements in TFT r_0 and inductor technology integrated on the large-area substrate would provide the largest benefit, with projections exceeding 10GHz.

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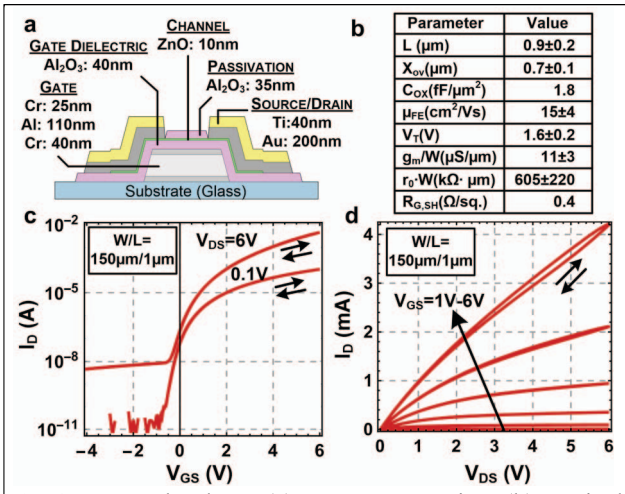

Fig. 1. TFT technology. (a) TFT cross section. (b) Typical TFT properties (shown for L=1μm and V_{GS}=5V). (c) Representative transfer curve and (d) output curve.

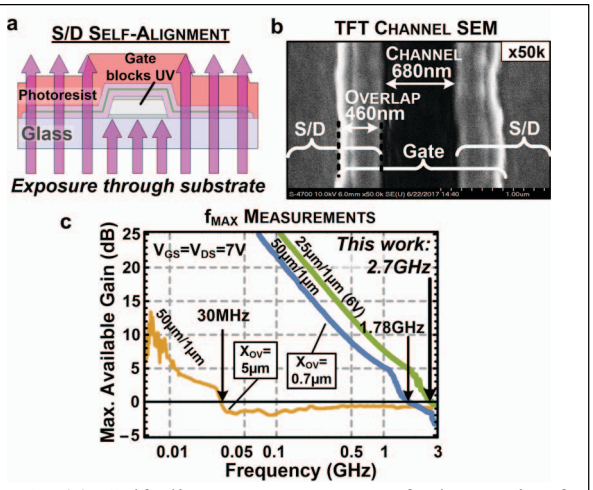

Fig. 2. (a) Self-alignment exposure of photoresist for defining S/D liftoff. (b) SEM of self-aligned TFT. (c) Measurement of power gain with f_{MAX} up to 2.7GHz.

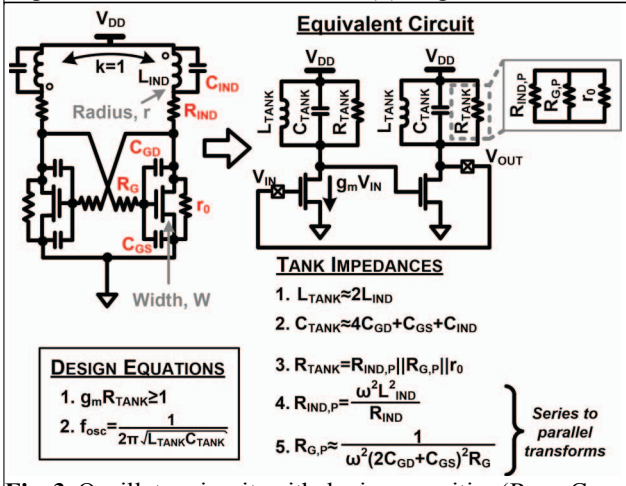

Fig. 3. Oscillator circuit, with device parasitics (R_{IND}, C_{IND}, r_0, R_G, C_{GD}, C_{GS}), and equivalent small-signal model. Tank impedances and design equations are shown.

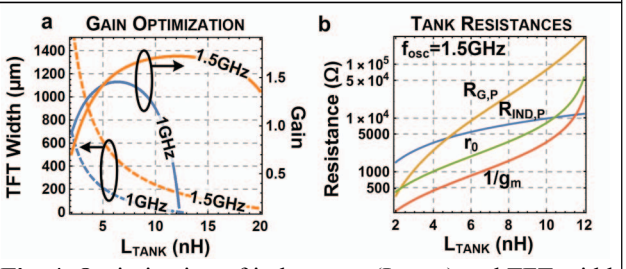

Fig. 4. Optimization of inductance (L_{TANK}) and TFT width (W) for maximum gain (shown for 6 fingers). (a) At a fixed frequency, as L_{TANK} is increased, W must be reduced to reduce C_{TANK}. The gain is calculated for each (W, L_{TANK}) pair, showing an absolute maximum as L_{TANK} increases. (b) The parallel tank resistances and $1/g_m$ are calculated for f_{osc}=1.5GHz at each L_{TANK} and corresponding W from part (a). While R_{TANK} increases with L_{TANK}, g_m decreases along with W. Since $R_{IND,P}$ scales more slowly, the gain reaches a peak.

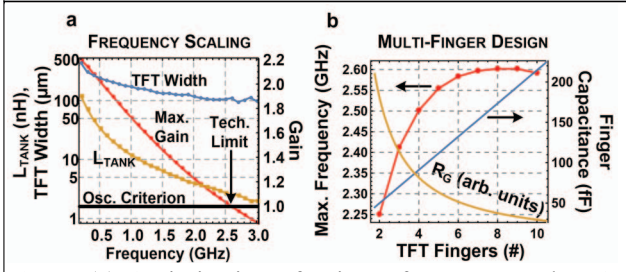

Fig. 5. (a) Optimization of gain as frequency scales. At each frequency, the W and L_{TANK} for achieving the maximum gain are shown [as per Fig. 4(a)]. As frequency increases, W and L_{TANK} must be made smaller and the maximum gain decreases. When the achievable gain drops below unity, the circuit cannot oscillate, thereby defining a technology limit (~2.6GHz). (b) Multi-finger TFT design optimization. Fingers reduce the gate resistance but at a capacitance penalty, affecting the technology limit. The optimum for gain=1 is 8 fingers.

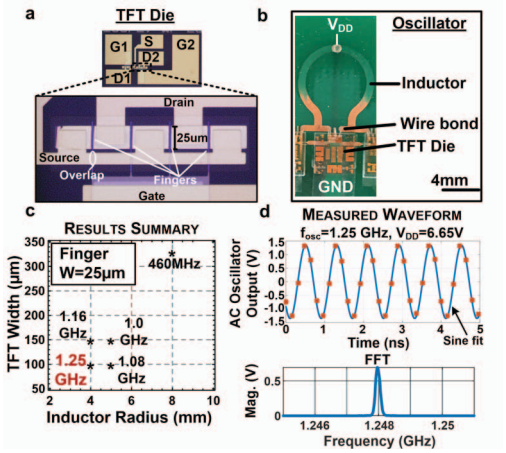

Fig. 6. Experimental results. a) TFT Die, b) inductor PCB for test, c) Summary of results for various radii and TFT width, and d) Waveform and associated FFT for 1.25GHz result (oscilloscope sampling frequency is 6GB/s).