

Design and Characterization of High Quality-Factor Inductors for Wireless Systems Compatible With Flexible Large-Area Electronics

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Abstract—Resonant operation, exploiting high quality-factor planar inductors, has recently enabled gigahertz (GHz) applications for large-area electronics (LAE), providing a new technology platform for large-scale and flexible wireless systems. This work first presents the design, analysis, and characterization methodology of flex-compatible large-area planar inductors. Specifically, three distinct radio frequency (RF) inductor characterization methods are experimentally demonstrated and compared, with the most accurate method among them (i.e., *S*-parameters in a two-port configuration) demonstrating a record-high quality factor of up to ~ 65 in the 2.4-GHz frequency band. Enabled by accurate characterization, key inductor design considerations regarding the resistive loss due to inductor’s metal traces are then discussed. Finally, a case study of the recently demonstrated LAE resonant switch shows the potential of these high-performance inductors towards large-area and conformal wireless systems for integrated Internet of Things (IoT) and 5G/6G applications.

Index Terms—5G/6G, flex compatible, Internet of Things (IoT), monolithic integration, planar inductor.

I. INTRODUCTION

LARGE-AREA electronics (LAE) is a broad class of technologies that employ low-temperature processing and monolithic integration of semiconductors, metals, and dielectrics over large and flexible substrates of polymers or glass, which can span the order of meters. The rich functionality offered by LAE makes it a promising technology platform for next-generation flexible systems [1], [2], [3]. However, due to compromised material properties from low-temperature processing and considerable parasitic components introduced by large-area photolithography, conventional LAE devices have typically been limited to low operation frequency, compared to devices from today’s mainstream electronics technologies (e.g., Si-CMOS and III-V). Recent materials and devices

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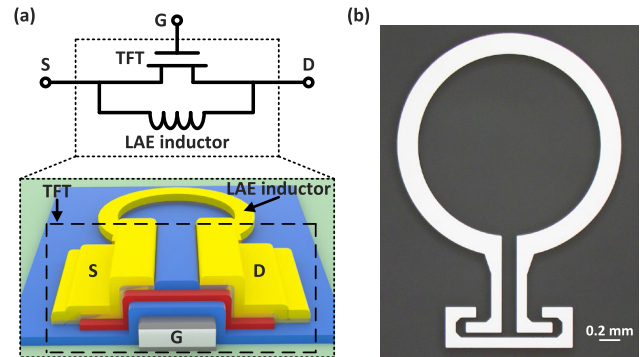


Fig. 1. (a) Schematic of a TFT in parallel with an LAE inductor, operated as a resonant switch in the GHz regime (adapted from [5]). (b) Die photo of an LAE-based flex-compatible on-chip planar inductor made of 2.5- μm -thick silver, with a radius of 1 mm and a trace width of 0.2 mm.

progress has realized gigahertz (GHz) LAE devices and thereby led to GHz LAE systems, enabling control over large and conformal radiative apertures for future wireless applications in the Internet of Things (IoT) and 5G/6G [4], [5], [6]. One key enabling approach for these breakthroughs has been the resonant operation of LAE devices utilizing large-area flex-compatible planar inductors. Such inductors can achieve high quality factors (Q -factors) by leveraging wide and thick metal traces, as well as low-loss substrates. Such resonant operation brings the operation frequency of LAE circuits/systems close to the LAE device limits in the GHz regime. Since this frequency regime is of particular interest for low-power and long-range wireless communication (e.g., the 2.4-GHz frequency band for Wi-Fi and Bluetooth), an in-depth understanding of the inductors is essential for system design and further improvement.

As an example, conventional LAE thin-film transistors (TFTs) typically operate up to hundreds of megahertz, mainly limited by low channel carrier mobility and large overlap capacitances between source/drain and gate. Such parasitic capacitance can be minimized by self-alignment, reducing overlap from ~ 5 to $\sim 0.5\mu\text{m}$ [7]. As shown in Fig. 1(a), the residual overlap capacitance can then be “resonated out” by an inductor in parallel with the TFT. The high Q -factor of the inductor enables a narrowband resonant switch with high OFF-state impedance in the 2.4-GHz band [5], [6]. Thus, process-compatible monolithic integration of such inductors

can enable highly functional and controllable metasurfaces based on arrays of such LAE resonant switches.

This work investigates planar inductors of 2.5- μm -thick, thermally evaporated silver on glass substrates with a maximum process temperature of $\sim 25^\circ\text{C}$ (room temperature) and 200°C , which are compatible with LAE fabrication on flexible substrates [8], [9]. With metal thicknesses beyond the skin depth at 2.4 GHz and the benefits of low-loss substrates, the measured Q -factor is up to ~ 65 in the 2.4-GHz band, which is at least three times that of prior state-of-art inductors (both flex-compatible and flex-incompatible) with similar geometry, in a similar frequency band [10], [11], [12], [13]. This is achieved without added design/fabrication complications for the inductor performance enhancement, thus facilitating integration in flexible electronics. For example, the use of patterned ground shields is avoided, which have been critical features widely used for inductors in Si-CMOS technology to suppress substrate losses, in order to achieve Q -factor beyond 10 in a similar frequency band [10].

More importantly, proper radio frequency (RF) inductor characterization methodology is required for accurate inductor performance evaluation and optimization, especially for inductors with such a high Q -factor. To this end, three distinct RF inductor characterization methods were experimentally implemented and compared in this work, namely: 1) S_{11} in a one-port configuration; 2) Y -parameters in a two-port configuration; and 3) S -parameters in a two-port configuration. Through comparison with simulated results generated by Ansys High-Frequency Structure Simulator (Ansys HFSS), the last method is identified as the most appropriate method to characterize inductors with such a high Q -factor. The limitations, leading to larger errors observed for Q -factor extraction in the first two approaches, are analyzed, and they arise due to practical constraints in creating an ideal ground short during high-frequency characterization.

This article serves as an extended version of the previous conference presentation [14]. Section II gives an overview of the design and fabrication of the flex-compatible high Q -factor inductors. Section III presents the inductor characterization results at both dc and RF. Section IV introduces the key inductor engineering considerations, with a focus on the resistive loss due to the inductor's metal traces. Section V provides a case study of the application of these high Q -factor inductors in an LAE resonant switch. Conclusions are drawn in Section VI.

II. INDUCTOR DESIGN AND FABRICATION

Fig. 1(b) shows the die photo of a planar loop inductor demonstrated in this work. Silver was chosen for its relatively low Young's modulus (83GPa) and high conductivity ($\sim 6.3 \times 10^7\text{S/m}$ at 20°C), to facilitate the integration with flexible electronics and to reduce series resistance from metal traces in the inductor. The silver was made 2.5 μm thick, while its skin depth in the 2.4-GHz band is $\sim 1.5\mu\text{m}$. Furthermore, the low-loss substrates available in LAE (e.g., loss tangent of ~ 0.002 for polyimide [15] and ~ 0.004 for Corning glass [16] in LAE, versus on the order of 0.01 or more for Si [17], in the GHz regime) and the absence of conductive

ground near or underneath the inductors eliminate the need for extra design/fabrication complications commonly used for Q -factor enhancement (e.g., patterned ground shields [10] and guard rings [18]). Such a simple design facilitates integration in flexible electronics.

The silver film was deposited by thermal evaporation and patterned by lift-off, at room temperature. Post-annealing in the forming gas at 200°C was performed to increase the grain size of the silver thin film and thus improve conductivity. The inductors were fabricated on glass substrates to ease device characterization with RF probes, and the entire fabrication process can be readily transferred to flexible substrates, due to the low thermal budget. In prior work, we have found that inductor performance on glass or polyimide substrates is identical [8], [9], [19], [20], [21].

III. INDUCTOR CHARACTERIZATION RESULTS

A. Inductor Characterization Results at DC

Series resistance from metal traces is one of the dominant loss mechanisms for inductors. Measured with four-point probes, the dc conductivity of as-deposited silver films was from 4.7×10^7 to $5.0 \times 10^7\text{S/m}$ across the substrate. Post-annealing improved the conductivity by $\sim 13\%$, helping to suppress the resistive loss (more details in Section IV-B). All RF measurement results that follow are collected from inductors after annealing, unless otherwise specified.

B. Inductor Characterization Results at RF

Fig. 2(a) shows the device model of the inductor, where L is the inductance, R is the resistive loss (including series resistance from metal traces, radiation loss, and eddy-current effect, etc.), and C is the parasitic capacitance from coupling between metal traces. In the frequency regime away from the self-resonance frequency [i.e., $\approx 1/2\pi(LC)^{1/2}$, simulated to be $\sim 8.9\text{GHz}$ for the inductor shown in Fig. 1(b)], a more compact equivalent representation can be used to model the inductor, consisting of effective inductance L_{eff} and resistive loss R_{loss} in series. Q -factor is the key metric to quantify resistive loss in an inductor and is defined as follows:

$$Q = \frac{\text{Im}(Z)}{\text{Re}(Z)} = \frac{2\pi f \cdot L_{\text{eff}}}{R_{\text{loss}}} \quad (1)$$

$$Z = |Z| \cdot e^{j\theta_Z} \quad (2)$$

where Z is the inductor's impedance.

An accurate evaluation of inductor with a high Q -factor requires extremely careful RF characterization. For example, assuming an inductor with Q -factor of 60, the phase of inductor impedance θ_Z is $\tan^{-1}(Q) \approx 89^\circ$ (i.e., very close to the ideal inductor-impedance phase), and thus, even minute inaccuracy in the measured θ_Z will lead to a considerable error in Q -factor. The following comparison between the results from three distinct inductor RF characterization methods and Ansys HFSS simulation results further confirms that characterization methodology critically impacts the accurate extraction of effective inductance and Q -factor.

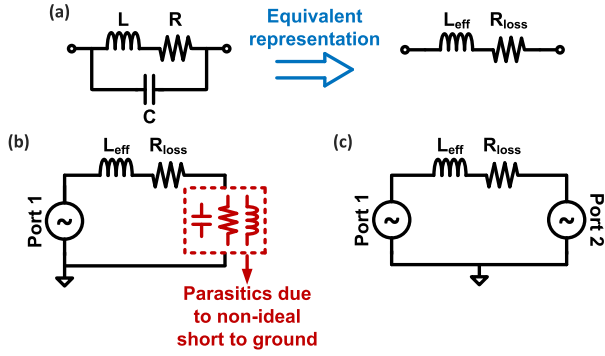


Fig. 2. (a) Device model of inductor. Schematics of inductor in (b) one-port configuration and (c) two-port configuration, for characterization of effective inductance L_{eff} and quality factor Q .

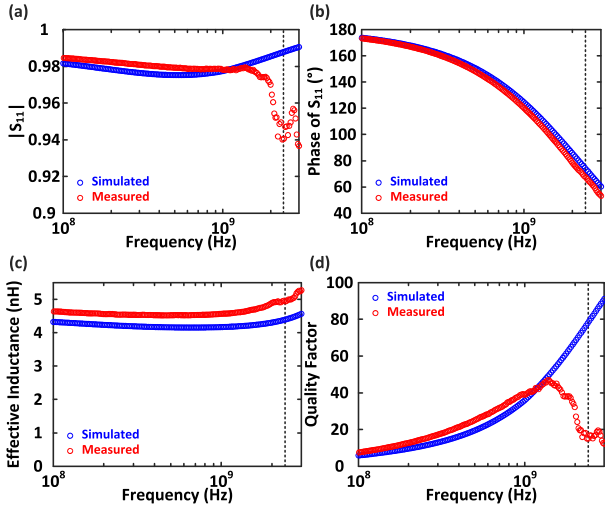


Fig. 3. Comparison of (a) magnitude of S_{11} , (b) phase of S_{11} , (c) effective inductance, and (d) quality factor, between simulation and measurement, using S_{11} in one-port configuration. The vertical dashed lines in the plots indicate 2.4GHz.

1) S_{11} in One-Port Configuration: Fig. 2(b) shows the schematic for characterizing the inductor in a one-port configuration. From the measured S_{11} , the effective inductance L_{eff} and Q are extracted as follows:

$$Z_{11} = Z_0 \cdot \frac{1 + S_{11}}{1 - S_{11}}, \text{ where } S_{11} = |S_{11}| \cdot e^{j\theta} \quad (3)$$

$$L_{\text{eff}} = \frac{\text{Im}(Z_{11})}{2\pi f} = \frac{Z_0}{2\pi f} \cdot \frac{2|S_{11}|}{|1 - S_{11}|^2} \cdot \sin(\theta) \quad (4)$$

$$Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})} = \frac{2|S_{11}|}{1 - |S_{11}|^2} \cdot \sin(\theta). \quad (5)$$

From (5), we can see that the extracted value of Q is very sensitive to $|S_{11}|$, as $|S_{11}|$ is typically close to 1 for inductors, especially with high Q -factor, as in our case. Therefore, the error in S_{11} due to the practical difficulties in creating a perfect short to ground during high-frequency characterization, caused by parasitics shown in Fig. 2(b), propagates to the extracted Q through $|S_{11}|$. Fig. 3 shows that, although there is a good match in both magnitude and phase of the measured and simulated S_{11} (i.e., $< 6\%$ difference in magnitude and $< 10\%$ difference in phase), the extracted values of Q from measurement and simulation differ by a factor up to ~ 8 in the GHz regime,

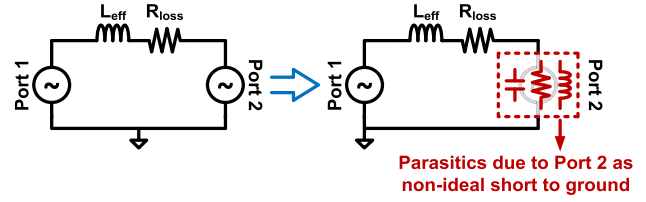


Fig. 4. Schematics of inductor in two-port configuration, for characterization of effective inductance and quality factor using Y_{11} .

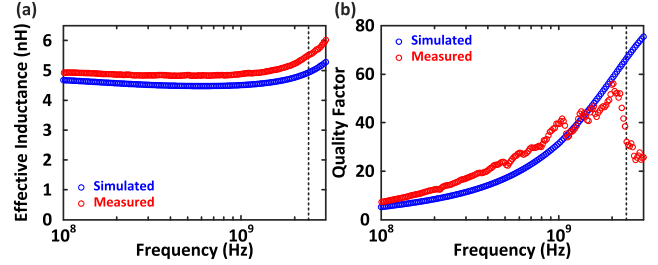


Fig. 5. Comparison of (a) effective inductance and (b) quality factor between simulation and measurement, using Y -parameters in two-port configuration. The vertical dashed lines in the plots indicate 2.4GHz.

as shown in Fig. 3(d). This suggests that using S_{11} in a one-port configuration is not a reliable characterization methodology for high Q -factor inductors demonstrated in this work.

2) Y -Parameters in Two-Port Configuration: Fig. 4 shows the schematic for characterizing the inductor in a two-port configuration using Y -parameters. By creating a short to ground on port 2, L_{eff} and Q can be extracted from Y_{11} using (6) and (7) (equivalently, the extraction can be performed using Y_{22} when port 1 is shorted to ground). Therefore, similar to using S_{11} in the one-port configuration, this method also requires a perfect short on port 2 for accurate extraction of L_{eff} and Q . Thus, Fig. 5 shows that the accuracy is again compromised, as seen by the difference between the simulated and measured Q beyond 2 GHz in Fig. 5(b)

$$L_{\text{eff}} = \frac{\text{Im}(1/Y_{11})}{2\pi f} \quad (6)$$

$$Q = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})}. \quad (7)$$

3) S -Parameters in Two-Port Configuration: From the S -parameters of an inductor in a two-port configuration, L_{eff} and Q can be extracted as follows, to avoid the need to create a perfect short to ground on either port [22], [23]:

$$Z = 2Z_0 \cdot \frac{1 + S}{1 - S}, \text{ where } S = \frac{1}{2}(S_{11} + S_{22} - S_{12} - S_{21}) \quad (8)$$

$$L_{\text{eff}} = \frac{\text{Im}(Z)}{2\pi f} \quad (9)$$

$$Q = \frac{\text{Im}(Z)}{\text{Re}(Z)}. \quad (10)$$

As shown in Fig. 6, the essence of this method is to evaluate L_{eff} and Q under a differential voltage input on the two ends of the inductor. Therefore, ground effectively moves to the middle of the inductor, and therefore, there is no need to have an explicit short to ground on either port. This overcomes

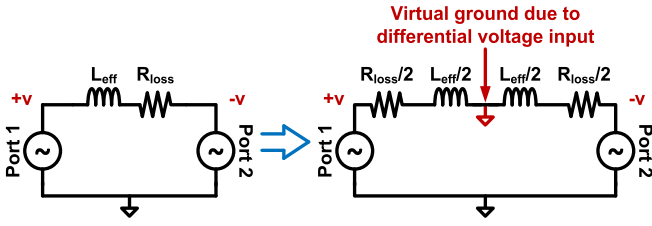


Fig. 6. Schematics of inductor in two-port configuration, for characterization of effective inductance and quality factor using S -parameters.

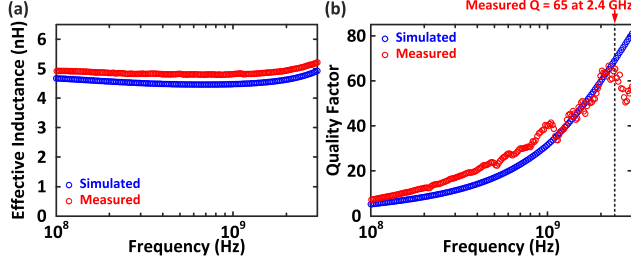


Fig. 7. Comparison of (a) effective inductance and (b) quality factor between simulation and measurement, using S -parameters in two-port configuration.

extraction inaccuracy due to imperfect shorting to ground. Fig. 7 shows that L_{eff} and Q extracted from the S -parameters in the two-port configuration closely match those from the simulation.

IV. KEY DEVICE ENGINEERING CONSIDERATIONS FOR HIGH Q -FACTOR INDUCTORS

Since series resistance from metal traces is one of the dominant loss mechanisms for inductors, it is necessary to minimize such resistance to achieve high Q -factor inductors. Key device engineering considerations towards this are discussed as follows.

A. Analysis of Skin Effect

As the operation frequency of inductors increases, the skin effect raises the series resistance of the metal traces, as it reduces the effective conducting thickness where the current flows [24], [25]. The following expression for skin depth δ governs how much skin effect contributes to the total resistive loss in the inductor demonstrated in this work:

$$\delta = \frac{1}{\sqrt{\pi f \mu_0 \mu_r \sigma}} \quad (11)$$

where σ is the conductivity of silver thin film measured at dc. The relative magnetic permittivity of silver μ_r is assumed to be 1 in this case. Considering the silver thin film thickness t_m of $2.5 \mu\text{m}$ used in this work and the conduction at both top and bottom surfaces of the silver thin film, the effective thickness for conduction t_{eff} can be approximated as a piecewise function of frequency, shown in (12). Fig. 8(a) indicates that the transition frequency between $\delta \geq t_m/2$ and $\delta < t_m/2$ is $\sim 3.3 \text{ GHz}$. We note that the conduction at the two sidewalls of silver thin film is neglected in this analysis, and this is valid due to the high aspect ratio of the cross section of silver thin

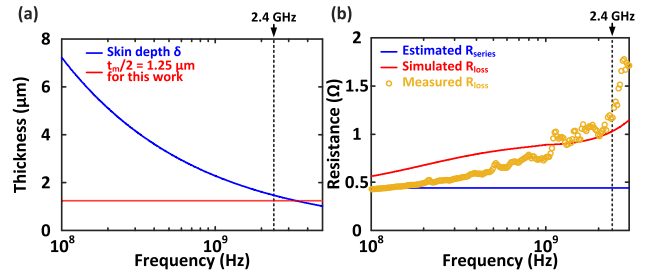


Fig. 8. (a) Skin depth of silver thin film versus frequency. (b) Comparison of the estimated series resistance from metal traces R_{series} and the simulated and measured total resistive loss in inductor R_{loss} .

film [i.e., the trace width is $200 \mu\text{m}$, while the trace thickness is only $2.5 \mu\text{m}$, as shown in Fig. 1(b)]

$$t_{\text{eff}} = \begin{cases} t_m, & \text{if } \delta \geq t_m/2 \\ 2\delta, & \text{if } \delta < t_m/2. \end{cases} \quad (12)$$

Fig. 8(a) shows the calculated skin depth δ versus frequency, in comparison with $t_m/2$ (i.e., $1.25 \mu\text{m}$ for this work). We can see that, as the silver thin-film thickness of $2.5 \mu\text{m}$ used in this work has not reached the thickness limit posed by the skin effect in the 2.4-GHz band, there is still room for further improvement of inductor quality factor through increasing metal trace thickness. More analysis of this aspect is presented in Section IV-C.

With skin effect considered, the series resistance from metal traces R_{series} can be estimated based on the inductor layout shown in Fig. 1(b). Given the silver thin-film thickness of $2.5 \mu\text{m}$ used in this work, Fig. 8(b) compares this estimated R_{series} with the simulated and measured total series resistive loss R_{loss} (see the definition in Section III-B). According to the simulation data shown in Fig. 8(b), the estimated R_{series} of $\sim 0.44 \Omega$ contributes $\sim 43\%$ of R_{loss} at 2.4 GHz, suggesting other sources (e.g., radiation loss [26] and eddy-current effect [27]) being nonnegligible and contributing to the remaining $\sim 57\%$ of R_{loss} in this case.

B. Effects of Post-Deposition Annealing

With the intention of boosting Q -factor of inductors, post-deposition annealing ($5\% \text{H}_2 + 95\% \text{N}_2$ for 1 h at 200°C) is performed to improve the conductivity of silver thin film. The measured inductor metrics before and after annealing are then compared. Although Fig. 9(a) shows that annealing raises the conductivity of the silver film by $\sim 13\%$, Fig. 9(c) indicates that the annealing process only slightly increases the Q -factor below 1 GHz, while the improvement in the GHz regime is negligible. This again supports the understanding that the series resistance from metal trace is not the only major source of resistive loss in the inductor under characterization, with other sources (e.g., radiation loss [26] and eddy-current effect [27]) being nonnegligible in the frequency band of interest.

C. Effects of Metal Trace Thickness

As discussed in Section IV-A, the series resistance from metal traces is directly related to the thickness of inductor's

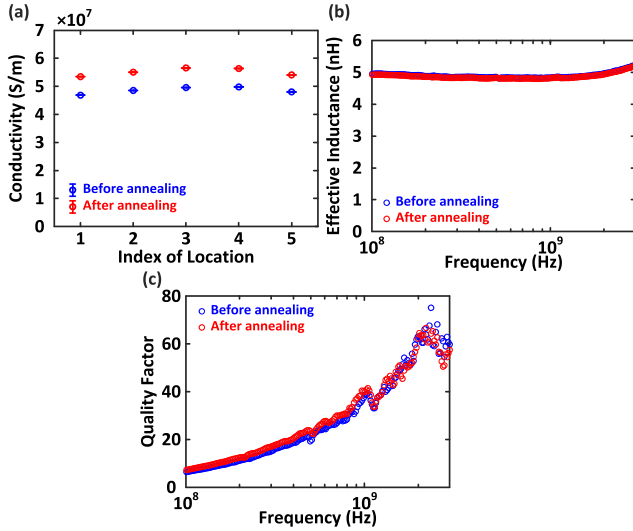


Fig. 9. (a) Comparison of conductivity of silver film before and after annealing, measured by four-point probe (the error bar corresponds to the maximum and minimum values). Comparison of measured (b) effective inductance and (c) quality factor before and after annealing, using S -parameters in two-port configuration.

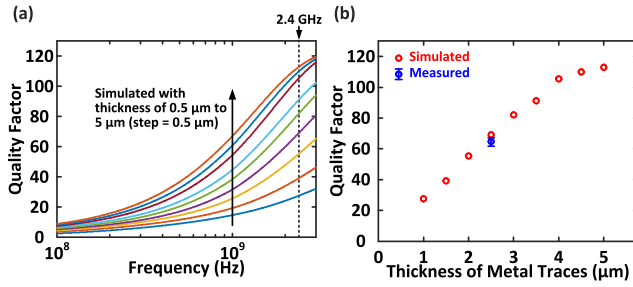


Fig. 10. (a) Simulated quality factor of inductors with different values for metal trace thickness versus frequency. (b) Simulated and measured quality factor at 2.4 GHz versus thickness of metal traces. The error bar for the measured data corresponds to the maximum and minimum values.

metal traces, and there is still room to optimize the quality factor through tuning this thickness value. A set of inductors, with the same geometry as shown in Fig. 1(b) and various values for thickness of metal traces, are simulated. Fig. 10 shows that higher quality factor can be achieved with thicker metal traces, while the improvement in quality factor becomes marginal with thickness of over $\sim 4\mu\text{m}$, limited by skin effect. On the other hand, due to the potentially compromised mechanical properties (e.g., flexibility and stretchability), inductors with thicker metal traces may incur more constraints for applications in flexible and conformal circuits/systems. Therefore, when integrating these flex-compatible inductors with flexible electronics, a careful selection of thickness of metal traces is essential to balance the electrical performance (e.g., resistive losses and thus quality factor) and mechanical performance (e.g., feasible bending radius without damage). This also motivates further study regarding the mechanical properties of these high Q -factor inductors.

V. APPLICATION OF HIGH Q -FACTOR INDUCTOR IN LAE RESONANT SWITCHES

Large-area and flex-compatible inductors with high Q -factor demonstrated in this work have the potential to bring the

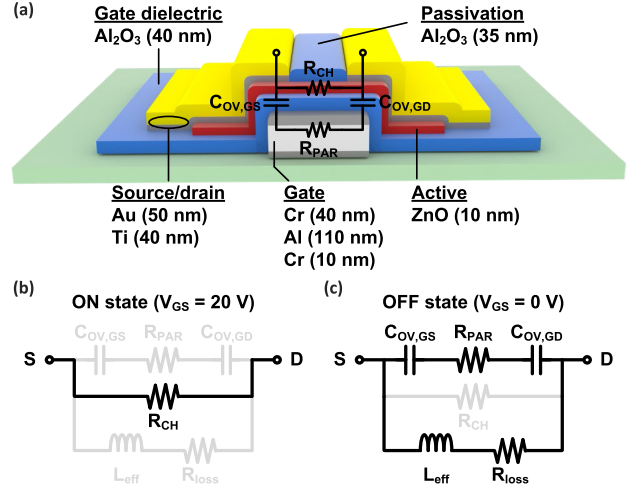


Fig. 11. (a) Schematics of TFT used in LAE resonant switch. Device models of LAE resonant switch in (b) ON state and (c) OFF state. (Adapted from [5].)

operation frequency of LAE circuits/systems into the GHz regime, through resonant operation. One example is the LAE resonant switch based on a TFT with high Q -factor inductor in parallel. This provides gate-controlled switchable impedance between source and drain for effective current regulation in the 2.4-GHz frequency band [5], [6]. Through detailed analysis of the switch's measured OFF-state impedance, this section identifies that resistive loss in TFT, instead of that in the inductor, is the main limiting factor for switch performance and therefore the target for optimization toward further improvement.

A. Structure of Resonant LAE Switch

As shown in Figs. 1(a) and 11, the resonant LAE switch consists of a TFT and a high Q -factor inductor in parallel. When the switch is in ON state (e.g., $V_{GS} = 20\text{V}$), the ON state impedance $|Z_{ON}|$ is predominantly set by channel resistance R_{CH} . When the switch is in OFF state (e.g., $V_{GS} = 0\text{V}$), the OFF-state impedance $|Z_{OFF}|$ consists of the parasitic branch in TFT (i.e., overlap capacitance $C_{GS,OV}$ and $C_{GD,OV}$, in series with parasitic resistance R_{PAR}) and the inductor in parallel. More details on operation principles and modeling of resonant LAE switch can be found in [5] and [6].

B. Analysis of OFF-State Impedance

The OFF-to-ON impedance ratio $|Z_{OFF}/Z_{ON}|$ is used as the key performance metric for LAE resonant switch, as higher $|Z_{OFF}/Z_{ON}|$ leads to a better control of current between the source and drain of the switch. This necessitates a large $|Z_{OFF}|$. Fig. 12 shows a detailed breakdown of the components that affect $|Z_{OFF}|$, and the series-to-parallel transformation can be performed using (13)–(16). At resonant frequency $(1/2\pi(L_{eff,P} \cdot C_{PAR,P})^{1/2})$, $|Z_{OFF}|$ is a parallel combination of the resistive losses from both TFT and inductor, as shown in (17)

$$R_{PAR,P} = R_{PAR} + \frac{1}{[2\pi f(C_{GS,OV} || C_{GD,OV})]^2 \cdot R_{PAR}} \quad (13)$$

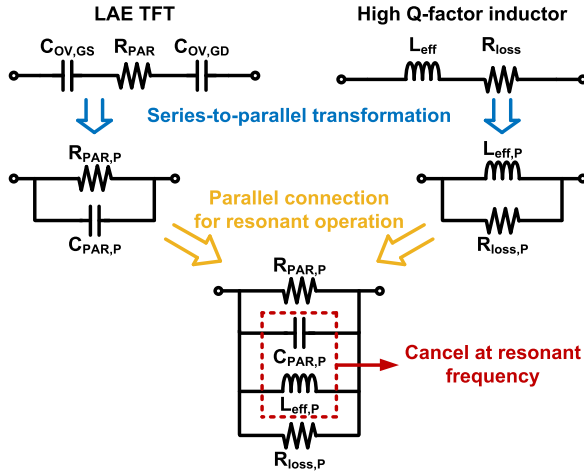
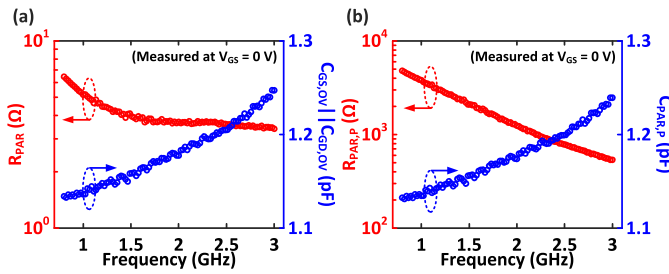


Fig. 12. Analysis of OFF-state impedance for LAE resonant switch.


 Fig. 13. Measured (a) R_{PAR} and $C_{GS,OV} || C_{GD,OV}$ and the corresponding (b) $R_{PAR,P}$ and $C_{PAR,P}$ of a typical TFT used in LAE resonant switch ($V_{GS} = 0V$) versus frequency.

$$C_{PAR,P} = \frac{C_{GS,OV} || C_{GD,OV}}{1 + [2\pi f (C_{GS,OV} || C_{GD,OV}) \cdot R_{PAR}]^2} \quad (14)$$

$$R_{loss,P} = R_{loss} + \frac{(2\pi f L_{eff})^2}{R_{loss}} \quad (15)$$

$$L_{eff,P} = \frac{R_{loss}^2 + (2\pi f L_{eff})^2}{(2\pi f)^2 \cdot L_{eff}} \quad (16)$$

$$|Z_{OFF}| = R_{PAR,P} || R_{loss,P}. \quad (17)$$

Fig. 13 shows the TFT's contributions to $|Z_{OFF}|$ at $V_{GS} = 0V$. R_{PAR} includes resistance from TFT's metal interconnection, resistance across the gate electrode along the channel length direction, and contact resistance between TFT's S/D and channel, and so on. With $C_{GS,OV} || C_{GD,OV}$ of $\sim 1.2pF$ shown in Fig. 13(b), the value for L_{eff} is chosen to be $3.8nH$ to give the desired operation frequency [e.g., $\sim 2.36GHz$ shown in Fig. 14(a)].

In order to identify the dominant source for resistive loss in the entire LAE resonant switch, various values of inductor's Q -factor are used in the simulation of $|Z_{OFF}|$. Fig. 14(a) summarizes the results from both simulation and measurement, and we can see that a high Q -factor of inductor is necessary to achieve a large $|Z_{OFF}|$. In addition, Fig. 14(b) shows that, with Q -factor up to ~ 65 in the 2.4-GHz band, as demonstrated by this work, $|Z_{OFF}|$ is indeed limited by resistive losses in

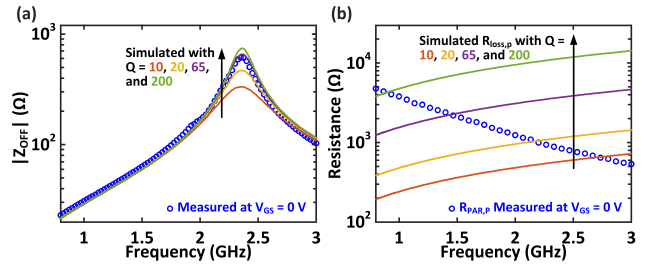
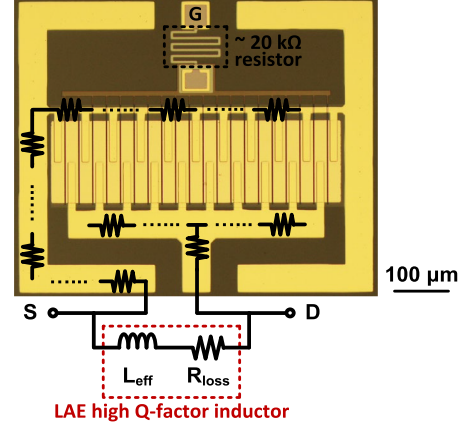

 Fig. 14. (a) Comparison of $|Z_{OFF}|$ from measurement (at $V_{GS} = 0V$) and simulation with various values for quality factor Q . (b) Comparison of the measured $R_{PAR,P}$ at $V_{GS} = 0V$ and the simulated $R_{loss,P}$ with various values for quality factor Q .


Fig. 15. Die photo of the multifinger TFT used in LAE resonant switch, showing the resistance from TFT's metal interconnection.

TFT, instead of that in inductor. Among all possible sources for TFT's resistive losses, the resistance from TFT's metal interconnection is shown in Fig. 15, and it is estimated to be $\sim 3\Omega$, based on the sheet resistance of metal layer and the TFT layout. Since this resistance value is comparable to the value of R_{PAR} in the 2.4-GHz band shown in Fig. 13(a), resistance from TFT's metal interconnection plays a more dominant role in TFT's resistive losses and thus performance of LAE resonant switch, compared to other resistive loss mechanisms in TFT (e.g., resistance across the gate electrode along the channel length direction, and contact resistance between TFT's S/D and channel).

Therefore, further improvement of LAE resonant switch requires reduction of resistive losses in TFT, and possible approaches include using more compact TFT layout to reduce resistance from metal interconnection, increasing the conductivity of metal interconnection (e.g., thicker metal layers and/or metals with higher conductivity). It is evident from the literature [28], [29], [30], [31], [32], [33], [34] that printed silver traces, after appropriate annealing, can reach the same quality factor as evaporated silver.

VI. CONCLUSION

Table I summarizes the key metrics achieved by state-of-art on-chip inductors demonstrated in mainstream electronics technologies (e.g., Si-CMOS and III-V) [10], [11], existing flex-compatible processes [12], [13], and this work. The high

TABLE I

SUMMARY TABLE COMPARING HIGH Q -FACTOR FLEX-COMPATIBLE PLANAR INDUCTOR DEMONSTRATED IN THIS WORK AND PRIOR STATE-OF-ART INDUCTORS

	This work	[10]	[11]	[12]	[13]
Flex-compatible	Yes	No	No	Yes	Yes
Large-area monolithic integration	Yes	No	No	Yes	Yes
Peak quality factor	65 (at 2.4 GHz)	14.3 (at 2.6 GHz)	< 3 (0.1 - 3 GHz)	~21 (at 1 GHz)	14.6 (at 3.45 GHz)
Inductance (nH)	~ 5	4.8 and 5.3	2 - 8.5	10 and 25	~ 6

Q -factor flex-compatible inductor demonstrated in this work features a record-high Q value, which is at least three times that of its counterpart available in other technologies with similar geometry, in a similar frequency band. The high-performance inductor demonstrated here facilitates the development of highly efficient flexible and conformal wireless systems for applications in the IoT and 5G/6G. Future research directions include further suppression of resistive losses in inductors, as well as controlling the change in effective inductance and Q -factor under substrate deformation toward the integration with flexible electronics.

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REFERENCES

- [1] T. Someya et al., "Conformable, flexible, large-area networks of pressure and thermal sensors with organic transistor active matrixes," *Proc. Nat. Acad. Sci. USA*, vol. 102, no. 35, pp. 12321–12325, Aug. 2005.
- [2] Y. Sun and J. A. Rogers, "Inorganic semiconductors for flexible electronics," *Adv. Mater.*, vol. 19, no. 15, pp. 1897–1916, Aug. 2007.
- [3] R. D. Bringans and J. Veres, "Challenges and opportunities in flexible electronics," in *IEDM Tech. Dig.*, Dec. 2016, pp. 6.4.1–6.4.2.
- [4] C. Wu et al., "A phased array based on large-area electronics that operates at gigahertz frequency," *Nature Electron.*, vol. 4, no. 10, pp. 757–766, Oct. 2021.
- [5] C. Wu et al., "Gigahertz large-area-electronics RF switch and its application to reconfigurable antennas," in *Int. Electron Devices Meeting Tech. Dig.*, Dec. 2020, pp. 33.6.1–33.6.4.
- [6] C. Wu et al., "A monolithically integrable reconfigurable antenna based on large-area electronics," *IEEE J. Solid-State Circuits*, early access, Oct. 19, 2024, doi: 10.1109/JSSC.2023.3322905.
- [7] Y. Mehlman, Y. Afsar, N. Yerma, S. Wagner, and J. C. Sturm, "Self-aligned ZnO thin-film transistors with 860 MHz f_T and 2 GHz f_{max} for large-area applications," in *Proc. 75th Annu. Device Res. Conf. (DRC)*, Jun. 2017, pp. 1–2.
- [8] Y. Afsar et al., "Impact of bending on flexible metal oxide TFTs and oscillator circuits," *J. Soc. Inf. Display*, vol. 24, no. 6, pp. 371–380, Jun. 2016.
- [9] Y. Afsar et al., "Oxide TFT LC oscillators on glass and plastic for wireless functions in large-area flexible electronic systems," in *SID Symp. Dig. Tech. Papers*, May 2016, vol. 47, no. 1, pp. 207–210.
- [10] S.-M. Yim and T. Chen, "The effects of a ground shield on the characteristics and performance of spiral inductors," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 237–244, Feb. 2002.
- [11] H. Wu, S. Zhao, D. S. Gardner, and H. Yu, "Improved high frequency response and quality factor of on-chip ferromagnetic thin film inductors by laminating and patterning Co-Zr-Ta-B films," *IEEE Trans. Magn.*, vol. 49, no. 7, pp. 4176–4179, Jul. 2013.
- [12] B. S. Cook et al., "Inkjet-printed, vertically-integrated, high-performance inductors and transformers on flexible LCP substrate," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–4.
- [13] L. Sun et al., "Flexible high-frequency microwave inductors and capacitors integrated on a polyethylene terephthalate substrate," *Appl. Phys. Lett.*, vol. 96, no. 1, Jan. 2010, Art. no. 013509.
- [14] Y. Ma, S. Wagner, N. Verma, and J. C. Sturm, "High quality-factor planar inductors compatible with flexible large-area electronics for integrated IoT and 5G/6G applications," in *Proc. IEEE Int. Flexible Electron. Technol. Conf. (IFETC)*, Aug. 2023, pp. 1–3.
- [15] H. Araki et al., "Low permittivity and dielectric loss polyimide with patternability for high frequency applications," in *Proc. IEEE 70th Electron. Compon. Technol. Conf. (ECTC)*, Jun. 2020, pp. 635–640.
- [16] H. Jain, *Dielectric Properties of Glass*. Accessed: Nov. 25, 2008. [Online]. Available: https://www.lehigh.edu/imi/teched/GlassProp/Slides/GlassProp_Lecture23_Jain2.pdf
- [17] M. N. Afsar and H. Chi, "Millimeter wave complex refractive index, complex dielectric permittivity and loss tangent of extra high purity and compensated silicon," *Int. J. Infr. Millim. Waves*, vol. 15, no. 7, pp. 1181–1188, Jul. 1994.
- [18] Q. Zhang, Y. Wu, C. Zhao, Y. Yu, H. Liu, and K. Kang, "Mechanism analysis and experiment of the effects of the guard ring on the inductors performance," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 3, pp. 275–278, Mar. 2023.
- [19] Y. Hu et al., "Flexible solar-energy harvesting system on plastic with thin-film LC oscillators operating above ft for inductively-coupled power delivery," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2012, pp. 1–4.
- [20] Y. Hu et al., "High-resolution sensing sheet for structural-health monitoring via scalable interfacing of flexible electronics with high-performance ICs," in *Proc. Symp. VLSI Circuits (VLSIC)*, Jun. 2012, pp. 120–121.
- [21] Y. Hu et al., "A self-powered system for large-scale strain sensing by combining CMOS ICs with large-area electronics," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 838–850, Apr. 2014.
- [22] M. Danesh, J. R. Long, R. A. Hadaway, and D. L. Haramé, "A Q -factor enhancement technique for MMIC inductors," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 1998, pp. 183–186.
- [23] E. Lourandakis, *On-Wafer Microwave Measurements and De-Embedding*. Norwood, MA, USA: Artech House, 2016.
- [24] H. A. Wheeler, "Formulas for the skin effect," *Proc. IRE*, vol. 30, no. 9, pp. 412–424, Sep. 1942.
- [25] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*. Boston, MA, USA: Cengage Learning, 2022.
- [26] S. Pinel et al., "Very high- Q inductors using RF-MEMS technology for system-on-package wireless communication integrated module," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, Jun. 2003, pp. 1497–1500.
- [27] B.-L. Ooi, D.-X. Xu, P.-S. Kooi, and F.-J. Lin, "An improved prediction of series resistance in spiral inductor modeling with eddy-current effect," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 9, pp. 2202–2206, Sep. 2002.
- [28] P. J. Smith, D.-Y. Shin, J. E. Stringer, B. Derby, and N. Reis, "Direct ink-jet printing and low temperature conversion of conductive silver patterns," *J. Mater. Sci.*, vol. 41, no. 13, pp. 4153–4158, Jul. 2006.
- [29] S. F. Jahn et al., "Inkjet printing of conductive silver patterns by using the first aqueous particle-free MOD ink without additional stabilizing ligands," *Chem. Mater.*, vol. 22, no. 10, pp. 3067–3071, May 2010.
- [30] X. Nie, H. Wang, and J. Zou, "Inkjet printing of silver citrate conductive ink on PET substrate," *Appl. Surf. Sci.*, vol. 261, pp. 554–560, Nov. 2012.
- [31] D. Zhao, T. Liu, J. G. Park, M. Zhang, J.-M. Chen, and B. Wang, "Conductivity enhancement of aerosol-jet printed electronics by using silver nanoparticles ink with carbon nanotubes," *Microelectronic Eng.*, vol. 96, pp. 71–75, Aug. 2012.
- [32] W. Shen, X. Zhang, Q. Huang, Q. Xu, and W. Song, "Preparation of solid silver nanoparticles for inkjet printed flexible electronics with high conductivity," *Nanoscale*, vol. 6, no. 3, pp. 1622–1628, 2014.
- [33] Y. Mou, Y. Zhang, H. Cheng, Y. Peng, and M. Chen, "Fabrication of highly conductive and flexible printed electronics by low temperature sintering reactive silver ink," *Appl. Surf. Sci.*, vol. 459, pp. 249–256, Nov. 2018.
- [34] E. S. Rosker et al., "Approaching the practical conductivity limits of aerosol jet printed silver," *ACS Appl. Mater. Interfaces*, vol. 12, no. 26, pp. 29684–29691, Jun. 2020.



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