Analyzing and Increasing Yield of ZnO Thin-Film Transistors for Large-area Sensing Systems by Preventing Process-Induced Gate Dielectric Breakdown

Zhiwu Zheng, Levent E. Aygun, Yoni Mehlman, Sigurd Wagner, Naveen Verma and James C. Sturm
Princeton University, Department of Electrical Engineering, Princeton, New Jersey, 08544, USA
Email: zhiwuz@princeton.edu / Phone: (609) 258-6624

Thin film transistors (TFT's) on flexible large-area substrates enable large-scale deployment of form-fitting embedded and tactile sensors. However, the combination of insulating substrates (e.g., glass, plastics), long metal traces for distributed sensors and circuits over large areas, plasma processing and packaging/assembly for hybrid (CMOS-TFT) systems makes anomalous breakdown in TFT gate dielectrics a prominent limiter of yield in complex systems. In this work, we use layout modifications, shielding layers, and temporary "shorting bars" to enable high-yield processing and assembly of distributed sensor-acquisition circuits, in which 161 ZnO TFT's are used per sensor (Fig. 1) to implement compressed sensing (i.e., matrix projection). Although this is a large number of TFT's, compressed sensing greatly enhances critical system metrics, e.g., reduces the number of acquisition cycles and physical interfaces to a readout CMOS IC, as demonstrated in a tactile force-sensing system [1].

ZnO TFT's were fabricated on glass with a bottom-gate staggered structure (Fig. 2). Cr was first evaporated and patterned as gate metal. An Al_2O_3/ZnO/Al_2O_3 stack by RF (13.56 MHz) plasma-enhanced atomic layer deposition (PEALD) at 200 °C (plastic compatible) formed gate dielectric, channel layer, and passivation layer, respectively [2]. After isolation, via etching and passivation removal, source/drain metal was deposited and patterned, followed by a final interconnect layer.

The circuit for compressed sensing requires a matrix of 5 rows each with 32 TFT's. Each row of TFT's is connected to a common long (~8 mm) gate line (Fig. 3) [1]. Initially, when this connection was formed together with the gate electrodes, the TFT's exhibited widespread gate breakdown. We attribute this to non-uniform surface charging along the gate line from the plasma during the PEALD Al_2O_3 deposition, caused by the edge asymmetry between the RF powered electrode and the larger grounded electrodes (sample holder and chamber walls) [3], or to current imbalance due to non-uniform plasma [4] exacerbated by cycling the plasma every atomic layer during the PEALD process. A long metal interconnect under the Al_2O_3 enables electrons to tunnel up and down through the dielectric (Fig. 4). This leads to dielectric breakdown after passage of ~$2x10^{16}$ electrons/cm^2, as we measured on the 40-nm thick Al_2O_3 gate dielectric. Breakdown was prevented by separating the gate metal for each TFT before gate stack PEALD to break the current path, and connecting the gates only after all plasma processing, in a final interconnect step. This approach raised the yield of fully functional 161-TFT die from 2 out of 98 to 40 out of 77. As an added benefit, there was a striking increase in the I-V curve uniformity (Fig. 5) due to less stress in the gate dielectric.

The glass substrate was singulated into individual die with a dicing saw. The initial dicing damaged all 40 die (which had been functional before) by breaking down gate dielectrics, especially of all the sensor-select TFT's (1 of the 161 TFT's per die). Applying metal shielding layers on top of the photoresist-coated glass substrate and its underside did not help significantly. However, modeling capacitive division of an ESD voltage of 10kV between the top and bottom shields estimated only 9V across the gate dielectric (C5 in Fig. 6), not enough to cause failure. On the other hand, a pinhole short in the top photoresist would produce 84V across the gate dielectric, well above its measured breakdown voltage of ~40V. We prevent this damage by depositing temporary metal "shorting bars" between the source/drain and gate of all functional TFT's at transistor level (Fig. 7) to hold zero voltage on the gate dielectric, and remove them after dicing. This brought the die yield (all 161 TFT's functional) to 100% (5 out of 5) after dicing (Fig. 8).

In summary, compression of sensor data in the TFT domain enables a great reduction in the required number of interfaces and acquisition cycles between large-area electronics and CMOS IC's, but requires a high TFT yield. We identified plasma charging damage and ESD during dicing as process steps severely impairing yield, and showed how to prevent such damage using layout modifications and temporary shorting of connections on key components.

This work was supported by the Princeton Program in Plasma Science and Technology, the Semiconductor Research Corporation, and DARPA.

[1] L. Aygun, *et al*., *Proc. ISSCC.*, p. 280 (2019).
[2] Y. V. Li, *et al.*, *71st DRC*, p. 167 (2013).
[3] J. Ballutaud, Ph.D. dissertation, EPFL, ch. 7 (2004).
[4] S. Fang, *et al.*, *J. Appl. Phys.,* vol. 72, p. 4865, (1992).

Authorized licensed use limited to: Princeton University. Downloaded on August 22,2024 at 18:23:31 UTC from IEEE Xplore. Restrictions apply.

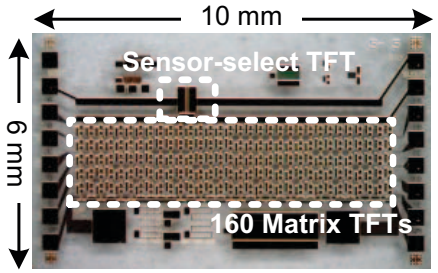

Fig. 1. Die, on glass, of control logic block for selecting sensors and superposing their currents for compressed-sensing acquisition in tactile sensing.

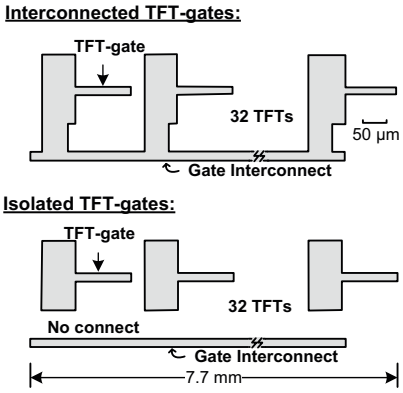

Fig. 3. Top-view layouts of chrome layers for interconnected (top) and isolated (bottom) TFT-gates. 7.7 mm long lines connect the gates of each row of the data compression array.

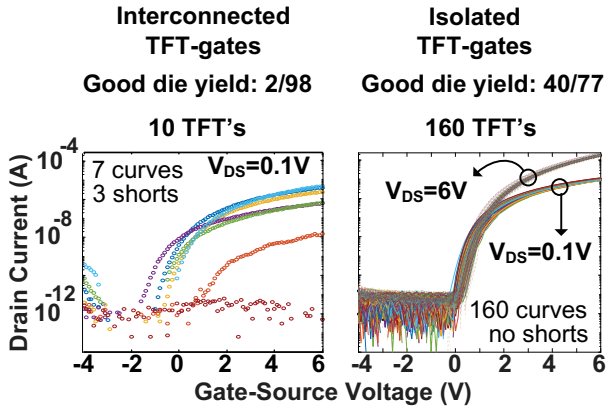

Fig. 5. Transfer curves for (left) 7 of 10 measured TFT's with interconnected gates (3 had gate shorts), and (right) 160 TFT's with isolated gates. Isolating the gates raised the number of die with all 160 TFT's yielding from 2/98 to 40/77.

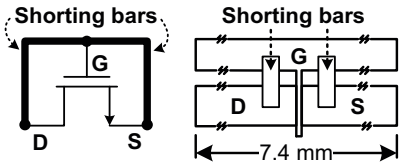

Fig. 7. Shorting bar applied to the sensor-select transistor.

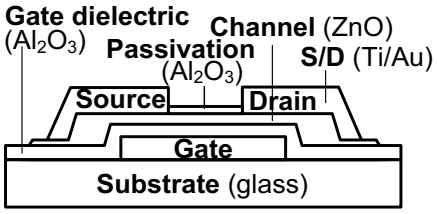

Fig. 2. In-house fabricated evaporated-Cr bottom-gate TFT, with dielectric (Al_2O_3), channel (ZnO), and passivation layer (Al_2O_3) deposited by PEALD, followed by evaporated source/drain (S/D) metal. Final interconnect not shown.

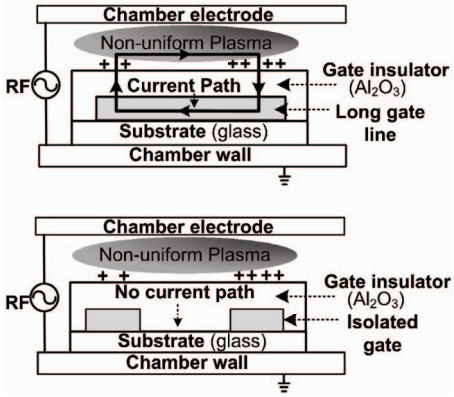

Fig. 4. Visualization of net current through gate dielectric due to non-uniform plasma (top) and its suppression by isolating the electrodes in each row of gates (bottom).

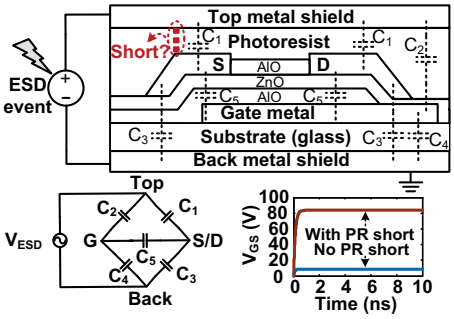

Fig. 6. Electrical model of effect of electrostatic discharge during dicing, showing how capacitive coupling determines induced gate-source/drain voltage (voltage on C_5). Assuming a 10kV ESD event and no pinhole in the photoresist, only an (inconsequential) 9V is developed on the gate dielectric. A short through a photoresist pinhole raises the voltage on the dielectric to 84V (enough to damage the dielectric).

Top & bottom Metal shield	Shorting bars	Die yield
No	No	0/40
Yes	No	3/20
Yes	Yes	5/5

Fig. 8. Comparison of effects of top and bottom metal shields *vs.* shorting bars in reducing die loss due to ESD during dicing.

Authorized licensed use limited to: Princeton University. Downloaded on August 22,2024 at 18:23:31 UTC from IEEE Xplore. Restrictions apply.