f_{MAX} Exceeding 3 GHz in Self-Aligned Zinc-Oxide Thin-Film Transistors with Micron-Scale Gate Length

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Introduction

Large-area electronic (LAE) metal-oxide thin-film transistors (TFTs) with f_T and/or f_{MAX} beyond 1 GHz demonstrated over recent years [1-3] enable critical circuits and systems towards wireless applications in Internet of Things and 5G/6G (e.g., a 1-GHz phased array for far-field radiation beam steering [4]). Since most existing approaches towards GHz TFTs rely on improved charge-carrier mobility through high-temperature deposition of semiconductors and/or submicron TFT feature size achieved by electron-beam lithography, they are incompatible with low-cost, large-area, and flex-substrate fabrication of TFTs. By additional dependence on gate resistance R_G, f_{MAX} opens broader device engineering space to maintain large-area and flex-compatibility, and motivates f_{MAX}-limited circuit/system topologies [4]. Here, we show that with optimal TFT bias voltages and reduced R_G through TFT width scaling, a record-high f_{MAX} exceeding 3 GHz is achieved in self-aligned zinc-oxide (ZnO) TFTs with gate length of $\sim 1\ \mu m$, patterned by photolithography, with a maximum process temperature of ~ 200 ℃. A high-frequency non-quasi-static TFT model [5] is used to guide the device engineering efforts towards this result.

Device Fabrication

Fig. 1(a) shows the cross-section of the bottom-gate staggered ZnO TFT [5]. Its key features include: (1) a composite gate electrode of 10-nm Cr/110-nm Al/40-nm Cr to reduce R_G; (2) photolithography-only patterning (no electron-beam lithography) for minimum gate length of $\sim 1\ \mu m$; (3) self-aligned source/drain metal patterning, resulting in length of source/drain-to-gate overlaps L_{OV} $\sim 0.5\ \mu m$.

Device Characterization Results and Analysis

Fig. 1 shows typical transfer and output curves of ZnO TFTs, and their DC metrics. Fig. 2 shows the high-frequency TFT model and equations for TFT parameter extraction. With the TFT characterized as a two-port network, values for TFT parameters (i.e., C_{GS}, C_{GD}, g_m, τ, r_o, R_G, and C_{DS}) can be extracted from the measured Y-parameters [5]. C_{GS}, C_{GD}, R_G, and C_{DS} are mostly determined by TFT layout and geometry, and thus they are nearly independent of bias voltages. On the other hand, the strongly voltage-dependent g_m and r_o require identifying the optimal bias voltages for maximum f_{MAX}. Figs. 3(a) and 3(b) show the extracted g_m and r_o for $W/L = 50\ \mu m/\sim 1\ \mu m$. The competing effects of g_m (high V_{GS} desired) and r_o (low V_{GS} desired) on f_{MAX} lead to optimal bias voltages of $V_{GS} = V_{DS} = 6\ V$ in Fig. 3(c), which maximize f_{MAX} in the saturation region, below the thermally-induced breakdown limit [5].

Beyond the optimization of TFT bias voltages, f_{MAX} can be further improved by reducing R_G through TFT width scaling, since R_G is the major resistive loss within TFTs. Figs. 4(a) and 4(b) show the maximum available power gain MAG and stability factor k for a range of channel widths W, measured at $V_{GS} = V_{DS} = 6\ V$. Fig. 4(c) shows that an f_{MAX} exceeding 3 GHz is observed in the $W = 15\ \mu m$ TFT. As compared to TFTs with larger W, the $W = 15\ \mu m$ TFT shows slightly worse g_m and τ in Fig. 5(a), due to lower I_{DS} current and thus smaller $V_{DS} \cdot I_{DS}$ power, as less heating lowers the effective electron mobility [6]. While this reduces the MAG of the $W = 15\ \mu m$ TFT at low frequencies in Fig. 4(a), the reduced R_G and thus $k < 1$ maintained up to 3 GHz lead to f_{MAX} beyond 3 GHz.

Finally, the TFT parameters extracted from the width scaling experiment (the value for R_G is estimated from the sheet resistance and geometry of the gate electrode), summarized in Fig. 5(b), are used to simulate MAG and k for the $W = 15\ \mu m$ TFT. Figs. 5(c) and 5(d) show that the simulated MAG and k closely match measurements up to 3 GHz, validating the device characterization and the high-frequency modeling.

Conclusions

Through the optimization of bias voltages and the reduction of resistive loss within TFTs achieved by width scaling, this work demonstrates self-aligned ZnO TFTs with f_{MAX} exceeding 3 GHz, which is among the highest for metal-oxide TFTs with large-area and flex-compatibility. These results suggest that, even with limited channel mobility and using photolithography, TFT parameter engineering is a promising path to GHz LAE systems with f_{MAX}-limited operation. Therefore, robust GHz modeling methodology will be essential to consolidate the understanding of TFT operation, and to guide future device optimization (e.g., to further reduce R_G for higher f_{MAX}).

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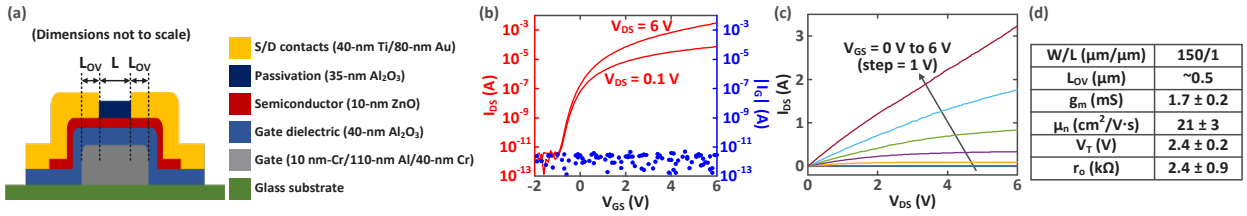

Fig. 1. (a) ZnO TFT cross-section (L = channel length; L_{OV} = length of source/drain-to-gate overlaps). Typical (b) transfer and (c) output curves of ZnO TFTs with $W/L = 150\ \mu m/1\ \mu m$. (d) Mean and standard deviation of device figures of merit, extracted from 10 ZnO TFTs measured at DC ($V_{GS} = V_{DS} = 6\ V$). Adapted from [5].

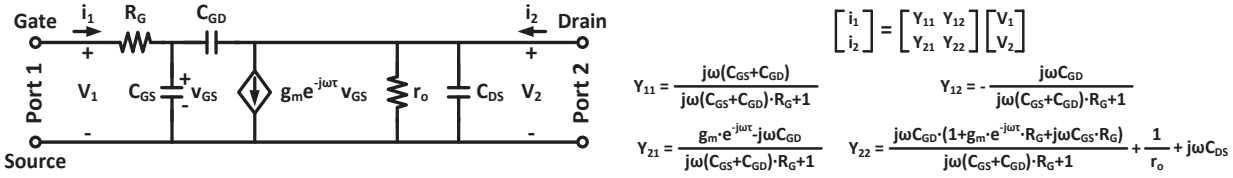

Fig. 2. High-frequency small-signal model for ZnO TFTs and equations for device parameters extraction.

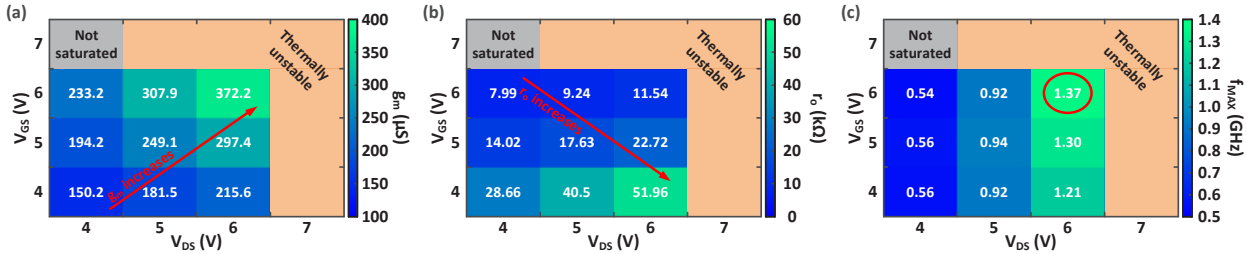

Fig. 3. Values extracted from measurement for (a) g_m and (b) r_o, and (c) measured f_{MAX} of a ZnO TFT with $W/L = 50\ \mu m/{\sim}1\ \mu m$, at various V_{GS} and V_{DS}. The yellow-shaded region labeled "Thermally unstable" corresponds to the bias voltages at which thermally-induced breakdown occurs due to TFT heating. The grey-shaded region labeled "Not saturated" corresponds to bias voltages at which the TFT is in the linear instead of saturation region, assuming $V_T = 2.4\ V$ (Fig. 1(d)). These two unwanted situations limit the feasible range of V_{GS} and V_{DS} for maximizing f_{MAX}.

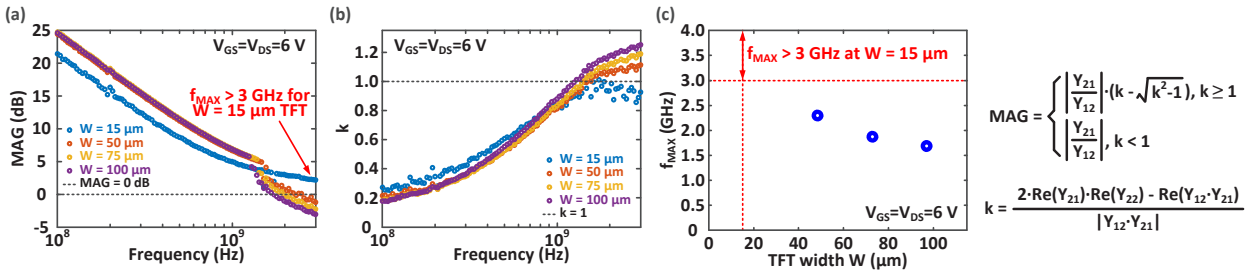

Fig. 4. Measured (a) MAG and (b) k of ZnO TFTs with $L = {\sim}1\ \mu m$ and various W, at $V_{GS} = V_{DS} = 6\ V$. (c) Plot of f_{MAX} extracted from (a) (where MAG drops below 0 dB) versus TFT width W. The frequency limit of the Agilent E5061B vector network analyzer used for high-frequency TFT characterization is 3 GHz.

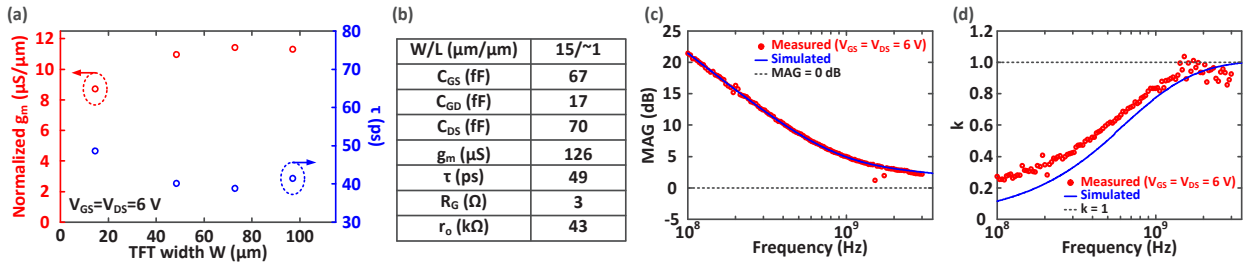

Fig. 5. (a) The values extracted from measurement for normalized g_m and τ, versus TFT width W. (b) The device parameters for $W = 15\ \mu m$ TFT. Comparison of measured and simulated (c) MAG and (d) k for $W = 15\ \mu m$ TFT.

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