High Quality-Factor Planar Inductors Compatible with Flexible Large-Area Electronics for Integrated IoT and 5G/6G Applications

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***Abstract*—Resonant operation, exploiting high quality-factor planar inductors, has recently enabled giga-Hertz applications in large-area electronics, opening up a new technology platform for large-scale and flexible wireless systems. This work presents the design, analysis, and characterization methodology of flex-compatible large-area planar inductors with a record-high quality factor of up to 65 in the 2.4-GHz frequency band. The inductor design and analysis address a key frequency limiter to recently demonstrated large-area and conformal wireless systems for integrated Internet of Things and 5G/6G applications.**

Keywords—Internet of Things, 5G/6G, planar inductor, monolithic integration, flex-compatible

I. Introduction

Large-area electronics (LAE) is a class of technologies that employ low-temperature processing and monolithic integration of semiconductors, metals, and dielectrics over large and flexible substrates of polymers or glass, that can span the order of meters. The rich functionality that LAE offers makes it a promising technology platform for next-generation flexible systems. Recent materials and devices progress has led to giga-Hertz (GHz) LAE systems, enabling large and conformal radiative apertures for future wireless applications in Internet of Things (IoT) and 5G/6G [1], [2]. Large-area flex-compatible planar inductors are a critical technology feature, as they can achieve high quality factors (Q factors) by leveraging large geometries, wide metal traces, and low-loss substrates. Through resonant operation, these inductors have brought the frequency of LAE circuits/systems close to the LAE device limits in the GHz regime. Since this regime is of particular interest for low-power and long-range wireless communication (e.g., 2.4-GHz band for Wi-Fi and Bluetooth), a detailed understanding of the inductor is essential to further system improvements.

Conventional LAE thin-film transistors (TFTs) operate up to 100's of mega-Hertz, limited by large overlap capacitances between source/drain and gate. This parasitic capacitance is minimized by self-alignment, reducing overlaps from $\sim 5\ \mu m$ to $\sim 0.5\ \mu m$. The residual overlap capacitance is further "resonated out" by a high Q-factor inductor in parallel with the TFT. As shown in Fig. 1(a), this enables a narrowband resonant switch with high OFF-state impedance in the 2.4-GHz band [2]. Thus, process-compatible monolithic integration of such inductors can enable highly functional and controllable meta-surfaces based on arrays of such LAE switches.

This work compares planar inductors of 2.5-μm thick silver on glass substrates with a maximum process temperature of $\sim 25℃$ (room temperature) and $200℃$, which are compatible with LAE fabrication on flexible substrates [3], [4]. With metal thickness beyond the skin depth at 2.4 GHz and the benefit of low-loss substrates, the measured Q factor is 65 in the 2.4-GHz band, which is at least 3 times that of prior state-of-art inductors (both flex-compatible and flex-incompatible) with similar geometry, in a similar frequency band [5]-[8]. This is achieved without added design/fabrication complications (e.g., patterned ground shields [5], which are necessary in Si-CMOS to raise Q factor beyond 10 in the similar frequency band).

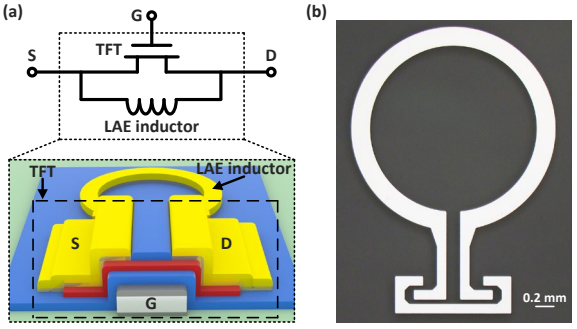

Fig. 1. (a) Schematic of a thin-film transistor in parallel with an LAE inductor, operated as a resonant switch in the GHz regime (adapted from [2]). (b) Die photo of an LAE-based flex-compatible on-chip planar inductor made of 2.5-μm thick silver, with a radius of 1 mm and a trace width of 0.2 mm.

Three distinct inductor characterization methods were used and experimentally compared, namely: (i) S_{11} in a one-port configuration; (ii) Y parameters in a two-port configuration; and (iii) S parameters in a two-port configuration. Through comparison with simulated results generated by Ansys HFSS, the last method is identified as the most appropriate method to characterize inductors with such a high Q factor, due to higher error in the first two approaches for Q factor extraction, caused by practical limitations in creating a perfect short to ground during high-frequency characterization.

Section II gives an overview of the design and fabrication of the flex-compatible high Q-factor inductors. Section III presents the inductor characterization results at both DC and radio frequency (RF). Conclusions are drawn in Section IV.

II. Inductor Design and Fabrication

Fig. 1(b) shows the die photo of a planar loop inductor demonstrated in this work. Silver was chosen for its relatively low Young's modulus ($83\ GPa$) and high conductivity ($\sim 6.3 \times 10^7\ S/m$ at $20℃$), to facilitate the integration with flexible electronics and to minimize series resistance in the inductor. The silver was made $2.5\ \mu m$ thick, about twice its skin depth of $\sim 1.3\ \mu m$ in the 2.4-GHz band. Furthermore, the low-loss substrates available in LAE (e.g., loss tangent of ~ 0.002 for polyimide [9] and ~ 0.004 for Corning glass [10] in LAE, vs. on the order of 0.01 or more for Si [11], in the GHz regime) and the absence of conductive ground near or underneath the

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inductors eliminate the need for extra design complications commonly used for Q factor enhancement (e.g., patterned ground shields [5] and guard rings [12]). Such simple design facilitates integration in flexible electronics.

The silver film was deposited by thermal evaporation and patterned by lift-off, at room temperature. Post annealing in the forming gas at 200℃ was performed to increase grain size of the silver thin film and thus improve conductivity. The inductors were fabricated on glass substrates to ease device characterization with RF probes. The entire process with its low thermal budget can be readily transferred to flexible/conformal substrates [3], [4].

III. Inductor Characterization Results

A. Inductor Characterization Results at DC

Series resistance is one of the dominant loss mechanisms for inductors. The DC conductivity of as deposited silver films, measured with four-point probes, was from $4.7 \times 10^7\ S/m$ to $5.0 \times 10^7\ S/m$ across the substrate. Post annealing improved the conductivity by ~13%, helping to suppress the resistive loss. All RF measurement results that follow are collected from inductors after annealing, unless otherwise specified.

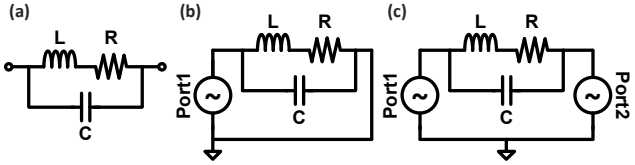

Fig. 2. (a) Device model of inductor. Schematics of inductor in (b) a one-port configuration and (c) a two-port configuration, for characterization of effective inductance and quality factor.

B. Inductor Characterization Results at RF

Fig. 2(a) shows the device model of the inductor, where L is the inductance, R is the resistive loss (series resistance from the metal film, radiation loss, eddy-current effect, etc.), and C is the parasitic capacitance from coupling between metal traces. Comparison between results from three distinct inductor RF characterization methods and Ansys HFSS simulation results indicates that characterization methodology critically impacts the accurate extraction of effective inductance and Q factor.

1) S_{11} in One-port Configuration

Fig. 2(b) shows the schematic for characterizing the inductor in a one-port configuration. From the measured S_{11}, the effective inductance L_{eff} and Q are extracted as follows:

$$Z_{11} = Z_0 \cdot \frac{1+S_{11}}{1-S_{11}}, where\ S_{11} = |S_{11}| \cdot e^{j\theta} \quad (1)$$

$$L_{eff} = \frac{Im(Z_{11})}{2\pi f} = \frac{Z_0}{2\pi f} \cdot \frac{2|S_{11}|}{|1-S_{11}|^2} \cdot sin(\theta) \quad (2)$$

$$Q = \frac{Im(Z_{11})}{Re(Z_{11})} = \frac{2|S_{11}|}{1-|S_{11}|^2} \cdot sin(\theta). \quad (3)$$

From Eq. (3), we can see that the extracted value of Q is very sensitive to $|S_{11}|$, as $|S_{11}|$ is close to 1 for inductors with high Q factors as in our case. Therefore, the error in S_{11} due to the practical difficulties in creating a perfect short to ground during high-frequency characterization propagates to the extracted Q through $|S_{11}|$. Fig. 3 shows that, although the measured and simulated S_{11} are close to each other in both magnitude and phase ($<$ 6% difference in magnitude and $<$ 10% difference in phase), the extracted values of Q from measurement and simulation differ by a factor up to ~8 in the GHz regime (Fig. 3(d)). This suggests that using S_{11} in a one-port configuration is not a reliable characterization methodology in this work.

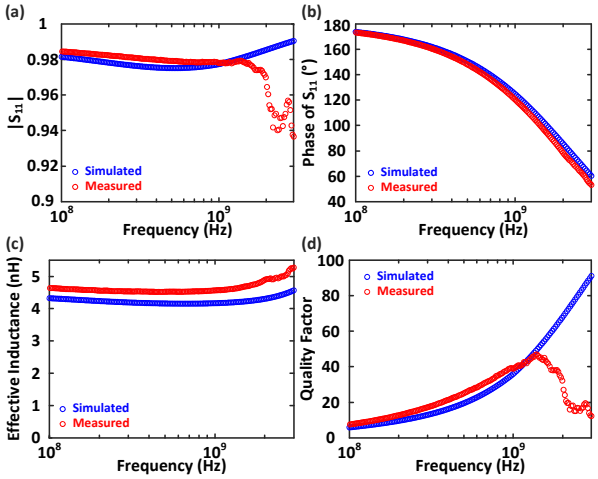

Fig. 3. Comparison of (a) magnitude of S_{11}, (b) phase of S_{11}, (c) effective inductance, and (d) quality factor, between simulation and measurement, using S_{11} in one-port configuration.

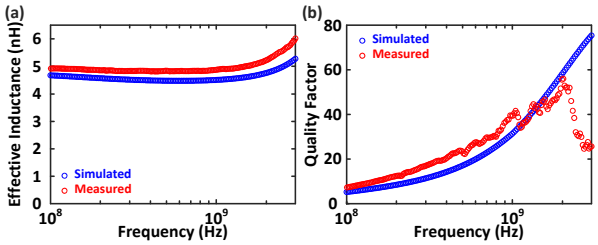

Fig. 4. Comparison of (a) effective inductance and (b) quality factor between simulation and measurement, using Y parameters in two-port configuration.

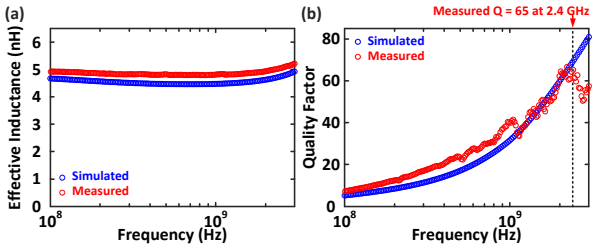

Fig. 5. Comparison of (a) effective inductance and (b) quality factor between simulation and measurement, using S parameters in two-port configuration.

2) Y parameters in Two-port Configuration

Fig. 2(c) shows the schematic for characterizing the inductor in a two-port configuration. By creating a short to ground on port 2, L_{eff} and Q can be extracted from Y_{11} using Eqs. (4) and (5) (equivalently, the extraction can be performed using Y_{22} when shorting port 1 to ground). Similar to using S_{11} in the one-port configuration, this method also requires a perfect short on port 2 for accurate extraction of L_{eff} and Q. Thus Fig. 4 shows that the accuracy is again compromised, as seen by the difference between the simulated and measured Q beyond 2 GHz in Fig. 4(b).

$$L_{eff} = \frac{Im(1/Y_{11})}{2\pi f} \quad (4)$$

$$Q = \frac{Im(1/Y_{11})}{Re(1/Y_{11})} \quad (5)$$

3) S parameters in Two-port Configuration

From the S parameters of an inductor in a two-port configuration, L_{eff} and Q can be extracted as follows, to avoid the need to create a perfect short to ground on either port [13]:

$$Z = 2Z_0 \cdot \frac{1+S}{1-S}, where\ S = \frac{1}{2}(S_{11} + S_{22} - S_{12} - S_{21}) \quad (6)$$

$$L_{eff} = \frac{Im(Z)}{2\pi f} \quad (7)$$

$$Q = Im(Z)/Re(Z). \quad (8)$$

This method evaluates L_{eff} and Q under a differential voltage input on the two ends of the inductor. Therefore, ground effectively moves to the middle of the inductor, and an explicit short to ground is not required on either port. This overcomes extraction inaccuracy due to imperfect shorting to ground. Fig. 5 shows that L_{eff} and Q extracted from the S parameters in the two-port configuration closely match those from simulation.

C. Effects of Post-deposition Annealing

In order to identify the dominant source for resistive loss within the inductors, the Q factors (extracted from S parameters in the two-port configuration) before and after annealing are compared. Although annealing raises the conductivity of the silver film by ~13% (Section III-A), Fig. 6(b) shows that annealing increases the Q factor slightly below 1 GHz, while the improvement in the GHz regime is negligible. This suggests that, in the frequency band of interest, the series resistance from the metal film is not the major source of resistive loss in the inductor. Other sources, e.g., radiation loss [14] and eddy-current effect [15], possibly dominate in this case. These results suggest that the post annealing is not required to achieve such high Q factors.

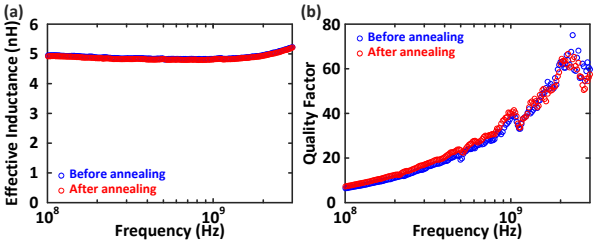

Fig. 6. Comparison of measured (a) effective inductance and (b) quality factor before and after annealing, using S parameters in two-port configuration.

IV. Summary

Table 1 summarizes the key metrics achieved by state-of-art on-chip inductors demonstrated in mainstream electronics technologies (e.g., Si-CMOS and III-V) [5], [6], existing flex-compatible processes [7], [8], and this work. The high Q-factor flex-compatible inductor demonstrated in this work features a record-high Q value, which is at least 3 times that of its counterpart available in other technologies with similar geometry, in a similar frequency band. The high-performance passive demonstrated here facilitates the development of highly efficient flexible and conformal wireless systems for applications in IoT and 5G/6G. Future research directions include further suppression of resistive losses in inductors, as well as controlling the change in effective inductance and Q factor under substrate deformation towards the integration with flexible electronics.

	This work	[5]	[6]	[7]	[8]
Flex-compatible	Yes	No	No	Yes	Yes
Large-area monolithic integration	Yes	No	No	Yes	Yes
Peak quality factor	65 (at 2.4 GHz)	14.3 (at 2.6 GHz)	< 3 (0.1 - 3 GHz)	~21 (at 1 GHz)	14.6 (at 3.45 GHz)
Inductance (nH)	~ 5	4.8 and 5.3	2 - 8.5	10 and 25	~ 6

Table 1. Summary table comparing the high quality-factor flex-compatible planar inductor demonstrated in this work and prior state-of-art inductors.

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