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## Fully-depleted Strained-Si on Insulator NMOSFETs without Relaxed SiGe Buffers

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### Abstract

Fully-depleted strained Si n-channel MOSFETs were demonstrated on a compliant borophosphosilicate insulator (BPSG) without an underlying SiGe buffer layer. Stress balance of a SiGe/Si structure, transferred onto BPSG by wafer bonding and Smart-cut<sup>®</sup> processes, is utilized for the first time to make strained-Si on insulator (sSOI) by a process that does not involve the introduction of misfit dislocations. Strained-Si n-channel MOSFETs with a strain level of 0.6%, equivalent to that of a conventional strained Si layer grown on a relaxed Si<sub>0.85</sub>Ge<sub>0.15</sub> buffer, exhibit 60% mobility enhancement over the control, in good agreement with theory. This approach to fabricating strained Si overcomes any potential process or device complexity due to the presence of a SiGe layer in the final devices.

### Introduction

Strained silicon has drawn attention because of its enhanced high electron and hole mobilities and its compatibility with mainstream Si CMOS processing (1). The strain-induced drive current enhancement is retained even at scaled channel length (2). Tensile strain in silicon is usually created by the pseudomorphic silicon growth on relaxed SiGe layers. A variety of methods, such as graded SiGe buffers (3) and He implantation into SiGe (4), have been employed to form relaxed SiGe, but the involvement of dislocations in these processes poses challenges for device applications, such as control of leakage current and device yield. The defect density can be reduced, but not eliminated, by using thick SiGe layers, resulting in low throughput. Recently, there have been numerous efforts to combine strained silicon with SOI structures to explore SOI-specific benefits, such as a dual-gate possibility (5), reduced parasitic capacitance, and improved device scaling. Most of these approaches consist of formation of relaxed SiGe on insulator (SGOI) and a subsequent tensile Si growth afterwards (6-8). The presence of the SiGe layer in the structure creates processing issues, including germanium diffusion into the strained Si, formation of low-resistance silicide and altered dopant diffusion. Langdo et al. recently obtained SiGe-free strained Si on insulator by transferring strained Si grown on relaxed SiGe buffer layers onto an oxide layer (9). This method requires thick SiGe buffers and it is challenging in selective removal

of thick SiGe while stopping on thin strained Si. Furthermore, the final silicon layer is subject to defects stemming from threading dislocations in the original SiGe buffer. In this report, we use compliant borophosphosilicate glass (BPSG) insulator to realize strained Si on insulator without SiGe buffer layers. Dislocations can be avoided in this process and thick buffer layers are unnecessary. Strained-Si NMOSFETs have been fabricated and show significant mobility enhancement over control devices.

### Fabrication of strained-Si on insulator

To avoid the inevitable dislocations in conventional relaxed SiGe buffers, we recently developed a process for defect-free relaxed SiGe on a BPSG insulator. Thin, fully-strained SiGe layers without defects are first grown on a silicon substrate. The strained SiGe is transferred by wafer bonding and Smart-cut<sup>®</sup> to a BPSG layer, and during annealing the SiGe can expand laterally and relax as the BPSG softens (Fig. 1) (10,11). Strained Si could be grown on these layers, but the SiGe would be present during FET fabrication and in the final structure.

To obtain SiGe-free strained Si on insulator, the process of Fig. 2 was developed, in which unstrained 25 nm Si was grown on top of 30 nm strained Si<sub>0.7</sub>Ge<sub>0.3</sub> before transfer. The Si/SiGe was transferred onto BPSG films, resulting in a strained SiGe/unstrained Si/BPSG structure. The SiGe/Si film was then patterned into islands of edge width from 30 to 200 μm. Annealing at 800°C softened the BPSG and allows the SiGe and Si stack to coherently expand, resulting in same strain change in both films:

$$\Delta \epsilon_{SiGe} = \Delta \epsilon_{Si} \quad (1)$$

where  $\epsilon$  is the strain in the film. The compressive strain in the SiGe relaxes and generates tensile strain in the Si (Fig. 2(b)) (12), which was confirmed by Raman spectroscopy (Figs. 3, 4). The final strain in the SiGe and Si films upon equilibrium is governed by stress balance between the layers (12):

$$\sigma_{SiGe} h_{SiGe} + \sigma_{Si} h_{Si} = 0, \quad (2)$$

where  $\sigma$  and  $h$  refer to the stress and thickness of the films, respectively. Since the lateral expansion occurs at the islands' boundary first and then propagates toward islands' center, the lateral expansion of the islands is much slower on larger islands. After a 90 min anneal at 800°C, stress balance was

### 3.2.1

reached on islands less than 100  $\mu\text{m}$  to create tensile strain in the silicon layer (Fig. 5). A wet etchant was then used to selectively remove the top SiGe film to yield a single tensile Si layer of only  $\sim 20$  nm thickness on BPSG (Fig. 2(b)) (13). Strain level of  $\sim 0.6\%$  was achieved in islands under 100  $\mu\text{m}$  in size. The tensile strain in silicon layer on 200  $\mu\text{m}$  islands was only about 0.15%, far less than the 0.63% expected at stress balance. Control (relaxed) silicon on the same wafer was achieved by removing the SiGe before annealing (Fig. 2(a)). Boron and phosphorus levels in the silicon, estimated by performing secondary ion mass spectroscopy (SIMS) on similar samples, are less than  $2 \times 10^{17} \text{cm}^{-3}$ .

### Device fabrication and results

Self-aligned long-channel NMOSFETs were fabricated using the  $\sim 20$  nm tensile silicon layer, obtained from the 30nm-SiGe/25nm-Si/BPSG structure described in the previous section, as the device channel (Fig. 6). The gate stack was comprised of 300 nm TEOS oxide and 80 nm poly-silicon. Phosphorous implantation (35keV,  $1 \times 10^{15} \text{cm}^{-2}$ ) was used to dope the source/drain and the gate poly. Dopants were activated by annealing at 700°C for 30 min. After device fabrication, Raman spectroscopy confirmed that the strain in the tensile silicon channel did not change, indicating no strain relaxation occurred in the processing steps.

Both strained and unstrained NMOSFETs were well-behaved with strained devices exhibiting much higher driving current. The drain current versus drain voltage at different applied gate voltages is shown in Fig. 7. The transconductance of strained and control devices is plotted in Fig. 8. The effective electron mobility was extracted from the drain current  $I_{DS}$  in the linear regime:

$$I_{DS} = (W/L)\mu_{eff}[C_{ox}(V_{GS} - V_T)V_{DS}], \quad (3)$$

where  $C_{ox}$  is the gate oxide capacitance and  $V_{DS}=10$  mV. Fig. 9 shows the measured effective electron mobility versus gate voltage for both strained and unstrained NFETs on BPSG. The mobility was extracted from devices processed simultaneously with identical geometry. Both the transconductance and effective electron mobility near turn-on were 55-60% higher in the strained silicon devices than in the control, in good agreement with the strain-induced mobility enhancement predicted by theory (Figs. 9, 10) (14).

The mobility enhancement was lower in devices fabricated on larger islands, on which lateral expansion of the SiGe to strain the silicon was slower. On 200  $\mu\text{m}$  islands, where the strain was only  $\sim 0.15\%$  due to insufficient lateral relaxation, the mobility enhancement was 1.2, in line with theory.

### Study of dopant diffusion from BPSG

Further annealing to fully relax large islands in the FET processing would result in dopant out-diffusion from the BPSG to the silicon. Fig. 11 shows that significant diffusion of boron occurred during annealing at 850°C for 1 hr. A  $\text{Si}_3\text{N}_4$

layer, sandwiched between BPSG and Si/SiGe layers, was tested to block the detrimental dopant diffusion. Prior to the Si/SiGe layer transfer onto BPSG, a 5.5 nm  $\text{Si}_3\text{N}_4$  layer was deposited on 10nm-Si/30nm-Si<sub>0.7</sub>Ge<sub>0.3</sub>/Si-substrate at 725°C using LPCVD. The layer transfer was then carried out, resulting in a structure of 30nm-Si<sub>0.7</sub>Ge<sub>0.3</sub>/10nm-Si/5.5nm-Si<sub>3</sub>N<sub>4</sub>/BPSG (Inset in Fig. 12). The dopant out-diffusion was completely suppressed with the boron level below SIMS resolution after annealing at up to 900°C for 1 hr (Fig. 11). Since the nitride film is not viscous but elastic, the nitride layer must be stretched along with the silicon layer during the lateral expansion of SiGe/Si. Upon stress balance, the compressive stress in the SiGe layer needs to balance out the tensile strain in both the silicon and nitride layers, leading to less tensile strain in the silicon layer than in nitride-free structures. When the nitride film is thin (5.5nm in our test), its effect on stress balance can be small and considerable tensile strain in the Si layer can still be generated. Raman spectroscopy performed on 30nm-Si<sub>0.7</sub>Ge<sub>0.3</sub>/10nm-Si/5.5nm-Si<sub>3</sub>N<sub>4</sub>/BPSG at stress balance indicates 0.7% tensile strain in the Si layer (Fig. 12), equivalent to Si grown on a relaxed Si<sub>0.82</sub>Ge<sub>0.18</sub> layer. This is actually slightly greater than the strain in the nitride-free device structure, due to the thinner silicon layer.

### Conclusions

Fully-depleted strained-Si NMOSFETs were demonstrated in a compliant BPSG structure that avoids SiGe in the final devices and does not require dislocations in buffer layers or at interfaces. The enhancement of the mobility due to the strain agrees well with theory. Adverse diffusion from BPSG during high-temperature annealing can be suppressed using a thin nitride film as a diffusion barrier. The process is highly scalable and requires fewer processing steps than other proposed sSOI fabrication techniques.

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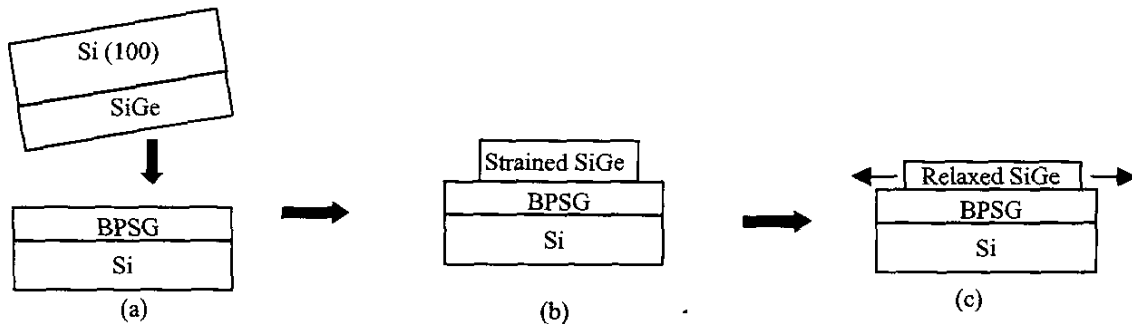


Fig. 1. Process flow of relaxed SiGe on BPSG insulator: (a) strained SiGe grown pseudo-morphically on Si(100) is transferred onto a BPSG layer by wafer bonding and Smart-cut<sup>®</sup> processes, (b) strained SiGe islands on BPSG are formed by plasma etching, and (c) strained SiGe islands relax by lateral expansion as BPSG softens during high-temperature annealing. Note no dislocations are required to change the in-plane lattice constant. [10,11].

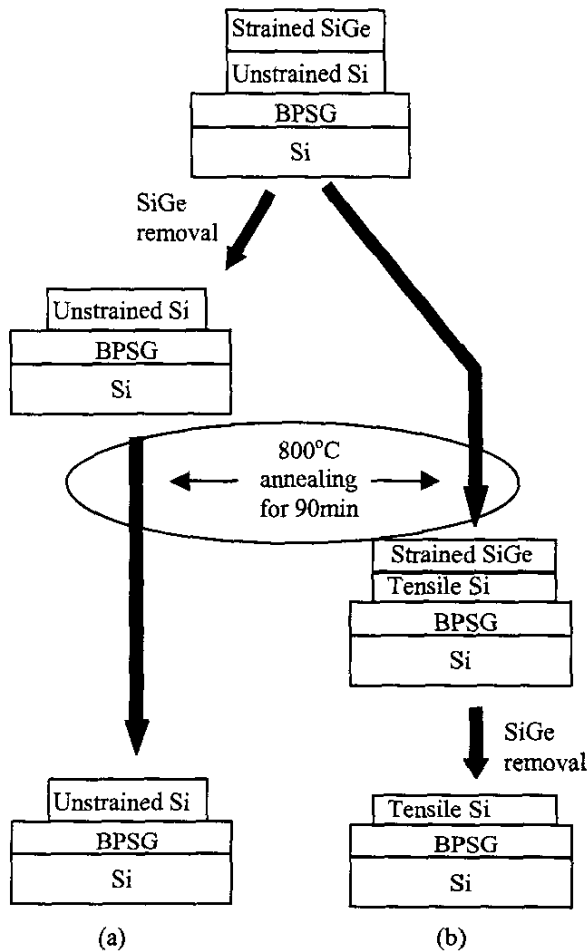


Fig. 2. Process flow of (a) unstrained Si on a BPSG insulator and (b) strained Si on a BPSG insulator. The strained SiGe/unstrained Si/BPSG at the top of this process flow diagram is made by the same process as shown in Fig. 1 (a) and (b) except that a thin unstrained Si layer is grown on top of the SiGe before transfer (12).

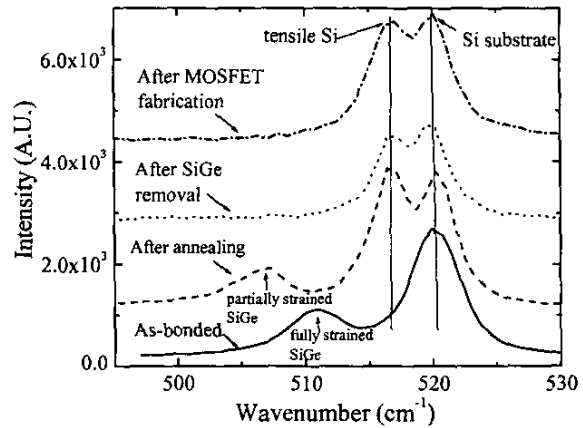


Fig. 3. Raman spectrum (Si-Si nearest neighbor vibration mode) measured at the center of a 90 μm x 90 μm island at various stages of processing. The peak positions depend on composition and strain. The annealing reduces compressive strain in the SiGe and adds tension in the Si. The FET process does not alter the strain in the Si.

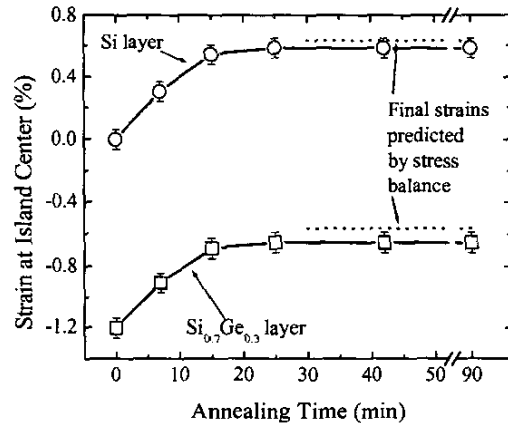


Fig. 4. Biaxial strain (from micro-Raman spectroscopy) of 30nm Si<sub>0.7</sub>Ge<sub>0.3</sub> and 25nm Si films at the center of a 30 μm x 30 μm island as a function of annealing time at 800°C, showing evolution of strain in silicon. Dashed lines are calculations of stress balance.

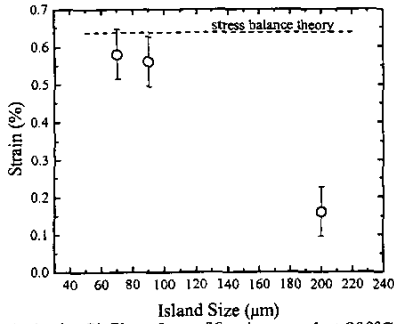


Fig. 5. Strain in the Si film after a 90 min anneal at 800°C as a function of island size, showing complete lateral relaxation on small islands.

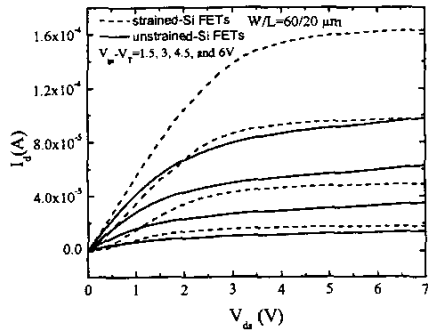


Fig. 7.  $I_d$ - $V_{ds}$  characteristic of the strained ( $\epsilon=0.56\%$ ) devices and the control (relaxed silicon on insulator) device on the same wafer.

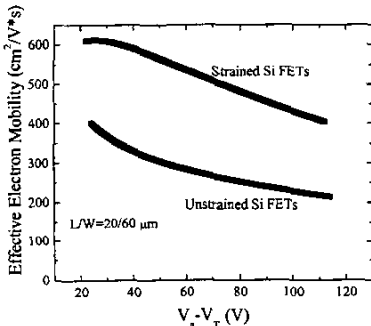


Fig. 9. Effective electron mobility of NFETs measured on 90 $\mu$ m islands ( $\epsilon=0.56\%$ ) as a function of gate voltage.

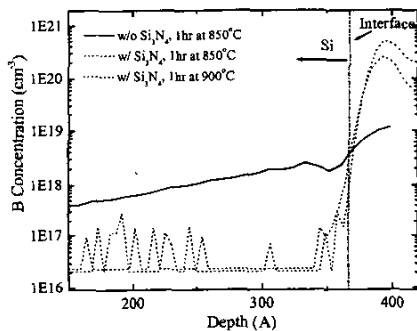


Fig. 11. Boron concentration around the silicon interface measured by SIMS. The vertical line denotes the Si/BPSG interface. The boron diffused significantly in the sample without a nitride layer. A 5.5 nm nitride layer between the BPSG and silicon completely hinders boron diffusion even for annealing at 900°C for 1 hr.

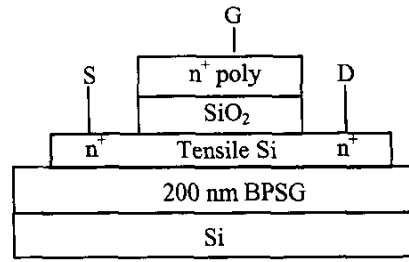


Fig. 6. Schematic diagram of n-channel FETs. The final tensile silicon thickness is about 20 nm.

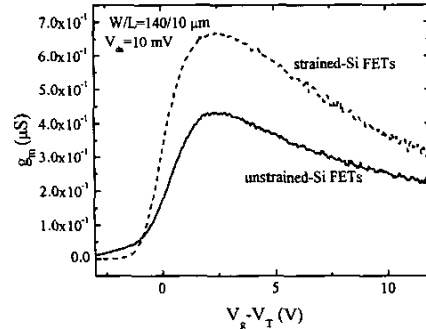


Fig. 8. Transconductance of n-channel FETs on 90 $\mu$ m islands ( $\epsilon=0.56\%$ ) as a function of gate voltage.

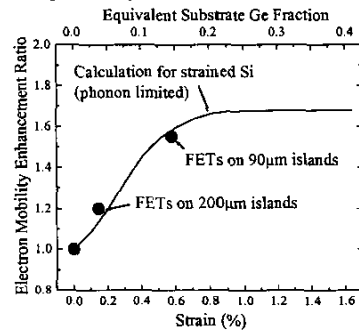


Fig. 10. Electron mobility enhancement, measured near turn-on, as a function of strain in the silicon channel layer. Also shown on the top x-axis is the Ge fraction in relaxed SiGe buffers in conventional strained Si on relaxed SiGe structures to give the same strain as that on the lower x-axis.

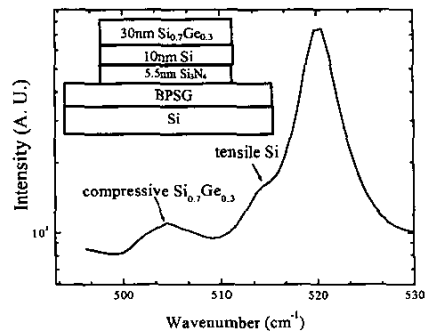


Fig. 12. Raman spectrum (Si-Si neighbor vibration mode) measured at the center of a 30  $\mu$ m  $\times$  30  $\mu$ m island (30nm-SiGe/10nm-Si/5.5nm-Si<sub>3</sub>N<sub>4</sub>/1 $\mu$ m-BPSG) after annealing at 800°C for 30 min. The Si layer is still stretched by compressive SiGe even when Si<sub>3</sub>N<sub>4</sub> layer is present.

### 3.2.4