Polycrystalline Semiconductors VI
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Preface

This book contains contributions that were presented at the International Conference on Polycrystalline Semiconductors having taken place from September 10 to 13, 2002, in Nara, Japan. Nara, the old emperor town, with its beautiful peaceful ancient buildings and with its stimulating vivacity was just the right place for this seventh conference of a whole series of POLYSE conferences. More than 100 participants from 7 countries gathered in the Nara Town Hall (Shinkokaido) and all the presentations took advantage from the cultural flair of the No theatre the stage of which provided the speaker's rostrum.

Like the previous conferences, POLYSE 2002 covered many aspects of polycrystalline semiconductors, but without doubt paid tribute to the strongly increasing economic importance of polycrystalline materials in devices like flat panel displays or thin film solar cells. Nevertheless, fundamental aspects from defect engineering problems to detailed engineering questions were broadly covered. Thus, again like at previous POLYSE conferences, a community with broad interest ranging from basic science to device engineering conducted fruitful discussions at a very high level to advance science and engineering.

The invited presentations were again a trigger to vivid discussion. The speakers presented a broad range of topics, interesting current problems and aspects reaching into the future. These invited speakers were:

J. D. Casperson	H. Fujiwara
H. Ichinose	J. Jang
S. Miyazaki	H. Mizuta
P. Roca I Cabarrocas	T. Shiba
U. Weber	M. Wu

We are grateful for their timely and excellent introductory presentations. These invited talks were accompanied by 33 oral and by 41 poster presentations. We would like to thank all the authors for their interesting contributions that present state-of-the-art research. Most of these contributions are found in these proceedings.

We obtained much support for the success of POLYSE 2002 and are very grateful to the members of our International Advisory Committee who supported us by invaluable input on topics and by suggestions of potential speakers. We also want to acknowledge the many sponsors and exhibitors, whose financial support certainly took a considerable share in the fruitful and successful course of the conference.

There existed a back-stage scenary where many helpful assistants assured smoothly planning and conduction of the conference. These persons deserve our cordial thanks for their endurance and concern.

Nara, Tokyo, Erlangen, and Stuttgart

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Polycrystalline silicon thin film transistors for CMOS on flexible steel foil substrates

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Keywords: Polycrystalline silicon, Thin film transistors, Steel foil substrate, Complementary metal-oxide-semiconductor circuit

Abstract. We made complementary metal-oxide-silicon circuits from polycrystalline silicon thin film transistors on steel foil substrates. As-rolled steel foils can be planarized and electrically insulated with a combination of spin-on and plasma-deposited SiO_2, which also functions as the barrier against contaminant diffusion. The processes at temperatures of up to 950°C include the furnace crystallization of amorphous silicon precursor films, thermal annealing of ion implants in self-aligned geometries, and thermal oxidation of the polycrystalline silicon film. Individual thin film transistors have reached electron and hole mobilities of 60 $cm^2V^{-1}s^{-1}$ and 15 $cm^2V^{-1}s^{-1}$, respectively. The propagation delay in ring oscillators is 1 μs per gate, and is determined by the channel resistance and the coupling capacitance between thin film transistor and substrate. Our work introduces polycrystalline silicon circuits on steel foil as a robust technology for flexible backplanes.

Introduction

Electronics on flexible steel substrates is becoming more and more interesting for flexible displays, curved circuits, curved detector arrays, mechatronic materials, sensor skins, and other large-area electronics [1,2]. Thin film transistors (TFTs), circuits, and display backplane matrices made from hydrogenated amorphous silicon (a-Si:H) have been fabricated on flexible substrates of plastic or steel [3,4,5]. Placing polycrystalline silicon (polysilicon) circuits on flexible substrates is desirable for driving high current loads such as organic light emitting diodes (OLEDs), and for monolithic integration of switching matrices with driver circuits.

Polysilicon films best suited for TFTs are made by crystallizing hydrogenated amorphous silicon precursor films. Crystallization techniques [6] include furnace annealing [7], rapid thermal annealing by lamp heating [8], and laser crystallization [9,10]. Furnace annealing produces highly uniform polysilicon films over large areas, and is a proven batch process. Crystallization and further processing are restricted to temperatures at or below the strain points of affordable substrate glasses of ~600°C, which requires annealing times as long as 20 hours [11,12]. Catalyzed crystallization can reduce this time to ~5 hours [13,14,15], which is still long when compared to the throughput of one plate per minute desired of the single-substrate cluster tools employed in the manufacture of active-matrix liquid-crystal displays. To find a fast and furnace-based crystallization process for large areas of low cost substrates, to enable the integration of driver circuits for active matrices, has been the primary goal of our and other research [16,17,18,19]. The melting point of steel lies about 1400°C, close to the melting point of single crystal silicon of 1414°C. Steel substrates allow raising the temperature for crystallizing the amorphous precursor film, which raises the crystal growth rate

exponentially, so that the crystallization time is reduced dramatically [20,21,22]. Indeed, polysilicon can be formed on steel with furnace crystallization times of minutes or seconds at temperatures up to 950°C

Another attractive feature of steel substrates is their flexibility and ruggedness. a-Si:H TFTs on sufficiently thin steel foil substrates can be bent to a radius of curvature as small as 1 mm without degradation of TFT performance [23,24]. This is attractive for fabricating flexible displays and sensor arrays. Organic light emitting diodes driven by a-Si:H TFTs on thin steel foil have been demonstrated [3], and a flexible reflective display was made from electronic ink driven by a-Si:H TFT matrix on steel [5]. Because steel is opaque, it can be used for emissive and reflective, but not for transmissive displays.

We crystallized polysilicon films on steel at temperatures ranging from 600°C to 950°C, with crystallization time ranging from ~6 hours at 650°C to 20 seconds at 950°C. First we tested mobility using coplanar top-gate TFTs in a non-self-aligned geometry with a deposited source/drain, and then in a more conventional self-aligned geometry with ion-implanted source/drain. Then, using a self-aligned TFT process, we made polysilicon complementary metal-oxide-semiconductor (CMOS) circuits on steel with CMOS inverters and ring oscillators.

Furnace crystallization of amorphous silicon on steel

200-µm-thick foils of AISI grade 304 stainless steel (Fe/Cr/Ni 72/18/10 wt.%) were cleaned with acetone and methanol. To reduce the roughness of the steel foil surface, a 210-nm-thick planarizing film of phosphorus-doped (0.5%) spin-on glass (SOG) was applied to both sides and baked. Then a 270-nm thick film of SiO_2 was deposited on both sides by plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of 250°C. Substrates were then heated in a tube furnace from 450°C to 800°C and cooled to 600°C, at a heating/cooling rate of 5°C/min. The ~0.5 µm thick insulation layer reduced the RMS surface roughness from 6 nm for bare steel foil to 2 nm as measured by atomic force microscopy (AFM).

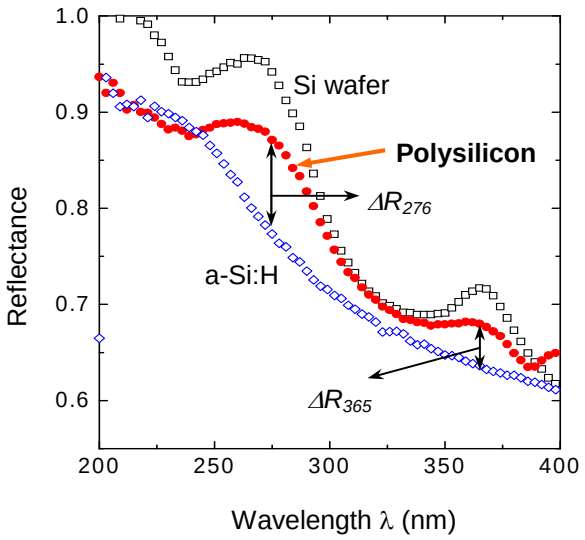

Figure 1. The reflectance spectrum of a fully crystallized polysilicon in the ultraviolet range. Spectra of c-Si and a-Si:H are plotted for comparison.

A 160 nm thick precursor film of a-Si:H was deposited by PECVD from pure silane at a substrate temperature of 150°C. The hydrogen content of these films is $3x10^{21}$ atoms/cm^3 [15]. Because the rate of nucleation has a higher activation energy than the rate of crystal growth [20,21,22], raising the crystallization temperature above 600°C increases the number of nuclei, reduces their size, and reduces the field effect mobility [25]. Somewhere above 850°C the nucleation rate is expected to drop while the growth rate keeps rising [20], so that at still higher temperature the grain size and hence the field effect mobility are expected to rise again [26]. Koster [20] suggested that the grain size starts increasing around 850°C, but Hatalis [26] used rapid thermal annealing to find that the smallest grains are obtained at ~1100°C. We explored crystallization temperatures of up to 950°C.

Reflectance of the film in the ultra-violet (UV) wavelength range has been used by many researchers to monitor the crystallization *ex situ* [7,8,15]. Figure 1 shows the UV reflectance spectrum of a polysilicon film crystallized at 600°C for 6 hours. Before the UV reflectance measurement, the polysilicon-on-steel is first cleaned in very dilute hydrofluoric acid ($HF:H_2O$ ~ 1:100) for ~ 20 sec. The UV reflectance spectrum is measured with a Hitachi U-3410 spectrophotometer. The difference between the reflectance of polysilicon and that of an a-Si:H film at 276 nm, ΔR_{276}, and 365 nm, ΔR_{365}, are used to monitor the completion of crystallization. Because ΔR_{276} is more pronounced than ΔR_{365}, it is more often used. ΔR_{276} keeps increasing during crystallization, and saturates at ~ 7.5% as crystallization approaches completion [15].

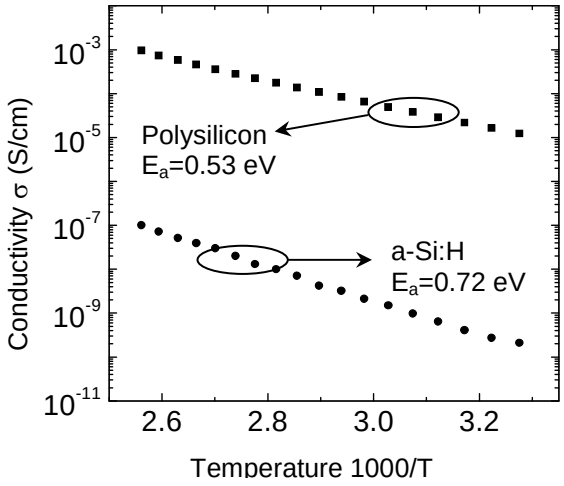

Figure 2. Conductivity in the dark of polysilicon and a-Si:H films. The polysilicon film was formed by furnace crystallization at 600°C/6 hour. The a-Si:H film was grown by PECVD at 250°C.

The dark conductivities σ of all polysilicon films were measured at room temperature to check for possible doping by contamination from the metal substrate. They lie at ~10^{-6} $S \cdot cm^{-1}$, i.e., not much above the conductivity of intrinsic polysilicon film prepared on glass substrates [27]. Figure 2 shows the conductivities as a function of temperature of a polysilicon film crystallized at 600°C and a PECVD a-Si:H film deposited at 250°C using a process optimized for a-Si:H TFTs (which is different from the deposition of a-Si:H for the TFTs of this paper). The thermal activation energies are 0.53 eV and 0.72 eV for polysilicon and a-Si:H films respectively. The activation energy of 0.53 eV suggests that the Fermi level is pinned at midgap. Crystallization at higher temperature and longer annealing time left the dark conductivity unchanged. This suggests an absence of metal contamination during crystallization process.

Transmission electron microscopy (TEM) is used to check the crystallinity and grain size of the polysilicon film. For TEM the polysilicon film was patterned into ~ 1 mm dots by dry etching. The SOG and SiO_2 were wet etched by buffered oxide etchant (BOE), and the floating polysilicon films were collected on the TEM substrate holder. Figure 3 is a dark-field transmission electron micrograph of polysilicon crystallized at 950°C/20 sec. The polysilicon on steel has the same dendritic grain as furnace-crystallized polysilicon on glass substrate or oxidized silicon wafer [30]. The average grain size of is ~0.5 μm.

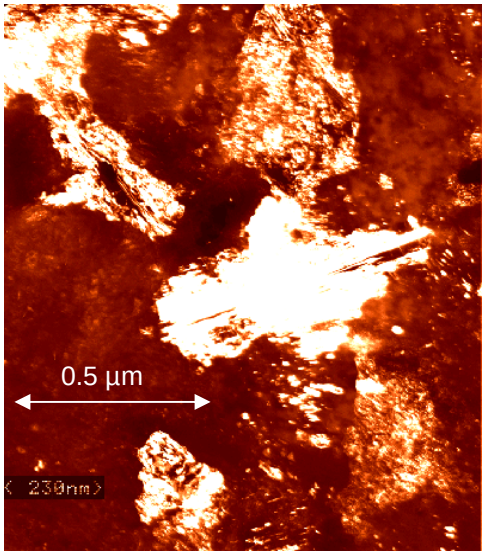

Figure 3. Dark field transmission electron micrograph of a 160 nm thick polycrystalline film made on a SOG/SiO_2 coated steel substrate by crystallization at 950°C/20 sec. The grain size is ~ 0.5 μm.

The smooth surface of furnace-crystallized polysilicon film on steel is shown by the atomic force micrographs of Figure 4. The AFM micrographs are taken at three different stages of the polysilicon-on-steel process: a) as-received steel foil substrate, b) after curing spin-on-glass and PECVD SiO_2, and c) with 160 nm polysilicon film crystallized at 950°C/20 sec. The polysilicon film has the lowest surface root mean square (RMS) roughness of 1.2 nm, compared with 2.2 nm of the insulation layer and 5.9 nm for the as-received steel foil.

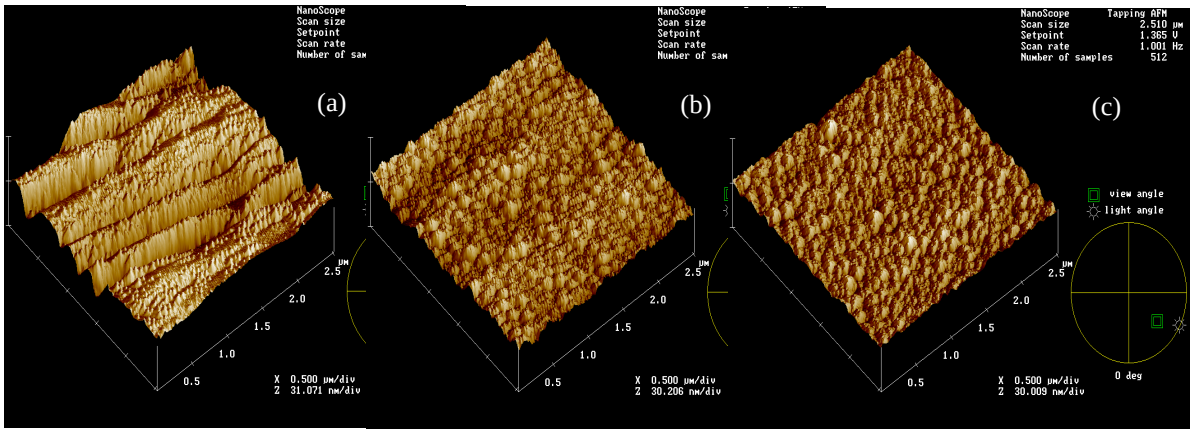

Figure 4. Atomic force micrographs of (a) as-rolled steel foil surface, (b) substrate surface after SiO_2/spin-on-glass planarization, and (c) surface of 950°C/20 sec polysilicon film on planarized substrate. Length of horizontal divison 0.5 μm, of vertical division 30 nm.

Polycrystalline silicon thin film transistor on steel

All transistors were made in the top-gate coplanar source/drain geometry. Initially a low-temperature device fabrication process (maximum T of 350°C) with deposited source and drain layers was used to gauge the quality of the polysilicon films directly after the recrystallization process. Once the high temperature capability of the polysilicon-on-steel had been ascertained, a self-aligned process with ion-implanted source and drain was used, requiring anneals over 600°C.

Low-temperature process with deposited source/drain. Initially, all post-crystallization processing was done with a maximum process temperature of 350°C, by a non-self-aligned process with channel W/L = 180μm/45μm. (Figure 5).

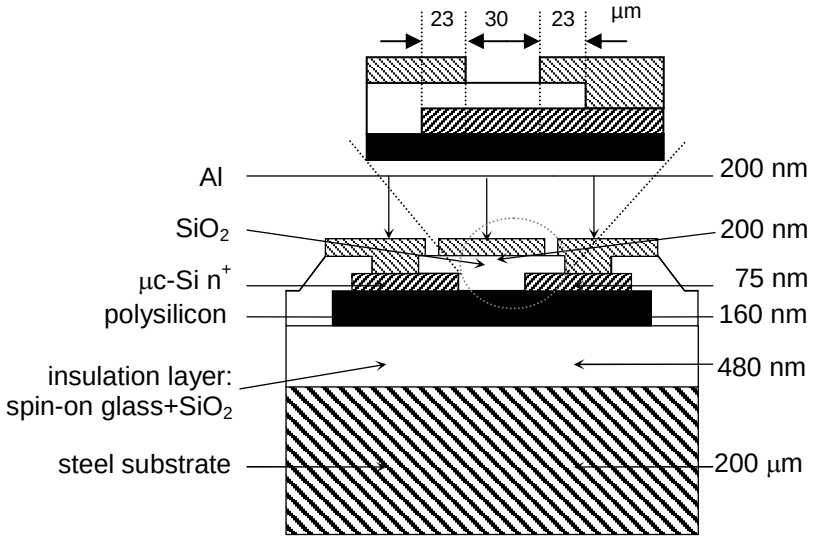

Figure 5. Schematic cross-section of a polysilicon top-gate transistor on a passivated steel substrate with deposited source/drain, showing detailed source/drain alignment.

Crystallization temperatures/times ranged from 600°C/6 hour to 950°C/20 sec. On top of the crystallized silicon layer, a 75-nm thick n^+ microcrystalline silicon (μc-Si:H) layer was deposited by PECVD at 350°C to serve as the eventual source/drain [31,32]. Then the original polysilicon layer was patterned into TFT islands by reactive ion etching (RIE), and the n^+ μc-Si:H layer was patterned by another RIE step. Next, a 200-nm thick gate oxide was deposited by PECVD at 250°C, followed by a wet etch to open the source/drain contact windows. 200-nm aluminum was thermally evaporated and then patterned by wet etch to form the gate and source/drain contacts. The final step in the TFT fabrication was a 15-min-long anneal at 250°C in forming gas (15 vol.% hydrogen – 85 vol.% nitrogen). This source/drain process is not practical for short-channel TFTs, which require low parasitic resistance, but it is sufficient for evaluating the carrier mobility in long channels.

Figure 6 shows the (a) transfer and (b) output characteristics of an n-channel transistor made from 650°C polysilicon. We calculated the threshold voltage V_{th} and the electron field effect mobility in the linear regime $\mu_{e,lin}$ from the linear plot of the drain current I_{DS} against gate source voltage V_{GS} at drain source voltage V_{DS} of 0.1 V. The average $\mu_{e,lin} = 63 \pm 11$ $cm^2 \cdot V^{-1}s^{-1}$ and $V_{th} = 7.2 \pm 1.8$ V. These averages of >10 devices include the standard deviation. The value of $\mu_{e,lin}$ lies among the highest of all transistors made from furnace-crystallized polysilicon [6]. The I_{DS} ON/OFF ratio (defined as the value of maximum I_{DS} to minimum I_{DS} with $V_{DS} = 10$ V with a V_{GS} range from – 10 V to 20 V) is ~10^6 over the entire range of 600°C to 950°C (Figure 7), a value comparable to those of the transistors made on glass with the same process [28]. This result suggests that TFT performance is not adversely affected by the high temperature annealing of silicon on metal substrates.

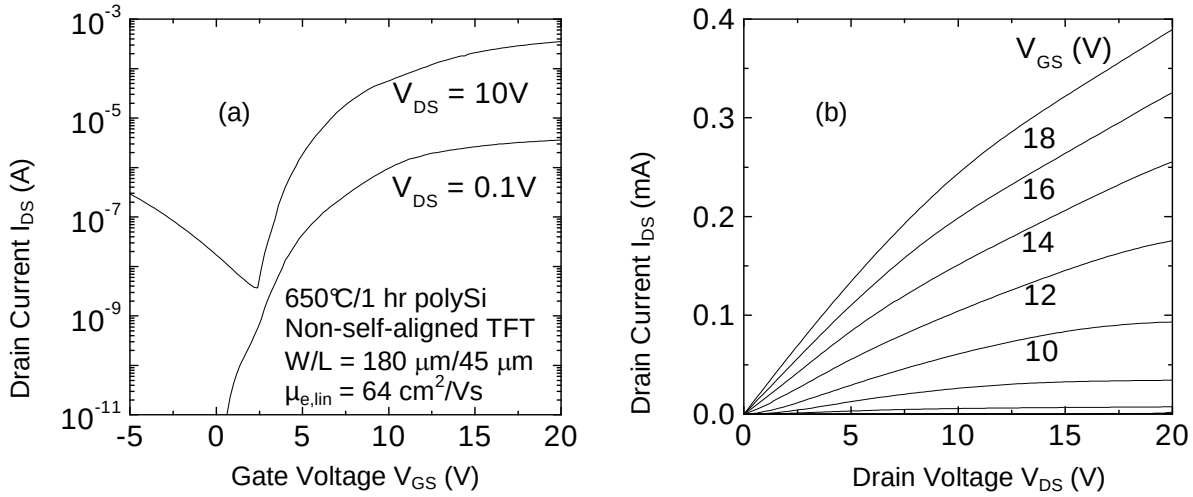

Figure 6. (a) Transfer and (b) output characteristics of a top-gate polysilicon TFT with deposited source/drain process. Polysilicon was made by crystallization at 650°C/1 hour on steel.

High-temperature process with ion-implanted source/drain. The precursor a-Si:H film was crystallized at 950°C for 20 sec or 20 min, and the active area defined by RIE (Figure 8). 150 nm gate SiO_2 was deposited by PECVD at 350°C. 200 nm intrinsic a-Si:H was deposited by PECVD at 270°C and then patterned by RIE to form the eventual gate. Then the SiO_2 layer was wet-etched to form the source and drain openings. For n-channel TFTs, the source and drain were implanted with phosphorus at 50 keV and a dose of $2x10^{15}$ cm^{-2}. The implant damage was annealed and the gate silicon was crystallized by a 30-minute furnace anneal at 750°C. Then the sample was immersed in a hydrogen glow discharge at 350°C for 1 hour. A 200-nm SiO_2 passivation layer was deposited by

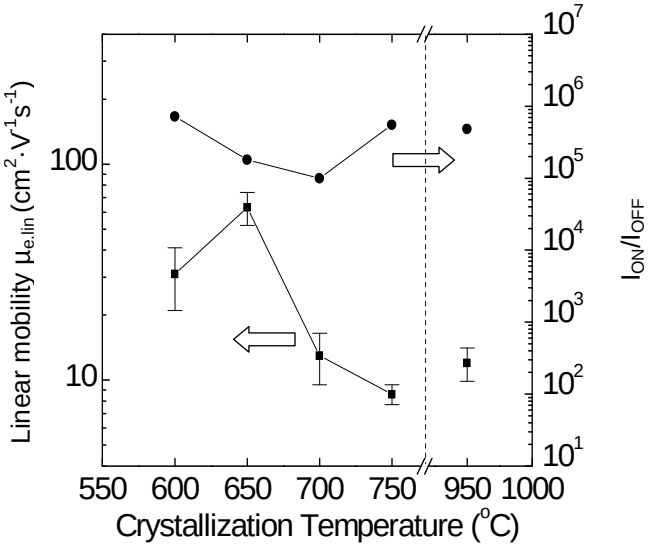

Figure 7. TFT performance vs. crystallization temperature for TFTs with deposited source/drain.

channel length by at most 0.25 µm. Figure 10 contains the plots of linear mobilities and OFF currents of n-channel TFTs made of two polysilicon films crystallized at: (a) 950°C/20 min and (b) 750°C/2 min, as functions of channel length. In Figure 9 (a), the linear mobility is ~30 $cm^2V^{-1}s^{-1}$ for channel length ranging from 2 µm to 50 µm, while in 9 (b), the linear mobility of TFTs with channel length < 3 µm is considerably better than for TFTs

PECVD at 250°C, and source/drain and gate contact windows were opened by wet etch of the passivation SiO_2. 300 nm Al was thermally evaporated and patterned to form the source/drain and gate electrodes. Finally, the TFTs were annealed in forming gas at 250°C for 15 minutes. The highest process temperature after crystallization was the 750°C post ion-implant anneal.

Self-aligned TFTs were made of polysilicon crystallized at 750°C/2 min, 950°C/20 sec, or 950°C/20 min, using 350°C gate oxide. Effective channel length measurements (done for 950°C/20 min annealing) showed that the effective channel length differed from the drawn

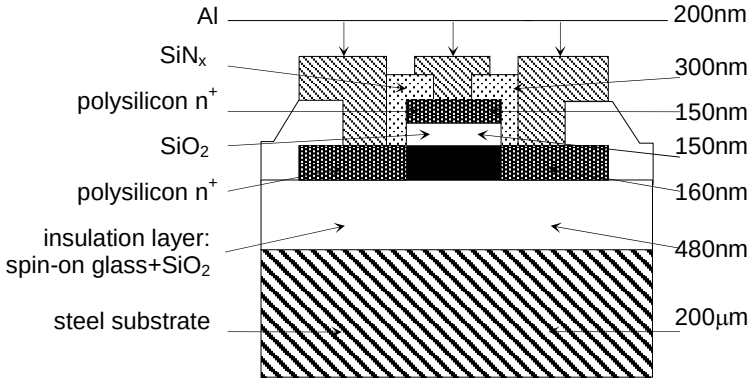

Figure 8. Schematic cross section of the self-aligned polysilicon thin film transistor on steel, with ion-implanted source/drain.

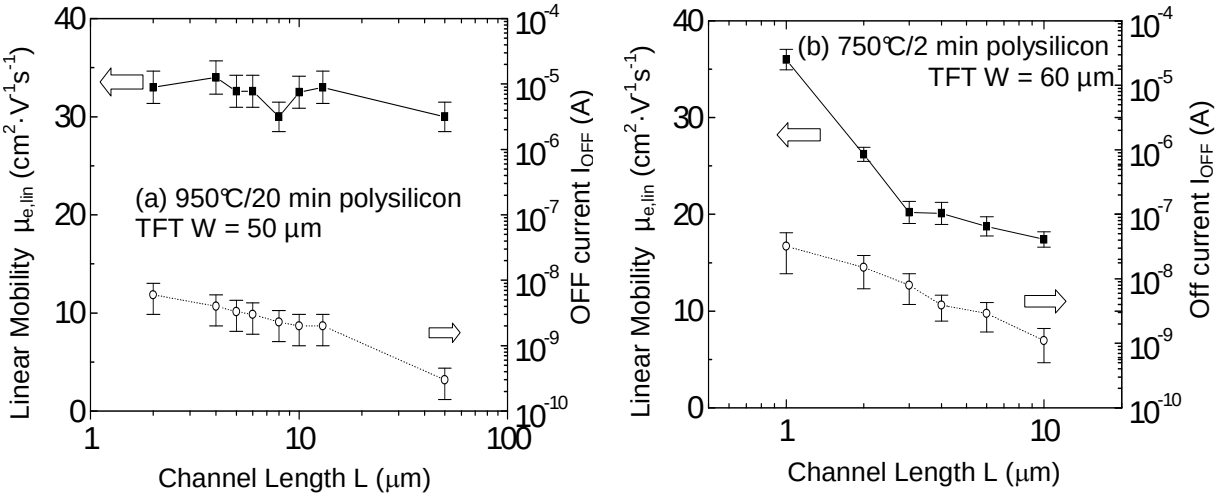

Figure 9. Linear mobilities and off currents of n-channel TFTs made of two polysilicon films crystallized at: (a) 950°C/20 min and (b) 750°C/2 min, as functions of channel length.

with longer channels. The mobility drops from 36 ± 1.1 $cm^2V^{-1}s^{-1}$ to 17 ± 0.8 $cm^2V^{-1}s^{-1}$ as channel length increases from 1 µm to 10 µm. This difference suggests that the grain size of the 950°C polysilicon is less than 2 µm, but the 750°C polysilicon film has a grain size of a few micrometers. The mobilities of 950°C TFTs are higher than those of 750°C TFTs. The OFF currents of the two batches of TFTs are of the same order, ~20 pA per µm of channel width for TFTs with 10-µm-long channels. The reciprocity of the OFF current to channel length in both cases indicates that the OFF current is set by the intrinsic conductivity of polysilicon film. Furthermore, the transistors made with 950°C/20 min crystallized polysilicon have the same OFF current as the transistors made from 950°C/20 second polysilicon. Excess metallic contamination (Fe, Cr) from steel would likely cause many midgap states and thus a large number of generation centers. Since longer annealing did not increase the leakage current, these data again suggest that metallic contamination does not affect the TFT performance.

The ability to crystallize device-grade films at 950°C suggested that the gate dielectric might be grown by the direct oxidation of the polysilicon films, instead of PECVD. Polysilicon formed by 950°C/20 sec crystallization was oxidized in flowing dry O_2 for 40 minutes at 950°C in a tube furnace to form gate oxide. The resulting oxide thickness is 51 nm as measured by a Dektak profiler and by ellipsometry on an oxidized reference lightly-doped silicon wafer. The transistors made with thermal oxide have a channel length of 5 µm and an average V_{th} = 8.5 ± 0.8 V, $\mu_{e,lin}$ = 27 ± 2.2 $cm^2V^{-1}s^{-1}$, and the OFF current I_{DS} is 35 ± 22 pA/µm of channel width at V_{DS} = 10V. Note that even after 40 minutes at 950°C during oxidation, the OFF current remains of the same order as that of the low-temperature TFTs, and of the self-aligned TFTs with 350°C deposited gate oxide.

CMOS polysilicon circuits on steel

To explore feasibility of polysilicon driver circuits on flexible substrates, CMOS polysilicon circuits were fabricated on steel with a 6-mask process (polysilicon island, gate, n^+ implant, p^+ implant, contact via, metal) and tested. The channel layer was 150-nm a-Si:H deposited by PECVD at 150°C and crystallized at 750°C/2 min. No active-layer implant was used. The process was the same as that used for self-aligned TFTs with the gate oxide deposited at 350°C. The n^+/p^+ source/drain (and gate doping) were implanted with phosphorus/boron at 50 keV/35 keV and a dose of $2x10^{15}$ $cm^{-2}/2x10^{15}$ cm^{-2}. The n^+/p^+ implant selection was made by masking drain/source individually with ~1 µm AZ5214 photoresist. Isolated n-channel TFTs made with this process have the same performance as described earlier. The hole mobility in the linear regime ranges from 19.1 ± 0.7 $cm^2V^{-1}s^{-1}$ to 13 ± 0.3 $cm^2V^{-1}s^{-1}$ in p-channel TFTs with channel length ranging from 1 µm to 50 µm.

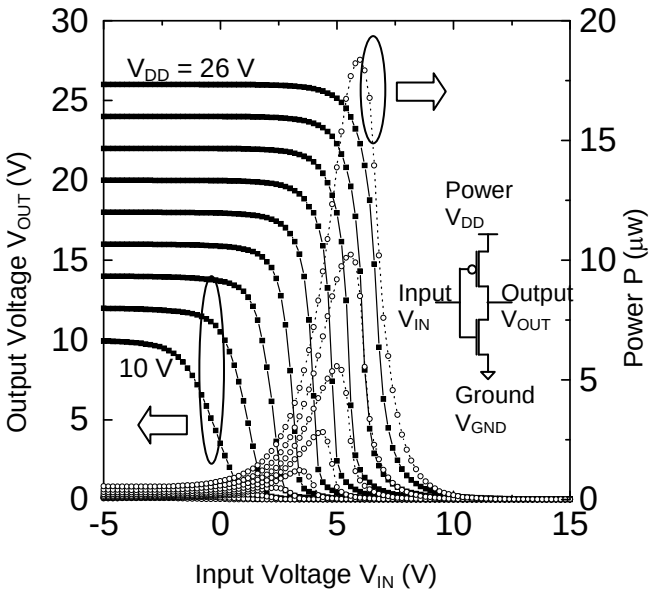

Figure 10. DC output characteristic of CMOS inverter made with polysilicon TFTs on steel with channel width W = 60 µm and length L = 6 µm.

Figure 10 shows the DC output and power characteristics of a CMOS inverter made from self-aligned polysilicon TFTs with L = 6 μm and W = 60 μm recrystallized at 750°C/2min and with 350°C PECVD gate oxide. This inverter has a full range swing from the power supply voltage V_{DD} to ground, and a small signal voltage gain K of ~25 at $V_{DD} \geq 20V$. The threshold voltage is not exactly half of V_{DD} due to the difference between the n- and p-channel TFT threshold voltages (8 V and – 20 V).

Figure 11 shows (a) the output of a 5-stage ring oscillator made with the CMOS polysilicon inverters with transistors of W/L = 60 μm / 4 μm at a supply voltage V_{DD} = 30 V, and (b) the oscillation amplitude and frequency vs. supply voltage. The oscillation frequency at V_{DD} = 30 V is ~ 1 MHz, corresponding to an average gate propagation delay of 100 ns, and the amplitude A_{osc} is 7.1 ± 0.9 V. The oscillation frequency rises when the power supply voltage V_{DD} is raised above 15 V, while the oscillation amplitude A_{osc} saturates at 7.1 ± 0.9 V.

The capacitance of the nodes of the ring oscillator has two dominant components: gate capacitance, estimated to be 0.11 pF for a gate oxide thickness of 150 nm, and capacitance between the metal lines and the substrate. With an insulator thickness of 480 nm and average metal area on each node of $7x10^3$ μm^2, the capacitance between the metal lines and steel substrate is 0.5 pF, which is larger than the gate capacitance. However, the overall speed is probably limited by the capacitance of the scope probe, which is ~13 pF. Thus the intrinsic circuit performance is probably higher than what we observed.

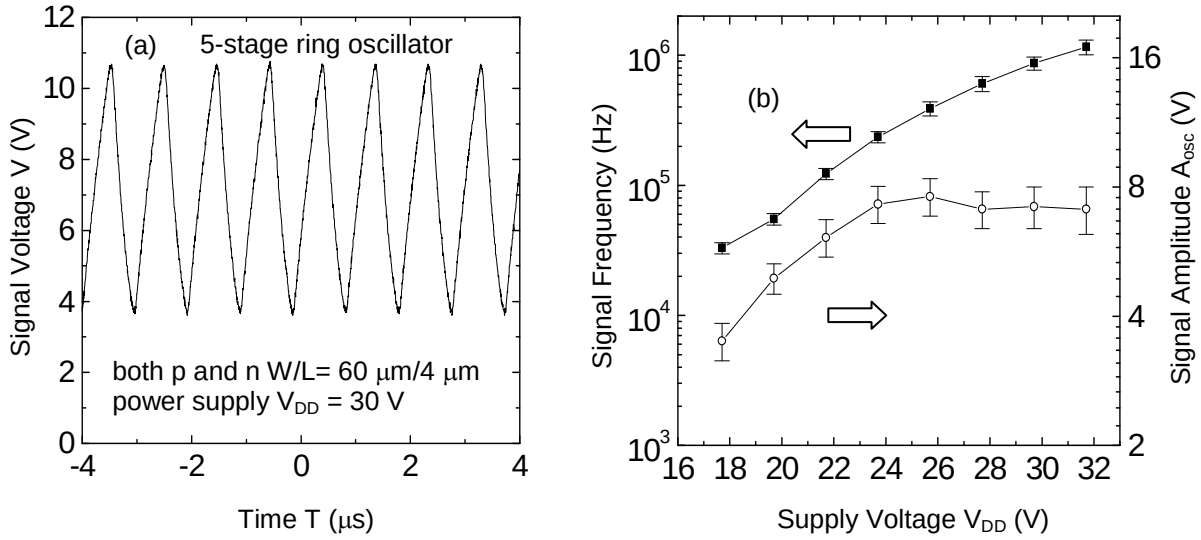

Figure 11. (a) Output signal of a 5-stage ring oscillator made with CMOS polysilicon inverters on steel. TFTs have channel width W = 60 μm and length L = 4 μm. (b) The oscillation amplitude and frequency vs. the power supply voltage.

Conclusion

Polycrystalline silicon on steel was formed by furnace crystallization of amorphous silicon at temperatures ranging from 600°C to 950°C on SiO_2 coated steel substrates. Due to their tolerance of high process temperatures, steel substrates enable much shorter crystallization times than glass substrates, and are tolerant of conventional high temperature silicon processing methods. Thin film transistors and CMOS circuits were fabricated with these polysilicon films on steel. The polysilicon TFT performance shows no evidence of contamination from the steel substrate. Ring oscillators with gate delay of ~0.1 μs were demonstrated. These complementary polysilicon thin film

transistor circuits on steel foil demonstrate a new route to large-area, flexible TFT backplanes, with the performance required for driver and matrix circuits of displays, sensor arrays, and mechatronic materials.

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