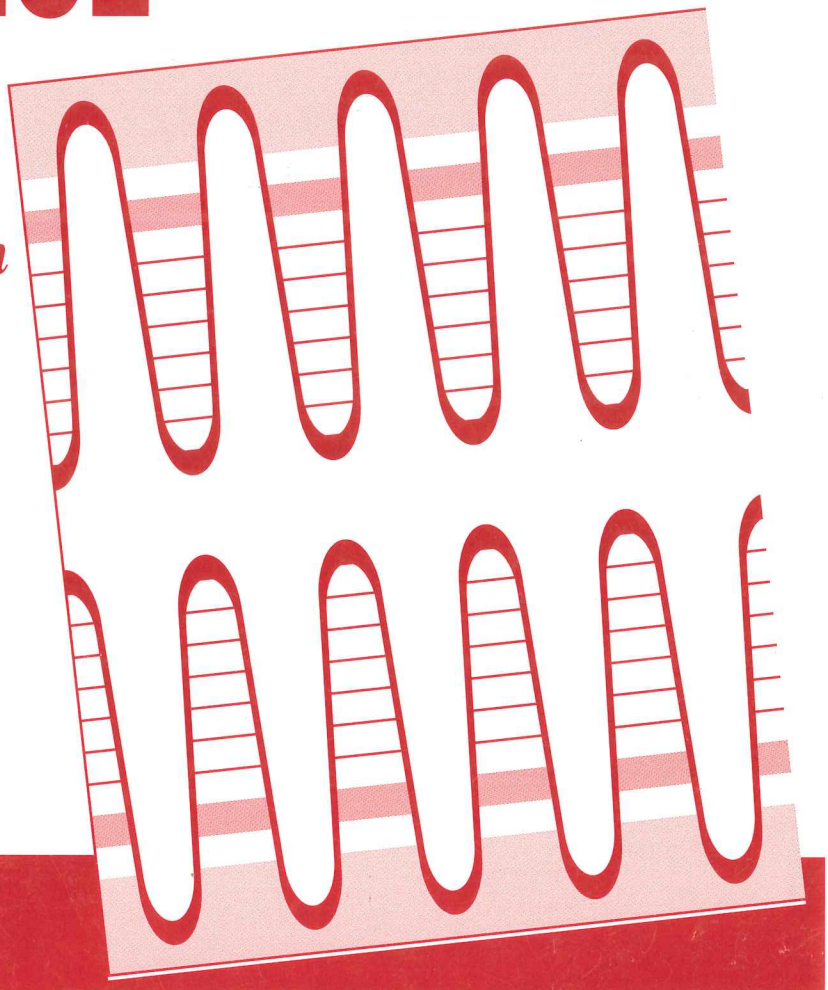
Jim Stark

44th

2002 ELECTRONIC MATERIALS CONFERENCE

Featuring...
The Electronic Materials Exhibition



University of California

Santa Barbara, California

June 26–28, 2002

TMS

Technical Program with Abstracts

active region of a device by many orders of magnitude. This technique has now been applied to bipolar devices. The device design is similar to a conventional bipolar design, with InSb used for all layers except for the emitter, which is made from $Al_{0.05}In_{0.95}Sb$ and provides a valence band barrier at the emitter-base junction. The base is highly p-type doped, but at present does not contain the p++ implant that will provide the full carrier extraction benefit. However the base can still be reverse-biased to extract carriers from (mainly) the low-doped collector region. The emitter size is 6 μm x 25 μm, and the collector size 22 μm x 25 μm. The resulting device shows low voltage output characteristics, with drain voltages up to 0.6 V and base voltages up to 0.25 V (0.05 V steps). The two lowest lines on the output characteristic are with a negative bias applied to the base, showing how the carrier extraction technique reduces leakage and suppresses breakdown (in fact at negative base voltages the device shows a breakdown voltage of over 1.2 V). The device also shows excellent transconductance, as shown in the characteristic above, limited at higher current by series resistance in the device, which needs optimising. The base-emitter diode shows a reverse current, even at positive base voltages, due to the removal of the thermally generated carriers from the device, and passes through zero current at Vbe = 0.25 V. Because of this, the differential current gain is very large (hence the output characteristic above is shown with base voltage as the parameter). AC measurements on these 6 μm emitter devices are very promising, showing an fT of over 25 GHz in a device not optimised for high speed performance. Modelling shows that addition of a p++ implanted base contact results in a factor of eight reduction in leakage current. It also shifts the base-emitter turn-on voltage down towards zero. Scaling of the device leads to a predicted fT of over 600 GHz for devices with 1 μm emitters.

Session E: Materials Integration: Wafer Bonding and Alternative Substrates - I

Wednesday AM — Room: UCEN Flying A
June 26, 2002 — Location: University of California

Session Chairs: Peter Moran, Michigan Technological University, 1400 Townsend Dr., Houghton, MI 19931 USA; Matt Seaford, RF Microdevices, 7628 Thorndike Ln., Greensboro, NC 27409 USA

10:00 AM

E1, Testing the Feasibility of Strain Relaxed Compliant Substrates: *M. Kostrzewa*[1]; G. Grenet[1]; P. Regreny[1]; J. L. Leclercq[1]; F. Bessueille[1]; N. Mokni[2]; A. Danescu[2]; F. Sidoroff[2]; G. Hollinger[1]; [1]Ecole Centrale de Lyon, LEOM, UMR CNRS 5512, Ecully 69134 France; [2]Ecole Centrale de Lyon, LTDS, UMR CNRS 5513, Ecully 69134 France

To prepare compliant substrates, the most evident approach is to insert a viscous layer in between the thin seed film and the host substrate. Several technological problems have to be solved before actually evidencing the compliant phenomenon itself. First, a sticking material has to be found. It has to be viscous at growth temperatures, compatible with epitaxial processes and appropriate to successfully bond a thin semiconductor layer on a host substrate. Second, the surface quality of the thin seed layer after all the technological steps has to be good enough to allow high quality epitaxial regrowth. Low viscosity borophosphorosilicate glass films has been used by several groups. They found that the strain relaxation is accompanied by a buckling which can be eliminated only by patterning the strained films into small areas. In order to learn more about this particular relaxation mechanism (and especially how it could affect the seed film lateral dimensions), we have studied the way an ultrathin epitaxial $In_{0.65}Ga_{0.35}As$ layer elastically relax when stuck on InP or Si substrate using a thick wax layer (with a very low viscosity at room temperature). By freeing the study from difficulties inherent to a real epitaxial overgrowth (high-vacuum, high-temperature) this approach has allowed us direct and time-monitored morphological observations at room-temperature. Moreover, we have performed what can be seen as the reverse process of an epitaxial growth, i.e., the chemical etching of the initial InP substrate. The experimental results clearly show how a mesa relax both by gliding its edges and by buckling its central area. The competition between these two relaxation processes is discussed via recently published theoretical backgrounds. Finally, we will discuss what can be issued from this theoretical-to-experiment confrontation in terms of compliance understanding and feasibility.

10:20 AM Student

E2, High Ge-Content Relaxed $Si_{1-x}Ge_x$ Layers by Relaxation on Compliant Substrate with Controlled Oxidation: *Haizhou Yin*[1]; Karl D. Hobart[2]; Rui Huang[3]; Jim Liang[3]; Zhigang Suo[3]; Sean R. Shieh[4]; Thomas S. Duffy[4]; James C. Sturm[5]; [1]Princeton University, Electl. Eng., Princeton, NJ 08544 USA; [2]Naval Research Laboratory, Washington, DC 20357 USA; [3]Princeton University, Princeton Matls. Inst. & Dept. of Mechl. & Aeros. Eng., Princeton, NJ 08544 USA; [4]Princeton University, Dept. of Geoscis., Princeton, NJ 08544 USA; [5]Princeton University, Ctr. for Photonics & Optoelect. Matls. & Dept. of Electl. Eng., Princeton, NJ 08544 USA

There has been increasing interest in compliant substrates for integration of heterogeneous epitaxial materials. In this talk, borophosphorosilicate glass (BPSG) on silicon is used as a compliant substrate to allow the relaxation of strained SiGe islands, a process which can allow relaxed layers to be obtained without the formation of misfit dislocation observed in graded SiGe buffers. Previous work has shown that relaxed SiGe on Si by this method is limited to small islands (less than 30micron) and low Ge fraction (less than 30%), with the buckling of the compressive SiGe layers as a fundamental limit. In this paper, we describe two key improvements to allow 200micron islands with up to 65% Ge to be relaxed: (i) oxidation of the SiGe layers to increase the Ge fraction, and (ii) the use of a deposited oxide to prevent buckling and control the oxidation rate. A wafer of 30nm-strained-$Si_{0.7}Ge_{0.3}$/25nm-Si/200nm-BPSG/Si was fabricated by bonding and "Smart-cut" as in ref. 1. SiGe islands of sizes 10-500micron were then patterned. Long anneals at 875°C were carried out to achieve intermixing of Ge and relaxation of the islands, which yielded relaxed 55nm-thick $Si_{0.84}Ge_{0.16}$ islands. Raman spectroscopy was used to independently determine both the Ge content and strain status of SiGe islands. This sample was oxidized from 800°C to 900°C to raise Ge content due to preferential thermal oxidation of Si atoms in the alloys. Two problems emerged during the oxidation process: (1) Surfaces of islands buckled due to the strain increase from higher Ge content and the island thinning; (2) the uniformity of Ge content across islands was poor, because the surface Ge content of islands is believed to determine the interface oxidation reaction and it is difficult to control the surface condition as Ge snowplows into the alloy during oxidation. A layer of PECVD oxide on the top was used to solve these problems. It effectively increases the island thickness, making them stiffer and consequently less prone to buckling. Furthermore, effect of the SiGe surface on oxidation is removed, because the oxidation process is now largely limited by the diffusion of oxidant through the top oxide. The oxidation rate can be well controlled by the thickness of the oxide layer. Without this capping layer, a lateral lattice constant larger than that of a relaxed $Si_{0.7}Ge_{0.3}$ on 200μm islands could not be achieved due to buckling and oxidation rate variations. However, with the capping process, uniform 200μm islands with fully relaxed $Si_{0.4}Ge_{0.6}$ were achieved. In smaller fully relaxed islands Ge content over 70% has been achieved. This is far higher than the effective Ge substrate content (i.e. the in-plane lattice constant of a relaxed layer) of $Si_{0.73}Ge_{0.27}$ previously reported using the oxidation technique. This work is supported by DARPA and ARO.

10:40 AM

E3, Strain Relaxation in Wafer-Bonded SiGe/Si Heterostructures Due to Viscous Flow of an Underlying Borosilicate Glass: *Peter Morán*[1]; K. D. Hobart[2]; [1]Michigan Technological University, Matls. Sci. Dept., 409 MME Bldg., Houghton, MI 49931 USA; [2]Naval Research Laboratory, 4555 Overlook SW, Washington, DC 20375 USA

We report a high-resolution x-ray diffraction (HRXRD) study of relaxation in a strained semiconductor heterostructure removed from its native substrate, bonded to a glass substrate, and subsequently heated. The data is consistent with the type of relaxation that would result from viscous flow of the underlying glass. It is not consistent with the type of relaxation that would result from an enhancement in misfit dislocation nucleation and/or threading dislocation glide due to a sub-surface bonded