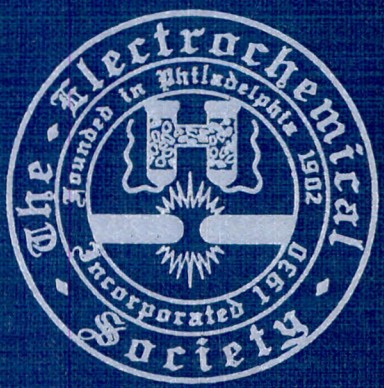
ULSI PROCESS INTEGRATION II



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Proceedings of the International Symposium

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PREFACE

The first international Symposium on ULSI Process was initially organized in Honolulu, Hawaii in 1999. The following Proceedings Volume contains papers that were presented at the second international symposium on ULSI Process Integration, held in Washington D.C. on March 24-31, 2001 as part of the 199th Meeting of the Electrochemical Society. The symposium was well rounded with a collection of 52 papers within 56 presentations. The presentations of the enclosed papers were scheduled Monday through Thursday which covered the entire length of the conference with a wide range of process integration and IC device applications.

The main focus of the ULSI Process Integration symposium was to provide an international forum on topics related to the interrelationships and interactions between multi-process steps. The unit process applications are taken a step further by considering the overall effects to the whole applied process. The single process steps were studied in the context of the formation of an electrical device. The program focused on recent innovations in ULSI scaling of devices, on transistor process technology, on defect impacts on process integration and on novel processes.

The ULSI Process Integration Symposium was sponsored by the Electronics Division of the Electrochemical Society and by the Electron Devices Society of the IEEE. The symposium was international in scope and included authors Belgium, France, Germany, India, Japan, Korea, Singapore and United States. This proceedings contains 52 papers, including 5 keynote speakers, 28 invited speakers and 19 contributing speakers. The symposium consisted of seven sections focusing on ***Process Integration and Device Scaling***, ***Process Integration and Device Performance***, ***Process Integration of Si-Ge Technologies***, ***FEOL Process Integration of Transistor Devices***, ***Process Integration and Defect Interactions***, ***Process Integration in Circuit Applications***, ***Substrate Integration Using SOI***, and ***FEOL Process Integration and Unit Processes***.

The Process Integration function has been a crucial engineering activity to the semiconductor development. Process Integration has used many unit process within a multi-process sequence to make them function properly within the ULSI electrical device. The process and device scaling highlighted in the keynote address by Dr. Iwai outlined the future problems in scaling below 100 nm feature size. He cited the process integration of some new materials and some novel devices that are needed to enable the ULSI devices below the sub 100 nm level. In the Full process integration section, Dr. Ishitani discussed the role of different photolithography techniques that would be useful in the 0.1um devices. The FEOL process integration section focused primarily on the gate stack and transistor integration like Dr. Huff's key note presentation that gave an excellent picture of the issues in the gate stack formation. The talk on "Silicon Germanium Trends on Process Integration" by Dr. Kasper summarized the roadmap of the SiGe development. The role of defects in integration from silicon metals to dislocations were highlighted by the section on Defects and Process Integration. Substrate Integration emphasis was focused on SOI tpoics. Finally, unit process development that may represent good concepts for future process integration were reviewed in the last section.

The **DIELECTRIC SCIENCE AND TECHNOLOGY DIVISION T.D. CALLINAN AWARD ADDRESS** on the "Evolution of the Metallization Concepts for Applications in the Integrated Circuits" was given by S.P. Murarka from Rensselaer Polytechnic Institute and is included in the Proceedings.

The organizers would like to thank the members of the technical program committee and all the authors for the on-time submission of their manuscripts. The invited speakers are acknowledged for making this symposium possible by sharing their perspectives and insights and by putting considerable effort in the preparation of the camera-ready manuscripts. We want to acknowledge the contribution of the Session chairmen in chairing the sessions. We also thank the staff of the Electrochemical Society for their support.

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THRESHOLD VOLTAGE STABILITY OF P-CHANNEL MOSFETS WITH HEAVILY BORON DOPED SIGEC GATE LAYERS

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P-channel MOSFETs with thin gate oxides are susceptible to undesirable positive threshold voltage shifts during post implant anneals due to boron penetration through the gate oxide and into the substrate. In this paper, we report p-channel MOSFETs with boron-doped polycrystalline SiGeC gate layers that show substantially reduced boron penetration and increased threshold voltage stability compared to devices with either Si or SiGe gates. Boron segregates into the SiGeC layers, allowing less boron into the gate oxide and substrate. Separate test structures demonstrate that boron segregates to SiGeC layers with high carbon concentration, indicating the effectiveness of SiGeC layers at suppressing penetration increases with carbon content. Electrical measurements indicate the boron remains electrically active.

INTRODUCTION

P-channel MOSFETs with very thin gate oxides and heavily boron-doped gates are susceptible to boron penetration through the gate oxide during post-implant anneals, resulting in undesirable positive threshold voltage shifts (1). This effect has been shown to be significantly increased by the presence of flourine introduced during a BF_2^+ implant (2). Previously, it was shown that the use of polycrystalline SiGeC gate layers in PMOS capacitors greatly reduced boron penetration compared to devices with Si or SiGe gates (3). In this paper, we report self-aligned-gate p-channel MOSFETS with boron doped SiGeC gate layers, with greatly reduced boron penetration and increased threshold voltage stability compared to devices with either all poly silicon gates or with poly SiGe gate layers. Boron preferentially segregates into the polycrystalline SiGeC layers compared to Si layers, allowing less boron to penetrate into the oxide and substrate, and giving a high boron level at the gate-oxide interface for low gate depletion.

MOSFET CHARACTERISTICS

Two sets of p-channel MOSFETs were fabricated to investigate the effectiveness of polycrystalline SiGeC gate layers in suppressing boron penetration. The first set (set A) had in-situ doped (as deposited) gates with either polycrystalline Si or SiGeC throughout the entire gate. For these devices, ~8nm gate oxides were first grown on n-type substrates. Poly gate deposition was then performed by RTCVD at 625^0C and 700^0C, using SiH_4, GeH_4, $SiCH_6$, and B_2H_6 as silicon, germanium, carbon, and boron sources, respectively. The entire gate was either boron doped (~$1x10^{21}$ cm^3) poly Si or poly SiGeC (20% Ge, 0.6% C), for a total gate thickness of ~150 nm (Fig. 1). Following

deposition, gates were patterned into ring structures to allow for device isolation. Gate, source, and drain for all samples were then simultaneously implanted with $2x10^{15}$ cm^{-2} BF_2^+ at 50 keV and annealed at 900^0C in N_2 for 20, 50, or 80 minutes to allow boron activation and diffusion, followed by metal deposition and patterning.

Devices with SiGeC gates have dramatically reduced boron penetration and increased threshold stability compared to devices with all Si gates. Figure 2 shows threshold voltage vs. anneal time for these devices. Both devices experience positive threshold voltage shifts with increasing anneal time, indicating boron penetration into the substrate. However, after 20 and 50 minutes of annealing, the Si gates have threshold voltages of 1.8 V and 5.3 V, respectively, whereas the SiGeC gate threshold voltages remain at 0.0 V and 0.3 V. Furthermore, the Si-gate 50 minute annealed device cannot be fully turned off, indicating enough boron has entered the substrate to prevent it from being fully depleted out. The SiGeC gates, however, for up to 80 minutes of annealing, maintain constant on/off currents and only shift to V_T=0.8 V (Fig. 3). Effective mobilities in the SiGeC gates are actually higher than those in the Si gates, indicating no big performance loss due to gate depletion in the SiGeC devices.

These devices, however, possess boron levels in the gate larger than what is commonly used in modern CMOS structures. Therefore, a second set of devices (set B) were fabricated, whose gates were deposited undoped and then subsequently doped only from the source/drain implant. Also, these structures have only a thin layer of SiGeC at the gate-oxide interface to act as a barrier, with most of the gate still poly Si (Fig. 4). A sample containing only a thin layer of SiGe was also included. For these devices, ~500 nm field oxides were first grown and patterned on n-type substrates (~1 x 10^{15} cm^3), followed by ~ 7nm gate oxidation in dry O_2 at 900^0C. Gates were then deposited by RTCVD under conditions described above. The first 60nm of each gate was either poly SiGeC (12% Ge, 0.35% C), poly SiGe, or poly Si; the remainder in all samples was poly Si, with a total gate thickness of ~500nm (all layers undoped initially). Gate, source, and drain for all samples were then simultaneously implanted with $2x10^{15}$ cm^{-2} BF_2^+ at 60 keV and annealed at 900^0C in N_2 for 20, 60, or 100 minutes, followed by a standard backend process.

Again, devices with SiGeC gate layers show substantially increased threshold voltage stability (Fig. 5). After 100 minutes of annealing, devices with Si and SiGe gate layers shift by 4.2 V and 3.2 V, respectively, whereas devices with SiGeC gate layers shift only 1.8 V. Furthermore, subthreshold current plots (not shown) reveal that for the 100 min anneal time, the Si and SiGe devices cannot be fully turned off, indicating that again enough boron has entered the substrate that it cannot be fully depleted. SiGeC gated devices, however, maintain similar on/off currents for the 100 min anneal as for the shorter anneal times. Smaller threshold voltages shifts (for similar anneal times) in the Si devices in set B compared to set A are perhaps due to the smaller level of boron doping in the gate compared to the set A devices. However, compared to the Si gates in each set, the SiGeC gates in set A actually appear more effective at suppressing boron penetration than the SiGeC devices in set B. This is most likely due to the higher carbon concentration in the set A devices (0.6% vs 0.35%), as described below.

DISCUSSION

To probe what causes the suppressed boron penetration in the SiGeC gates, a separate test structure was grown consisting of alternating ~60nm layers of in-situ boron doped ($\sim 10^{20}$ cm^{-3}) poly Si and poly SiGeC. Carbon concentrations in the SiGeC layers varied from 0 to 1%. This structure was annealed in N_2 at 800^0C for 18 hours, and SIMS profiles of boron concentration vs. depth were obtained before and after the anneal (Fig. 6). The as-grown profile shows that before the anneal, boron levels are about twice as high in the SiGeC layers than in the surrounding Si. After the anneal, the SiGeC layers with 0.5% and 1% carbon see an increase in boron level (with respect to the Si regions on either side), showing clear segregation to the these layers. Defining m as the ratio of the peak boron concentration in the SiGeC layer to the valley concentration in the surrounding Si, we obtain m=4.3 for the 1% layer and m=2.8 for the 0.5% layer (see table in figure 6). This indicates that segregation depends on the carbon concentration, increasing in layers with more carbon. Since SiGeC layers with higher carbon concentration accumulate boron more effectively, then in a MOSFET gate this should have the effect of allowing less boron out of the SiGeC gate layer and into the gate oxide and substrate.

Previously, weak segregation of boron to single crystal SiGe vs. Si has been reported (4). Major driving forces that have been given are first, the effect of the smaller boron atoms to reduce strain in compressively strained SiGe layers, and second, bandgap effects due to the different bandgap of SiGe vs. Si (5). For both of these cases, however, less segregation would be expected into SiGeC layers since carbon lowers the strain of strained SiGe layers and drives the bandgap towards that of Si (6,7,8). This is contrary to what is observed. The mechanism driving the segregation to polycrystalline SiGeC layers is under further study; however, it appears that boron remains electrically active in the layers. Sheet resistance measurements of the gates for the set A devices show that the boron remains electrically active during 900^0C anneals up to 5 hours. This suggests that large amounts of boron are not becoming deactivated through the formation of carbon related defect complexes.

CONCLUSIONS

Poly SiGeC gate layers are effective at suppressing boron penetration in p-channel MOSFETs. Boron preferentially segregates to the SiGeC layers in the gate, allowing less boron into the gate oxide and substrate during anneals. Since SiGeC layers with higher carbon concentration have a stronger ability to accumulate boron and suppress penetration, gate layers with higher carbon concentrations should show even higher threshold voltage stability.

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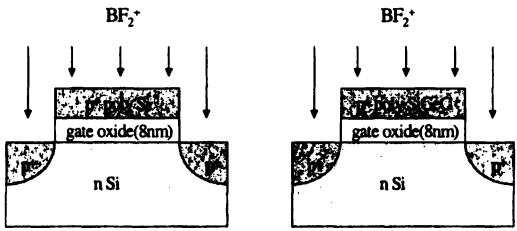


Figure 1: Gate structures for set A devices. In-situ B doping was ~$1x10^{21}$ cm^{-3} for both structures. For SiGeC gates, Ge and C concentrations were 20% and 0.6%, respectively.

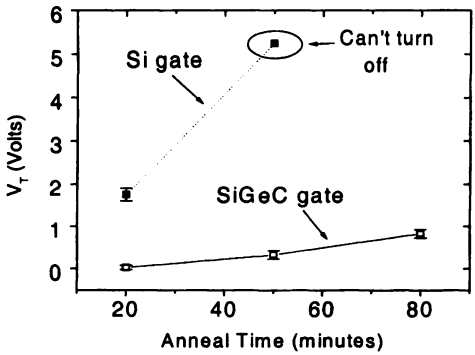


Figure 2: V_T vs anneal time for set A devices. For the Si gate 50 min device, V_T was defined by the shift in current characteristic at -40uA, since these devices could not be turned off. No FET characteristics were obtained for the Si gate 80 min device.

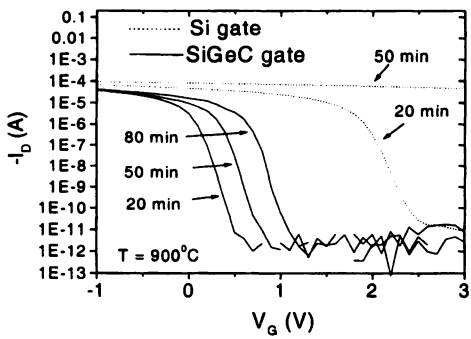


Figure 3: Subthreshold current plots for set A devices. V_D=-0.1V.

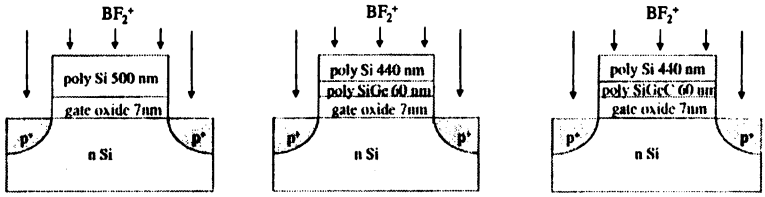


Figure 4: Gate structures for set B devices. Ge and C concentrations were 12% and 0.35%, respectively.

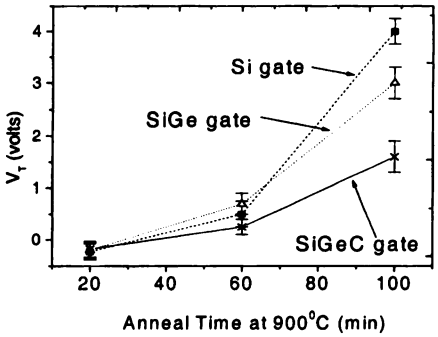
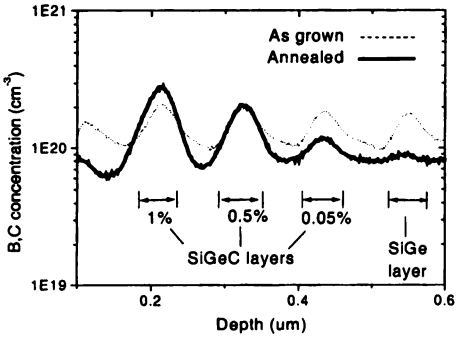


Figure 5: V_T vs. anneal time for set B devices. For Si and SiGe devices after the 100 minute anneal, V_T was defined by the shift in current characteristic at -100 uA, since these devices could not be turned off.



Carbon level	[B]SiGeC peak / [B]Si valley		Boron increase?
	as grown	annealed	
0%	1.8	1.2	No
0.05%	1.9	1.5	No
0.5%	2.0	2.8	Yes
1.0%	2.1	4.3	Yes

Fig. 6: Boron profiles in Si/SiGeC/Si sandwich structure (SiGeC layers preferentially doped as-grown), showing segregation of boron to SiGeC (after 800°C 18 hr N_2 anneal) for high carbon levels.