J. C. Sturm

43rd

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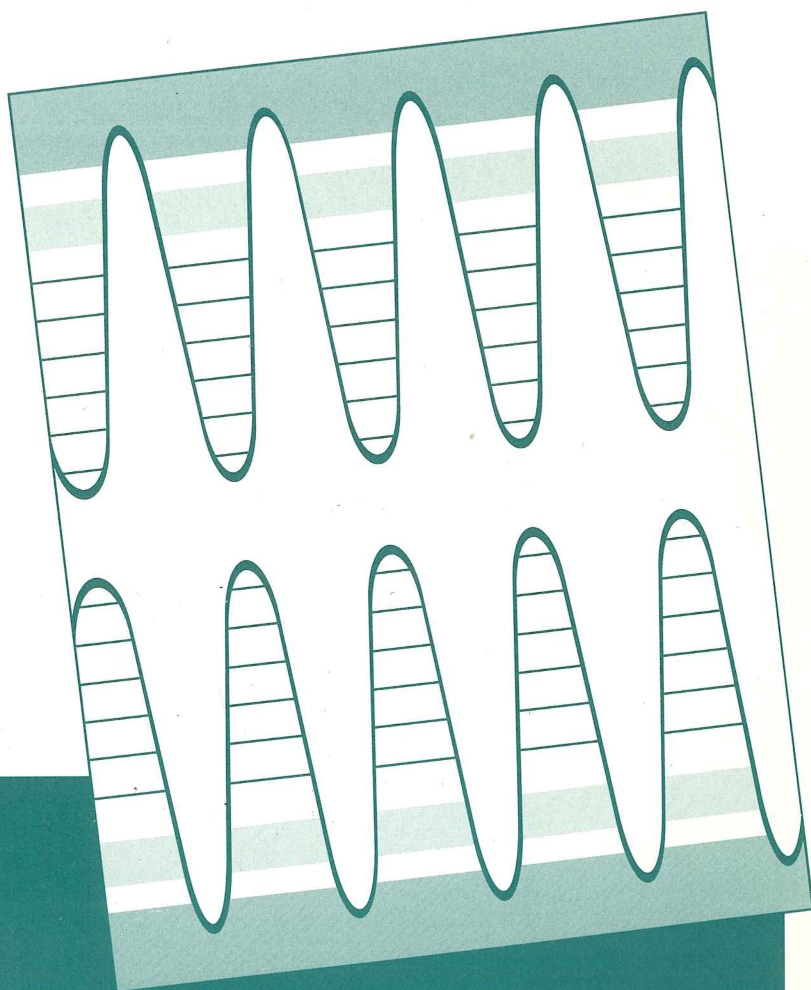

University of Notre Dame

Notre Dame, Indiana

June 27-29, 2001

TMS

Technical Program with Abstracts

related 1.6 eV feature associated with the outer GaN cap layer increases with increasing Ga concentration. The density of 2.34 eV AlGaN deep levels increases as interdiffusion increases at the interior AlGaN/GaN interface with decreasing R (e.g., < 5 nm to >13 nm) as measured by 500 eV Ar+ AES depth profiling. Ga and O interdiffusion (~100 nm) at the GaN/Al_2O_3 junction also varies with R. We believe these radial variations to be due to increasing temperature with decreasing R. The spatial distributions of defects suggest that: (a) the 2.34 and 2.18 eV defects are related to Ga vacancies[2,3] or their complexes, (b) that the <1.6 eV defect at the GaN surface is related to Ga interstitials[4] or their complexes. In principle, these correlations can identify and further minimize defect formation in device fabrication of nanoscale nitride thin film structures.
[1]S. T. Bradley, G. H. Jessen, L. J. Brillson, M. J. Murphy, and W. J. Schaff, J. Electron. Mater., in press; [2]J. Neugebauer and C. G. Van de Walle, Appl. Phys. Lett. 69, 503 (1997); [3]E. J. Tarsa, B. Heying, X. Hwu, P. Fini, S. P. DenBaars, and J. S. Speck, J. Appl. Phys. 82, 5472 (1997); [4]P. Boguslawski, E. L. Briggs, and J. Bernholc, Phys. Rev. B51, 17255 (1995).

11:20 AM, R9, Late News

Session S: Si-Based Heterojunction Growth and Characterization

Thursday AM June 28, 2001 — Room: 138 — Location: University of Notre Dame

Session Chair: Eugene Fitzgerald, Massachusetts Institute of Technology, Dept. of Matl. Sci. & Eng., Cambridge, MA 02139 USA

8:20 AM (Student)

S1, Investigating Hole Mobility Enhancements in Surface Strained Si/SiGe Heterostructures: *Christopher W. Leitz*[1]; Matthew T. Currie[1]; Eugene A. Fitzgerald[2]; Dimitri A. Antoniadis[3]; [1]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 77 Massachusetts Ave., Rm. 13-4150, Cambridge, MA 02139 USA; [2]Massachusetts Institute of Technology, Dept. of Matls. Sci. & Eng., 77 Massachusetts Ave., Rm. 13-5153, Cambridge, MA 02139 USA; [3]Massachusetts Institute of Technology, Dept. of Electl. Eng. & Comp. Sci., 77 Massachusetts Ave., Rm. 39-415B, Cambridge, MA 02139 USA

Surface channel strained Si devices fabricated on relaxed SiGe virtual substrates exhibit enhanced electron and hole mobilities, making them attractive candidates for SiGe-based CMOS applications. While electron mobility enhancements in surface strained Si/SiGe have been well-documented, hole mobility in these heterostructures has not been thoroughly explored. In this study, we investigate the dependence of hole mobility in strained Si/SiGe MOSFETs on substrate Ge content and strained layer thickness. We also explore methods of increasing hole mobility beyond that of strained Si while retaining the high quality Si/SiO_2 interface. In these experiments, MOSFETs are fabricated by a novel short flow process utilizing a deposited gate dielectric and only one lithography step. This type of device allows us to measure effective mobility at vertical fields approaching 1 MV/cm, thereby enabling us to quickly explore the impact of materials parameters on channel mobility at fields approaching those of state-of-the-art MOSFETs. We show for the first time that hole mobility enhancements saturate at virtual substrate compositions of 40% Ge and above, with mobility enhancements over twice that of co-processed bulk Si devices at vertical fields up to 7 x 10^5 V/cm. Peak mobility enhancements are demonstrated on devices fabricated on 40% Ge virtual substrates while mobility enhancements drop slightly at higher virtual substrate Ge contents, indicating that misfit dislocations degrade hole mobility at these mismatch levels. Furthermore, we demonstrate that hole mobility in strained $Si/Si_{0.7}Ge_{0.3}$ heterostructures displays no strong dependence on strained layer thickness, and preliminary measurements indicate that alloy scattering in surface channel MOSFETs does not greatly degrade hole mobility. Based on these results, we have explored alternative heterostructures aimed at attaining maximum electron and hole mobility enhancements while maintaining thermodynamically stable channel thicknesses and the high quality Si/SiO_2 interface. These devices offer the promise of symmetric electron and hole mobilities, which would enable greater flexibility in circuit design. We show that such heterostructures have peak effective hole mobilities of over 300 cm^2/V-s, and hole mobility enhancements of 2.2 are maintained at fields up to 8 x 10^5 V/cm. These results show promise for realizing optimized heterostructures for SiGe-based CMOS applications.

8:40 AM

S2, Growth and Stabilization of Sub 100-nm Vertical n-Channel MOSFET's: *John Edward Gray*[1]; M. Yang[2]; H. Yin[1]; J. C. Sturm[1]; [1]Princeton University, Electl. Eng., J-423, Equad, Olden St., Princeton, NJ 08544 USA; [2]IBM Microelectronics, Hopewell Junction, NY, USA

Vertical MOSFETs (VFETs) are a promising alternative to their conventional surface-channel counterparts, because of their potential ability to scale to short channel lengths and potential high packing densities. One approach towards constructing such devices involves defining the doping profiles and channel lengths by epitaxial growth. With low temperature CVD or MBE, very sharp profiles can be realized. The critical issue of this method is that because of oxidation-enhanced-diffusion or transient enhanced diffusion during subsequent processing (e.g. the gate oxidation on a pillar sidewall), excessive dopant diffusion can prevent successful device fabrication below channel lengths of 100 nm. In this paper, we report (i.) the growth of record ultra-sharp n-channel VFET structures by low temperature RTCVD, (ii.) the stabilization of such structures against phosphorus diffusion from the source-drains by the use of SiGeC for the first time, and (iii.) the first ~50 nm device results. The first topic addressed is the growth of ultra-sharp n-type doping profiles, which is a classical issues with both CVD and MBE because of surface segregation effects of P and As. By employing a surface cleaning technique when making the transition from high (~1020 cm-3) to low P doping[1,2] and a high pressure growth method to increase the P incorporation, a record transition slope on falling P profiles as sharp as ~3 nm/decade can be achieved, vs. < 100nm/decade with conventional approaches. On the rising edge, the P slope was improved from ~20 nm/decade to an ultrasharp transition of ~5 nm/decade (limited by SIMS resolution) by pre-dosing the interface with phosphorus during a growth interrupt. Without such methods, rising slopes of ~20 nm/decade are commonly observed. The VFET process employs a wet oxidation step at 750°C to grow gate oxide on the pillar sidewalls. It is well known that the interstitial silicon atoms injected by oxidation can increase diffusion P and B diffusion coefficients by ~30X at this temperature. As previously reported for p-channel devices[3,4], incorporating SiGeC regions in the source/drains to getter the interstitial silicon atoms can greatly reduce this undesired effect so that short channel structures can be realized. Here we report the results of this method applied to n-channel structures for various S/D doping levels, and the subsequent device results. For the first time we have successfully realized vertical n-channel FET's with channel lengths under 50 nm using CVD epitaxial growth. This work was supported by DARPA (N660001-97-1-8904) and ARO (DAA655-98-1-1270). [1]J. O. Chu, K. Ismail, and S. Koester, Abs. 40th Elec. Mat. Conf., Charlottesville, VA (1998); [2]M. Yang, M. Carroll, J. C. Sturm, and T. Buyuklimanli, J. Electrochem. Soc. 147, 3541-3545 (2000); [3]M. Yang, C-L. Chang, M. Carroll, and J. C. Sturm, IEEE Elec. Dev. Lett. 20, pp. 301-303 (1999); [4]M. Yang, and J. C. Sturm, Thin Solid Films 369, pp. 366-370 (2000).

9:00 AM (Student)

S3, Improvement of SiO2/SiGe Interface of SiGe pMOSFETs Using Water Vapor Annealing: *Tat Ngai*[1]; John Fretwell[1]; Xiao Chen[1]; James Chen[1]; Sanjay Banerjee[1]; [1]University of Texas at Austin, Microelect. Rsrch. Ctr., 10100 Burnet Rd., Austin, TX 78758 USA

The enhancement of hole mobilities in compressively-strained SiGe layers deposited on Si is well known. However, the realization of surface-channel SiGe PMOSFETs has been hindered by poor gate oxide quality. Although buried-channel SiGe PMOSFETs using thin Si cap layers can alleviate these problems, the reduction of effective gate capacitance is a drawback. A gate oxide deposition process using remote plasma chemical vapor deposition (RPCVD) has been developed to deposit ultra-thin gate oxides (down to 20 Å). These RPCVD oxides can be deposited directly on SiGe without a Si capping layer. Typical interfacial state density (Dit) values are 1 × 1010 cm2eV-1 and 3 × 1011 cm2eV-1 for Si and SiGe,

THURSDAY AM