RAPID THERMAL AND OTHER SHORT-TIME PROCESSING TECHNOLOGIES

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PREFACE

The international symposium on *Rapid Thermal and Other Short-Time Processing Technologies I* was held from May 14 through May 18, 2000 in Toronto, Canada as part of the 197th Meeting of the Electrochemical Society. For the second time this annual symposium on Rapid Thermal Processing (RTP) and related topics was held under the auspices of the ECS, with 49 papers scheduled and a high overall session attendance.
The purpose of this symposium, as that of its preceding events, was to provide an international forum for those working in the field of Rapid Thermal Processing to discuss all aspects of RTP and other related front-end CMOS technologies. The program focussed on recent innovations in equipment issues, short-time processing and their applications in the fabrication of nanoscale semiconductor microelectronics and other devices.

This book contains all refereed papers presented at the symposium. From its contents one can conclude that the focus of our annual symposium continues to shift from mainly instrumental issues (temperature control, uniformity and reproducibility) to issues concerning pushing the limits of ultrashallow junctions and ultrathin gate dielectrics in nanoscale CMOS manufacturing.
The development of new and improved RTP equipment is ongoing. For example, a revolutionary new floating wafer reactor concept was presented, where by means of heating in the hot-wall reactor wafers are gas-levitated. Furthermore, arc-lamp based RTP systems are revisited because of their potential to deliver higher temperature ramp rates than currently used and possible. These higher ramp rates are required to manufacture ultrashallow junctions in future devices, without problems induced by Transient Enhanced Diffusion. To that end "old" annealing techniques such as laser processing, athermal annealing using shock and sound waves, etc. are gaining attention again.

The symposium illustrated that the range of applications in RTP is still growing, but also that new, related short-time processing technologies technologies and challenges appear in advanced CMOS technology. In ultrathin gate dielectrics (and metallizations) Atomic Layer CVD may be a viable route to high-k materials with well-controlled thickness and performance. Thus the scope of our symposium widens.

A panel discussion was held on the key barriers emerging from this symposium, and on how stringent or not the ITRS roadmap requirements are. This discussion drew – as usual – a large audience. Our thanks are due to the panellists A. Agarwal (Eaton), A. Jain (Texas Instruments), K. Jones (University of Florida), M. Öztürk (North Carolina State University), S. Talwar (Verdant Technologies) and last, but not least, H. Huff (Sematech). Panel discussion moderator was J. Gelpey (STEAG RTP Systems). The main issue here was the perspective of advanced dielectric and metallization materials, and the (short-time) processing technologies needed in the future for sub-0.1 μm channel length.

The work presented in this volume includes comprehensive reviews as well as invited and contributed papers. The book contains seven major sections: 1) ultra-shallow

junctions, 2) contacts for nanoscale CMOS, 3) gate stacks, 4) new applications, 5) advances in RTP systems and process monitoring.

The editors are confident that this volume will provide scientists and technologists working in the field of RTP and related technologies with the latest developments, as well as understanding of the directions into which the key issues in front-end CMOS technology are evolving. We acknowledge the in-depth treatment by all authors of their fields of expertise. Our sincere appreciation goes to the persons who co-chaired sessions, and reviewed the papers.

Finally, we would like to acknowledge the financial support of our sponsoring ECS Divisions (Electronics, Dielectric Science and Technology, and High Temperature Materials Divisions) and of the following companies: Applied Materials, ASM International, CVC Products, Eaton Thermal Processing Systems, J.I.P.ELEC, Luxtron, Mattson Technology, STEAG RTP Systems and Vortek Industries. Many of these companiess belong to our 'traditional' core of sponsors. Without their continued support we could not uphold the high level of our symposium.

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July 2000

MECHANISMS AND APPLICATIONS OF THE CONTROL OF DOPANT PROFILES IN SILICON USING $Si_{1-x-y}Ge_xC_y$ LAYERS GROWN BY RTCVD

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Despite the reduced thermal budgets in modern ULSI processes, there are still many examples where the diffusion of common dopants adversely affects device performance. These especially include the cases of boron and phosphorus profiles, since the diffusion of these dopants is mediated by silicon interstitial atoms. Many process steps inject silicon interstitial atoms, which can lead to diffusion coefficients over an order of magnitude higher than those otherwise expected. In this paper, we first address the growth of structures with ultra-sharp doping profiles by RTCVD, and then discuss the use of $Si_{1-x-y}Ge_xC_y$ layers to control silicon interstitial profiles so that the sharp dopant profiles are maintained during device processing. Examples from vertical MOSFET structures are shown.

INTRODUCTION

Device scaling requires ever increasing abrupt device profiles. While most mainstream work is focussed on implanted profiles for conventional CMOS, in our work we are most interested in the development of ultra-sharp vertical device profiles by Rapid Thermal Chemical Vapor Deposition (RTCVD) in silicon and related $Si_{1-x-y}Ge_xC_y$ structures. There are two main challenges: first, one must grow tight device profiles at low temperature, and second, those profiles must be maintained during processing. The first challenge is difficult due to the traditional autodoping and reactor memory effects of n-type dopants. The second problem is made difficult by process steps such as ion implantation and annealing which create silicon interstitial atoms, which in turn can increase boron and phosphorus diffusion coefficients by over an order of magnitude at low process temperatures.

In this paper the ability to grow phosphorus doping profiles with a record transition rate (as sharp as 3 nm/decade) is first described. Second, the ability of $Si_{1-x-y}Ge_xC_y$ layers to suppress boron and phosphorus diffusion in nearby silicon regions is discussed. Finally, these steps are combined to grow vertical device profiles for both p-channel and n-channel FETs which are stable under post processing conditions. Channel lengths as short as 25 nm have been demonstrated.

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GROWTH OF ABRUPT DOPING PROFILES BY RTCVD

Abrupt boron profiles (< 10 nm/decade, limited by SIMS resolution) in low-temperature silicon-based epitaxy are relatively straightforward to achieve by switching the boron source gas (typically diborane) on and off [1-3]. On the other hand, the problems with arsenic and phosphorus doping profiles in silicon-based layers grown by CVD was well known from conventional epitaxial growth at high temperatures, and they have continued with growth at lower temperatures of 800 °C or less [4-6]. All of the data shown in this paper derive from an RTCVD growth system using dichlorosilane as the silicon source gas typically operating at 6 torr in a hydrogen carrier. Diborane, germane, phosphine, and methylsilane are added as sources of boron, germanium, phosphorus, and carbon, respectively [7,8]. For silicon growth in the range of 700 - 800 °C, when the phosphine source is switched off, the phosphorus profiles typically decay with a rate of ~100 nm/decade, with a background level between 10^{17} - 10^{18} cm^{-3} (profile marked "continuous growth" in Fig. 1). This clearly precludes the direct growth of device profiles on the scale of 100 nm or less.

One approach towards achieving sharper phosphorus profiles demonstrated with low-temperature Ultra High Vacuum (UHV) CVD epitaxy was to remove the wafer from the growth chamber after the n-type growth and chemically etch its surface to remove any phosphorus which may have segregated to the wafer surface. The wafer was then reinserted into the growth system and growth was resumed [10]. While this method was successful at achieving sharper phosphorus profiles, residual contamination was observed at the interrupt interface by SIMS. To adapt this process for RTCVD and to overcome this contamination drawback without causing excessive diffusion of doping profiles, a low-temperature cleaning process was developed involving an optimized wet clean followed by a short bake in hydrogen at 800 °C before epitaxy at a lower temperature. The quality of the interface was initially monitored by checking the photoluminescence of $Si_{1-x}Ge_x$ layers grown directly at 625 °C on this interface. Figure 2 shows the luminescence strength of the $Si_{1-x}Ge_x$ layer, which is a measure of carrier lifetime and thus the absence of interfacial contamination, as a function of the hydrogen pressure during a 1-min 800 °C anneal to desorb surface contamination. Optimum results are achieved in the 1-10 torr range. At pressures less than 1 torr, the low hydrogen coverage of the surface makes it susceptible to contamination, and at pressures over 10 torr, the partial pressure of contaminants in the hydrogen leads to contamination. Using such a process, layers with both carbon and oxygen contamination below the limits of SIMS resolution at the interface can be achieved, without any detectable motion of existing dopant profiles [11]. The ability to rapidly change the wafer temperature is critical for these results since it enables a short (~ 1 min) cleaning cycle at a temperature well above the growth temperature.

Applying such a process to the growth of abrupt phosphorus transitions by removing the wafer from the RTCVD reactor after n-type growth had a limited

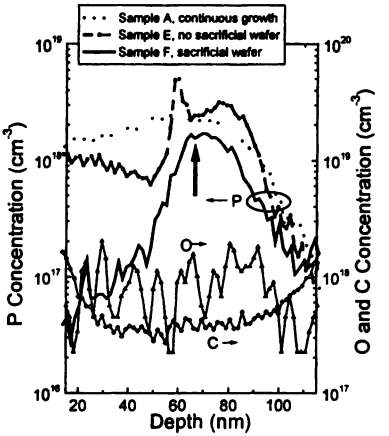


Fig. 1. Phosphorus profiles (by SIMS) from RTCVD of silicon at 700 °C where the interface was created by simply turning off the phosphine flow (sample A), removing the wafer from the reactor after the n-type growth and cleaning its surface before resuming growth (sample E), and cleaning the wafer as in (b) and cleaning the reactor with a dummy run when the wafer is removed before reloading (sample F) [9]. The vertical arrow shows the location of the interrupted growth for sample E and F.

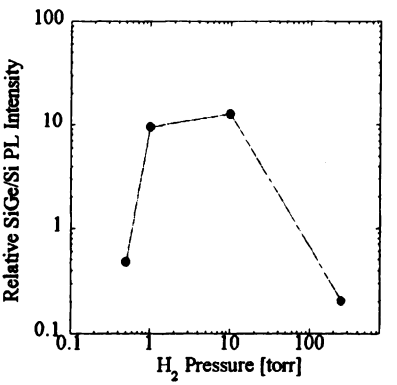


Fig. 2. SiGe/Si photoluminescence ratio (measured at 77K) of $Si_{0.8}Ge_{0.2}$ layers grown at 625 °C directly on silicon substrates after wet cleaning/HF/dip followed by a 1 min bake in hydrogen at 800 °C at different pressures [11].

improvement on the profile ("sample E, no sacrificial wafer" in Fig. 1). The background doping was still on the order of 10^{18} cm^{-3}. To further improve the profile, it was necessary to grow a "sacrificial wafer" in the reactor during while the device wafer was removed from the reaction chamber for surface cleaning. This dummy wafer gettered the residual phosphorus contamination in the reaction chamber, which was presumably sticking to the quartz walls. With such a combination of steps, abrupt phosphorus profiles of transition rate ~13 nm/dec. with a background < 10^{17} cm^{-3} could be achieved, without any detectable residual oxygen or carbon contamination at the interface ("sample F" in Fig. 1) [9]. Furthermore, we have observed that if the initial phosphorus level is higher (e.g. on the order of 10^{19} cm^{-3} or more), the phosphorus transient can be even sharper. Figure 3 shows a sample grown at 700 °C with an initial n-type doping 2 x 10^{19} cm^{-3} in which the falling phosphorus profile resulting from such an interrupt growth measured <4 nm/decade, again without residual interface contamination. To the best of our knowledge, this is the sharpest transition achieved to date for any n-type doping profile in silicon by CVD. Further work is needed to achieve equally sharp profiles on the rising edge of the n-type doping as seen in Fig. 3.

SiGeC AND DOPANT DIFFUSION

Both boron and phosphorus diffuse primarily via interstitialcy mechanisms, and thus have diffusion coefficients which are proportional to the silicon interstitial concentration [12]. Oxidation and ion implantation are known to inject interstitials into silicon, leading to the well-known oxidation-enhanced diffusion (OED) and transient-enhanced diffusion (TED) effects, respectively, in which the diffusion coefficients can easily be more than an order of magnitude above that for the structure in thermal equilibrium. The effect is especially severe at temperatures below 900 °C since in that range the normal equilibrium diffusion coefficients are very low. However, substitutional carbon (typically at a concentration of 0.1 - 1 %) in either Si or SiGe greatly reduces or eliminates this effect, presumably due to some reaction of the carbon to consume the interstitial silicon atoms [13-15]. To eliminate concern of carbon related defects being present in critical device regions, one can also put the carbon containing layer elsewhere in the device so that it intercepts the interstitials before they interact with the critical device profile [15].

Such an experiment is shown schematically in Fig. 4. A buried SiGeC layer is designed to consume interstitials injected during oxidation. The diffusion of boron in marker layers is used as a measure of the local interstitial concentration. Figure 5 shows the results of one such experiment, where the boron profiles both as-grown and after either annealing in nitrogen or oxygen at 850 °C are shown. Note that near the surface there is substantial OED, in that the profile after oxidation is much wider than that after nitrogen annealing. On the other hand, the boron below the SiGeC layer shows no difference in the two cases since the silicon interstitial atoms injected by oxidation did not go past the SiGeC layer [16].

By using multiple boron peaks above the SiGeC layer, as in the sample of Fig. 5, the profile of the boron diffusion coefficient, and thus the concentration of the silicon

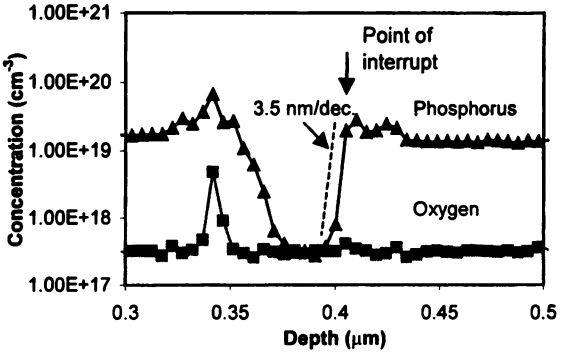


Fig. 3. Phosphorus and oxygen profiles by SIMS for a silicon layer grown at 700 °C where the growth was interrupted and the wafer cleaned ex-situ to achieve an ultra-sharp falling phosphorus profile (< 4 nm/decade).

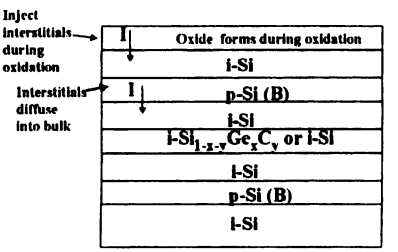


Fig. 4. Schematic of test structure for investigating effects of SiGeC on silicon interstitial profiles (in this case during oxidation) through the use of boron-doped marker layers.

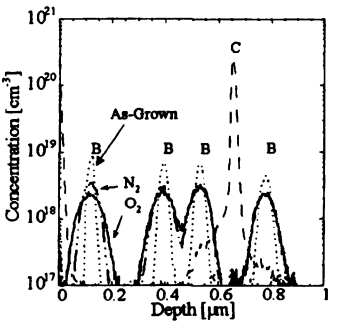


Fig. 5. Boron profiles of a test structure with a buried SiGeC layer as-grown by RTCVD and after annealing at 850 °C for 30 min in either oxygen or nitrogen [17].

interstitial atoms can be deduced (Fig. 6). At 850 °C, in the case of no SiGeC layer, the silicon interstitials diffuse far into the substrate to create enhanced diffusion over a wide depth. In the case of a SiGeC layer at a depth of either 250 or 700 nm, a straight line profile for the interstitials is found, consistent with that expected for a particle which travels by diffusion and which has a perfect sink within a diffusion length. In all cases an enhancement of the surface interstitial concentration of 9-13 X (the same value within experimental error) above that in equilibrium (nitrogen anneal) is found. A value of ~25 is found at 750 °C. This means that although clearly more interstitials are injected into the substrate (from the sharper diffusion gradient in sample C), the surface boundary condition during oxidation remains fixed. That is, the boundary condition on the surface during oxidation is apparently a fixed interstitial density, not a fixed interstitial injection rate into the substrate.

By combining the profiles of the enhancement of the interstitial concentration with diffusion coefficient information from the literature [18], the actual number of injected interstitial atoms during oxidation can be calculated. This is shown at both 750 and 850 °C for 120 min in Fig. 7. The presence of the SiGeC layer near the surface to pin the silicon interstitial concentration near zero increases the injected flux by four orders of magnitude, but the surface can still supply enough interstitials to keep the surface concentration fixed. In the highest case, the injected interstitials are still only < 1 % of the silicon atoms consumed by oxidation.

As the silicon interstitial atoms interact with the SiGeC the carbon comes out of substitutional sites. Thus this occurs faster during oxidation than nitrogen annealing, and eventually the layer may lose its ability to consume silicon interstitial atoms. The exact interaction between the interstitial atoms and the carbon at high temperature is not known, and an ongoing goal is to use the interstitial injection rate information given above to probe this reaction.

In structures with SiGeC, there also is a strong tendency in some cases for boron profiles to become sharper, as opposed to just having a reduced diffusion coefficient. This is not explained by interstitial profiles, and is associated with the segregation of boron to SiGeC layers. The phenomenon is not fundamentally understood, but it is not associated with a loss of electrical activity of the boron. This effect has been successfully employed to reduce boron penetration from boron-doped p^+ polysilicon gates through thin gate oxides into the substrate channel region in p-channel transistors [19]. At present, however, the mechanism behind this effect is not yet understood.

VERTICAL FETS

One attractive device structure for deep submicron FET scaling is a vertical FET. If the structure is grown by epitaxy, then the channel length is no longer defined by lithography but rather the layer thicknesses. While such devices still suffer today from parasitic capacitances and other practical problems, clever approaches are being developed to overcome such problems [20]. An approach we have followed for

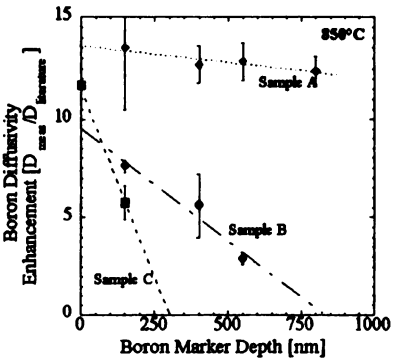


Fig. 6. Extracted profiles of the enhancement of silicon interstitial concentrations above their equilibrium values for (a) no SiGeC layer, (b) SiGeC layer at a depth of 800 nm from the surface, and (c) SiGeC layer 250 nm above the surface).

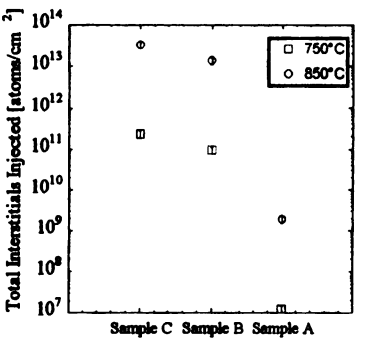


Fig. 7. Calculated number of interstitial silicon atoms for 120 min oxidation at 750 and 850 °C for (a) no SiGeC, (b) SiGeC 800 nm below the surface, and (c) SiGeC 250 nm below the surface.

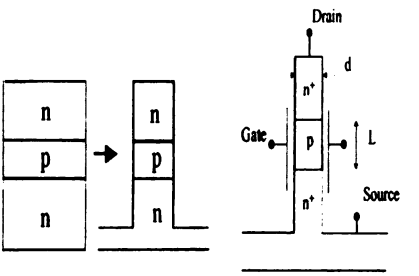
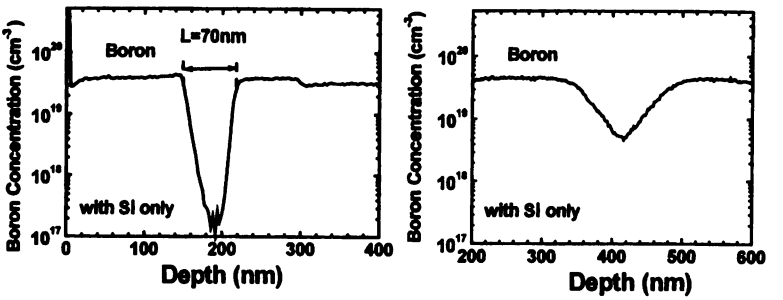
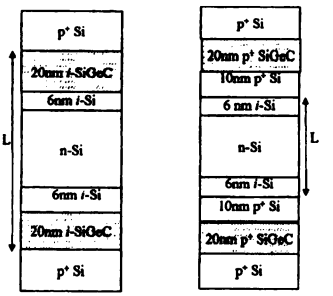


Fig. 8. Schematic cross section of fabrication and final structure of vertical MOSFETs as described in this work.



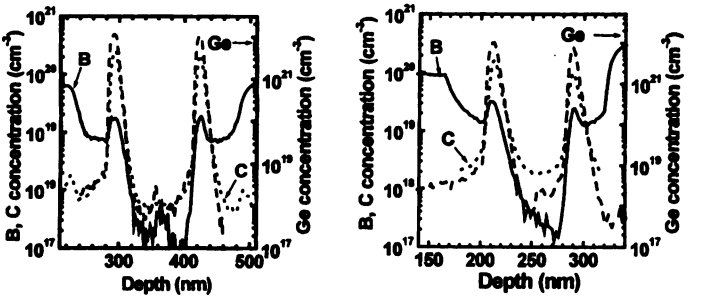
(a) (b)

Fig. 9. Boron profiles of vertical p-channel MOSFET structures (a) as-grown and (b) after 750 °C wet oxidation for 30 min without any SiGeC.



(a) (b)

Fig. 10. Vertical p-channel FET structures using SiGeC for the suppression of boron diffusion with (a) undoped SiGeC in channel and (b) doped SiGeC in source/drains.



(a) (b)

Fig. 11. Boron profiles both (a) as-grown and (b) after all processing including 750 °C 30 minute wet oxidation of structures with doped SiGeC in source drains.

developing both p-channel and n-channel devices is shown in Fig. 8. An npn (or pnp) structure is first grown, followed by vertical etching to create sidewalls. After thermal oxidation and doped polysilicon deposition for the gate, conventional backend processing completes the structure. (If the pillar is very thin, then the channel doping can be eliminated [21].)

In the process described above, the gate oxide must be grown after the epitaxial step. Therefore, the source/drain dopant will be subject to oxidation-enhanced diffusion, which will greatly limit the channel length. In our work, we have used a steam gate oxidation process at 750 °C for 30 min, which grows approximately 10 nm of gate oxide on a (100) silicon surface. The severe effect of such a short oxidation on the boron in the source/drains of a p-channel device made in all silicon is shown in Fig. 9, which clearly renders sub-100-nm devices impossible. Standard process modeling shows that nearly all of this diffusion is due to OED effects. Further deleterious effects might be expected from TED from any ion implants to improve the contact on top of the pillar (not used in this work). We thus investigated using SiGeC structures to stop the excess boron diffusion without degrading device electrical properties. In our first attempt, undoped SiGeC regions were placed inside the channel region, and the motion of the boron would stop when it hit the SiGeC due to the low diffusion coefficient of boron in the SiGeC (Fig. 10a). Such an approach was very effective at stopping boron diffusion, but having SiGeC in part of the channel led to device problems associated with oxidizing the SiGeC [22].

The next improvement was to make the channel and the parts of the source/drain near the channel entirely out of silicon, and to put a SiGeC region only a few nm from the doped silicon source/drains (Fig. 10b). Despite the fact that there are heavily-doped boron regions in silicon next to the all-silicon channel, the boron OED into the channel was still completely suppressed, due to the ability of the SiGeC to locally reduce the silicon interstitial concentration in nearby silicon regions (Fig. 11). By incorporating a phosphorus-doped channel with the interrupt techniques described earlier in the work to achieve a sharp profile, the final device profile (after gate oxidation and all device processing) is shown in Fig. 12. Note, that the channel is still clearly resolved despite the 750 °C wet gate oxidation. Figure 13 shows the I-V curves from the resulting FET. Ideal behavior was observed, and no excess leakage current compared to that in long-channel all-silicon devices (since short channel was not possible with all-silicon) was observed. Therefore, no defects or complexes resulting from the carbon were reducing lifetime in critical device regions. 25 nm devices have been successfully achieved by reducing the channel length (leaving the rest of the structure unchanged) [22].

Our present work is focussed on n-channel devices so that both p-channel and n-channel devices for CMOS are available. Phosphorus is used as a source/drain dopant (e.g. Fig. 3). As in the case of boron doped source/drains for p-channel devices, OED during gate oxidation significantly limits the shrinking of the channel length (Fig. 14). To address this problem, as in the case of p-channel devices, we have developed a doped SiGeC source/drain structure, where the SiGeC limits the OED on the dopant in the

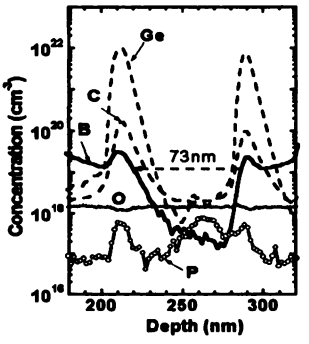


Fig. 12. Final p-channel device profile after all high temperature processing for a ~75 nm device. Processing includes an interrupt and ex-situ wafer cleaning after the phosphorus doping in the channel.

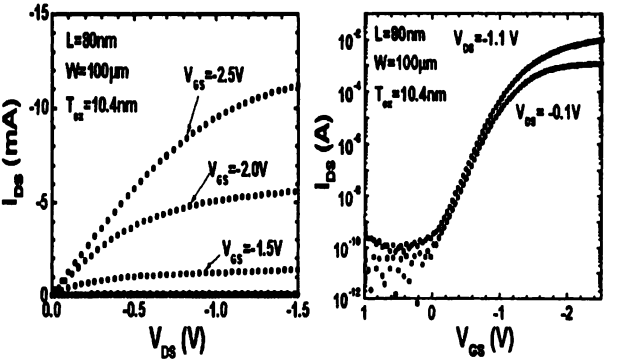
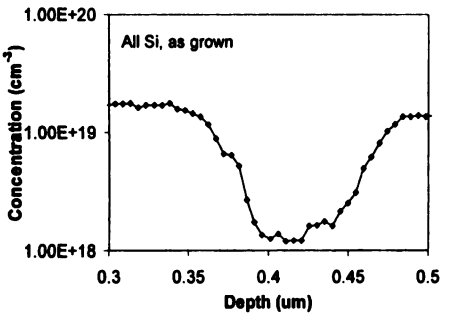


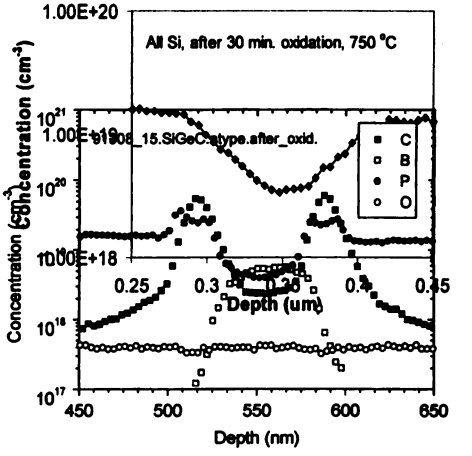
Fig. 13. I-V curves of ~75 nm channel length vertical p-channel MOSFETs from the structure of Fig. 12. W = 100 μm and gate oxide is 10 nm.

Fig. 14. Phosphorus profiles of vertical n-channel devices both as grown and after 750 °C wet gate oxidation. No interrupt was used in these structures, leading to the relatively poor phosphorus profiles.

nearby all-Si S/D regions to prevent diffusion of the source/drain dopant into the channel.



This is demonstrated in Fig. 15, where the dopant profiles as-grown and after processing are nearly unchanged. The



structures shown have a channel length of ~50 nm, so scaling down to the ~10 nm regime should be possible.

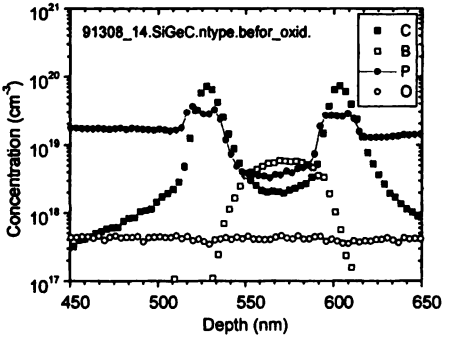


Fig. 15. Improved stability to gate oxidation of vertical n-channel MOSFET structures using n-type doped SiGeC source/drains. (a) is as-grown and (b) is after the 750 °C wet gate oxidation. Again no interrupt was used leading to the relatively poor initial phosphorus profiles.

CONCLUSIONS AND FURTHER WORK

Extremely abrupt device profiles of both p-type and n-type dopants can be grown by RTCVD with interfaces on the scale of nanometers. Although not yet quantitatively understood, SiGeC can be used to stabilize these profiles during subsequent processing against OED and related phenomena. SiGeC multilayer structures can also be used to probe the fundamental phenomena of interstitial injection during oxidation which underlies OED. Using such processes, both n-type and p-type vertical MOSFETs can be fabricated with channel lengths as short as 25 nm.

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REFERENCES

1. B. S. Meyerson, F.K. LeGoues, T.N. Nguyen, and D.L. Harame, *Appl. Phys. Lett.* **50,** 113 (1987).
2. P.J. Roksnoer et al., *Appl. Phys. Lett.* **58,** 711 (1991).
3. V. Venkataraman, P.V. Schwartz, and J.C. Sturm, *Appl. Phys. Lett.* **59,** 2871 (1991).
4. B.S. Meyerson and M.L. Yu, *J. Elecrochem. Soc.* **131,** 2366 (1984).
5. D. W. Greve and M. Racanelli, *J. Electrochem Soc.* **138,** 1744 (1991).
6. J.H. Comfort and R. Reif, J. *Appl. Phys.* **65,** 1053 (1989).
7. J.C. Sturm, P.V. Schwartz, E.J. Prinz, and H. Manoharan, *J. Vac. Sci. Tech.* B **9,** 2011 (1991).
8. A. St. Amour, C.W. Liu, J.C. Sturm, Y. Lacroix, and M.L.W. Thewalt, *Appl. Phys. Lett.* **67,** 3915 (1995).
9. M. Yang and M.L. Carroll and J.C. Sturm, J. *Electrochem. Soc.*, to be published, 2000.
10. J. Chu, K. Ismail, and S. Koester, 40th Elec. Mat. Conf., Charlottesville, VA (1998).
11. M. Carroll, M. Yang, and J.C. Sturm, *Electrochem Soc. Symp. Proc.* **99-10,** 319 (1999), and M. Carroll and J.C. Sturm, submitted, *J. Electrochem. Soc.*, (2000).
12. P.M. Fahey, P.B. Griffin, and J.D. Plummer, *Amer. Phys. Soc., Rev. Mod. Phys.* **61,** 289 (1989).
13. P.A. Stolk, D.J. Eaglesham, H.-J. Gossman, and J.M. Poate, *Appl. Phys. Lett.* **66,** 1370 (1995).
14. P.A. Stolk, H.J. Gossman, D.J. Eaglesham, and J.M. Poate, *Mater. Sci. Eng.* B**36,** 275 (1996).
15. L.D. Lanzerotti, J.C. Sturm, E. Stach, R. Hull, T. Buyuklimanli and C. Magee, *Appl. Phys. Lett.* **70,** 3125 (1997).
16. M.S. Carroll, C-L. Chang, J.C. Sturm, T. Buyuklimanli, *Appl. Phys. Lett.* **73,** 2695 (1998).
17. M.S. Carroll and J.C. Sturm, *Mat. Res. Soc. Symp. Proc.*, in press. (MRS Spring 2000 Meeting, San Francisco, April, 2000).
18. H. Bracht, N.A. Stolwijk, H. Mehrer, *Phys. Rev.* B **52,** 16542 (1995).
19. C.L. Chang and J. C. Sturm, *Appl. Phys. Lett.* **74,** 2501 (1999).
20. J.M. Hergenrother, et al., IEDM Tech. Dig. (1999).
21. D.J. Frank, S.E. Laux, and M.V. Fischetti, IEDM Tech. Dig. 553 (1992).
22. M. Yang, C.L. Chang, and J.C. Sturm, *IEEE Elec. Dev. Lett.* **20,** 301 (1999).