1998 Electronic Materials Conference

TECHNICAL PROGRAM

University of Virginia · Charlottesville, Virginia · June 24 - 26, 1998

*** Indicates *Invited** **+ Indicates Student Paper**

Wednesday, June 24, 1998

EMC PLENARY LECTURE/STUDENT AWARDS

Ceremony: 8:30 AM

Room: 402, Chemistry Building

Session Chairman: Thomas Kuech, University of Wisconsin, Dept. of Chemical Engineering, Madison, WI 53706

Plenary Speaker: Laurence Eaves, University of Nottingham, Dept. of Physics, Nottingham, NG7 2RD UK

Topic: "Superlattices and Resonant Tunnelling: A Quarter-Century Overview"

BREAK: 9:30 AM - 10:00 AM

WEDNESDAY AM

June 24, 1998

Session A. Novel Contacts and Low Temperature - Grown Materials

Room: E303
Location: Thornton Hall

Session Chairs: Len Brillson, The Ohio State University, 205 Dreese Lab, Columbus, OH 43210-1272 USA; Suzanne Mohney, Penn State, University Park, PA 16802

10:00 AM, A1+

Studies of Schottky Barrier Height of $Ga_xIn_{1-x}P$ ($0 \leq x \leq 1$) For HFET Applications: H. C. KUO[1]; H. Hsia[1]; D. Caruth[1]; B. G. Moser[1]; Z. Tang[1]; S. Thomas[1]; M. Feng[1]; G. E. Stillman[1]; C. H. Lin[2]; H. Chen[2]; [1]University of Illinois at Urbana-Champaign, Electrical and Computer Engineering, Microelectronics Laboratory, Urbana, IL 61801 USA; [2]University of Ilinois at Urbana-Champaign, Materials Research Laboratory, Urbana, IL 61801 USA

The incorporation of an InGaP Schottky barrier enhancement layer (SBEL) is very attractive for the InP based MESFET and HFET applications since $Ga_xIn_{1-x}P$ ($0 \leq x \leq 1$) have energy gaps covering the range from 1.35 to 2.24eV at room temperature and a conduction band discontinuity of GaInP/InP ($\Delta Ec=0.8\Delta Eg$ for GaP on InP) is favorable for SBEL. Also there are no DX centers in GaInP. The performance of InP FETs strongly depends on the optimization of the gate contact. Knowledge about the dependence of the Schottky barrier heights on the material composition of GaInP is very important. However, to the best of our knowledge, a systematic study of the Schottky barrier heights of GaInP on InP for varying gallium composition has not been reported in the literature. In this talk, we presents a study of Schottky barrier heights for GaInP ($0 \leq x \leq 1$) on InP using both I-V, I-V-T and C-V measurements. The device performance of InGaAs/InP HFETs utilizing GaInP SBEL will also be discussed. All layers structure were grown by GSMBE on InP substrates using In and Ga as group III sources and AsH_3 and PH_3 as group V sources. For C-V measurements, 0.5 μm thick Si-doped ($4\text{-}6X10^{17}$ cm^{-3}) GaInP samples with various Ga composition (0, 0.2, 0.3, 0.4, 0.5) were grown. Metamorphic buffer layers were grown on the InP substrate to reduce threading dislocations and improve the measurement reliability, even though C-V technique is not very sensitive to defects. The barrier heights were determined from the intercept voltages of the $(A/C)^2$-V plots. The compositional variation of the barrier heights for Au/GaInP/InP obtained from C-V measurements is nearly identical to that of the conduction-band offsets for InGaP/InP heterointerfaces. This result is consistent with the metal-induced gap states (MIGS) model of the Schottky barrier formation. Another series of samples of undoped $Ga_xIn_{1-x}P$ (x=0.2, 0.3, 0.4, 0.5,1) were grown on InP substrates for I-V measurement. The thickness of all GaInP SBELs was below critical layer thickness to prevent dislocation induced leakage current (no dislocations were observed by TEM). Using the thermionic-emission current equation and these characteristics, the effective barrier height was estimated to be in the range from 0.65 to 0.81 eV (ideality factors 1.01~ 1.3). This values are much lower than the data obtain from C-V measurements because the tunneling current increases as the thickness of the GaInP layer is decreased. We have designed and fabricated 0.25 μm gate-length InGaAs/P doped channel HIFETs utilizing 150 A $Ga_{0.2}In_{0.8}P$ SBEL. These devices show very good DC and RF performance. The extrinsic transcondance is 665 mS/mm. The f_{max} was 168 GHz and the f_T was 117 GHz. These results are comparable with InAlAs/InGaAs HEMTs which indicate the GaInP is a promising material for replacing InAlAs as gate SBEL material for InP based HFET applications.

10:20 AM, A2+

Reliability Studies on InAs/GaP and Au/Ti/GaP Schottky Diodes: J. JEON[1]; E. H. Chen[1]; V. Gopal[1]; E. P. Kvam[1]; J. M. Woodall[1]; [1]Purdue University, School of Engineering and NSF-MRSEC for Technology-Enabling Heterostructure Materials, West Lafayette, IN 47907-1289 USA

Schottky rectifiers have been widely utilized in semiconductor industry. Typically, these diodes consist of a metal in contact with a semiconductor material. However, thermal stability has been an important issue on these metal-semiconductor devices because of the metallurgical changes that can occur at the interface during any kind of intentional or unavoidable heat treatments. Recently, Chen et al reported that direct growth of InAs on GaP has shown promise as a Schottky diode. The resulting I-V characteristics showed low leakage currents and high breakdown voltages in reverse bias region and nearly ideal, Schottky-barrier like, forward bias characteristics with ideality factors of 1.1 or less. Since InAs/GaP junction has a large lattice mismatch (~11%), we expect that this mismatch could suppress the atomic inter-diffusion across the interface between InAs and Gap and hence reduce the mutual solubility of InAs and Gap. In this paper we discuss device reliability under thermal stress. Samples were prepared by Molecular Beam Epitaxy. After growth of a lightly doped (n=1E17) GaP layer, a thin heavily-doped (n=1E19) InAs layer (300 A) was deposited directly on GaP buffer. A thick heavily doped $In_{0.8}Ga_{0.2}As$ layer was grownon top for the purpose of making ohmic contact by AuTi evaporation. The device active region is at the InAs/GaP heterojunction. For comparison, metal-semiconductor Schottky diodes were fabricated by evaporating Au/Ti metal films on MBE grown GaP (1E17) materials. Both InAs/GaP and Au/Ti/GaP devices were annealed under a nitrogen ambient at various

Uemura and T. Baba: Jpn. J. Appl. Phys. 33 (1994) L1363. [2] T. Uemura and T. Baba: IEEE Electron Device Lett. 18 (1997) 225.

4:30 PM, G9

Negative Differential Resistance of CdF$_2$/CaF$_2$ Resonant Tunneling Diode on Si(111) Grown by Partially Ionized Beam Epitaxy: MASAHIRO WATANABE[1]; Yuichi Aoki[1]; Wataru Saitoh[2]; Mika Tsuganezawa[1]; [1]Tokyo Institute of Technology, Research Center for Quantum Effect Electronics, 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan; [2]Tokyo Institute of Technology, Electrical and Electronic Engineering, 2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552 Japan

Epitaxial growth of nanometer-thick CdF$_2$/CaF$_2$ multilayered heterostructures on a Si(111) substrate using partially ionized beam epitaxy has been demonstrated. Triple barrier resonant tunneling diode (RTD) consisting of these heterostructures were fabricated on Si and negative differential resistance (NDR) characteristics have been observed at room temperature. CdF$_2$/CaF$_2$ heterostructure is one of the attractive candidates for quantum effect devices on Si substrate such as resonant tunneling diodes and quantum cascade lasers because of its large conduction band discontinuity (2.9eV) at the heterointerface. CdF$_2$ and CaF$_2$ have fluorite lattice structure and well lattice matched to Si with mismatches of -0.8%, +0.6% at room temperature, respectively. Recently, epitaxial growth of CdF$_2$/CaF$_2$ heterostructure on Si(111) using molecular beam epitaxy (MBE) has been reported and room temperature NDR with double barrier RTD has been demonstrated by A. Izumi et al. In this paper, we have introduced partially ionized beam epitaxy (PIBE) for obtaining atomically flat CdF$_2$-CaF$_2$ heterointerface using ionization and acceleration of CaF$_2$. N-type Si(111) substrate with 0.1ϒ misorientation was chemically cleaned and protective oxide layer was removed in ultra high vacuum chamber by thermal heating with Si flux. First of all, 1nm-thick CaF$_2$ was grown at 750ϒC, with ionization by electron bombardment without acceleration bias voltage (V$_a$). Ionization of CaF$_2$ was effective for improvement of CaF$_2$ flatness and coverage over Si surface probably because ionized CaF$_2$ tends to make strong bonding with Si. Subsequently, 5nm-thick CdF$_2$ buffer layer was grown on the CaF$_2$ at 50ϒC. After the buffer layer growth, CaF$_2$ was grown at 50ϒC with ionization and acceleration V$_a$=2kV and CdF$_2$ was grown at 50ϒC without ionization. The structure of triple barrier RTD is as follows: Al electrode (electron injector)/1nm-thick CaF$_2$ barrier/ 2nm-thick CdF$_2$ quantum well/ 1nm-CaF$_2$ / 1nm-CdF$_2$/ 1nm-CaF$_2$ / 5nm-thick CdF$_2$ buffer layer/ 1nm-thick CaF$_2$ buffer layer/ n-type Si(111) substrate/ Al electrode. Diameter of the top Al contact was 0.018mm. In the measurement of current-voltage characteristics, clear NDR was observed at room temperature and the maximum peak to valley (P/V) ratio was about 14. The NDR characteristic was almost reproduced three times and the bias voltage of peak current was 1.5V, which agreed well with theoretical estimation. The peak current density was 70-95A/cm^2, which is approximately 10 times lower than theory probably because the resonant tunneling occurred in a part of the whole contact area of devices due to the barrier thickness fluctuation. References:[1]A. Izumi, N. Matsubara, Y. Kushida, K. Tsutsui, and N. S. Sokolov: Jpn. J. Appl. Phys., 36 (1997) 1849. [2]M. Watanabe, W. Saitoh, Y. Aoki, J. Nishiyama: Solid State Electronics, to be published.

4:50 PM, G10

Late News

Wednesday PM, June 24, 1998

Session H. Growth and Characterization of SiGe and SiGeC Heterostructures

Room: 005
Location: Olsson Hall

Session Chair: Julia Hsu, University of Virginia

1:30 PM, H1+

Luminescence Analysis of Germanium Nanostructures Grown on SiGe/ Si (118) by MBE: MURIELLE SERPENTINI[1]; Georges Bremond[1]; Abdel Kader Souifi[1]; Mario Abdallah[2]; Isabelle Berbezier[2]; [1]INSA Lyon, Laboratoire de Physique de la matière, UMR-CNRS 5511, bâtiment 502, 20 Avenue A.Einstein, Villeurbanne, Rhône 69621 France; [2]Campus de Luminy, CRMC2-CNRS, CASE 913, Marseille, Bouches du Rhone 13288 France

Quantum dots are expected to increase quantum efficiency and therefore are good candidates for the development of Si-based Optoelectronics. With this aim in view, self-organization growth on silicon (118) substrate seems to be a promising technique. The principle is as follows: a SiGe undulating layer is obtained by the growth on a silicon (118) substrate, then Ge is deposed on these undulations according to the Stranski-Krastanov mode. Using this method, the island lateral size can be better controlled. In this work we describe a photoluminescence investigation of such Si/Ge/SiGe/Si structures. We dispose of three samples with variable Ge thickness D (1, 3 and 7 monolayers) and one sample containing 7 monolayers of Ge without the first SiGe wetting layer. The study consists of time-resolved measurements and analyses of the photoluminescence signal as function of power excitation and temperature. Low temperature PL spectra show the 2D/3D changeover in the growth mode which occurs between D = 3ML and D = 7 ML. When increasing the temperature up to 300 K, the dots-related luminescence persists for the sample with D = 7 ML. For D = 3 ML, we observe a luminescence correlated to thickness oscillations. When increasing the power excitation, results show a shift of the picks towards higher energies. This shift is very significant for D = 7 ML, so we assume that the 3D-related transition is a type II optical transition. Time-resolved measurements are used in order to discuss the PL life-time of 2D and 3D related-transitions. This allows to separate the different contributions arising from different regions of the structures.

1:50 PM, H2+

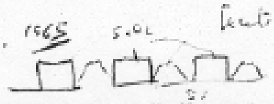
Mechanisms Determining Three-dimensional SiGe Islands Density on Si(001): J. S. SULLIVAN[1]; H. Evans[1]; M. R. Wilson[1]; T. F. Kuech[2]; M. G. Lagally[1]; [1]University of Wisconsin - Madison, Materials Science Department, 1500 Engineering Drive, Madison, WI 53706 USA; [2]University of Wisconsin - Madison, Department of Chemical Engineering, 1415 Engineering Drive, Madison, WI 53706 USA

Thin, epitaxial films of SiGe deposited on Si(001) can form three-dimensional (3-D), coherently strained islands via a modified Stranski-Krastanov growth mode. Scientific interest in such islands has shifted from their novelty to mechanisms of growth and of formation. Additionally, engineering films with specific island sizes and densities may be of practical value for unique optoelectronic properties. This paper describes the mechanisms affected by common process variables in epitaxial growth and how these mechanisms determine film morphology. We deposited SiGe films on Si(001) using low-pressure chemical vapor deposition in an ultra-high vacuum compatible reactor. Alloy composition, substrate temperature, and deposition rate were used to control the number density of faceted 3-D islands. Film growth was monitored with in-situ, real-time reflection high-energy electron diffraction, and the growth was quenched when the diffraction patterns displayed transmission spots and angled streaks indicating the presence of 3-D faceted islands. Atomic force microscopy was performed ex-situ to characterize film morphology. Island number density exhibits an Arrhenius-type dependence with substrate temperature. The density increases approximately a factor of two for every 50 K decrease in temperature (near 1000 K). Two thermally activated processes can account for increased island density with decreasing temperature, diffusion length and diffusion barriers. If the distance between two islands is greater than the diffusion length, another island is likely to nucleate between them. Diffusion barriers increase the two-dimensional (2-D) adatom gas density reducing the effective diffusion length at a given temperature. Three-dimensional island density increases as a power law with deposition rate. Increasing the deposition rate increases the 2-D adatom gas density. The higher 2-D adatom gas density leads to an effectively shorter diffusion length allowing 3-D islands to nucleate closer together. Number density is inversely proportional to Ge mole fraction in the alloy. Islands may "sense" the presence of other islands by strain fields that propagate through the substrate. A compressively strained coherent island will impart a compressive stress on the surrounding substrate which diminishes with distance from the island. The local chemical potential for the alloy near an island will increase due to the compressively strained substrate. The increased chemical potential prevents islands from being too close. Furthermore, alloy composition affects the magnitude of the strain fields such that higher Ge mole fractions increase the

3.C critical < Si growth rate (SiGe SiGeC [illegible])

radius around an island where nucleation of another island is unfavorable. The process variables of alloy composition, substrate temperature, and growth rate influence 3-D island density through various mechanisms. We will discuss our results in the context of simple thermodynamic and kinetic models that may be used to engineer films with a desired 3-D island density. This work was supported by the NSF.

ref. [illegible] 1565



2:10 PM, H3+

Facet Formations in Selective Epitaxial Growth of SiGe/Si Heterostructures Grown By Gas-Source Molecular Beam Epitaxy: GREG D. U'REN[1]; Mark S. Goorsky[1]; Kang L. Wang[2]; [1]UCLA, Dept. of Materials Science & Eng., 420 Westwood Plaza, 6532 Boelter Hall, LA, CA 90095-1595 USA; [2]UCLA, Dept. of Electrical Engineering, 420 Westwood Plaza, Room 66-147, Engineering IV, LA, CA 90095-1594 USA

disilane

Gas-source molecular beam epitaxy was used to investigate facet formations occurring in the selective epitaxial growth of $Si_{1-x}Ge_x/Si$ heterostructures (x < 0.2). We carried out experiments on nominal on-axis (100) Si substrates masked with 500-600 Å thermally grown SiO_2. Arrays 5 x 5 mm² of rectangular features 1-25 μm were defined by conventional photolithography techniques. Cross section transmission electron microscopy shows the development of {311} and {111} facets for a sidewall orientation parallel to the <110> directions. As growth proceeds and more importantly before lateral overgrowth, the {311} dominates. The combination of {111} and {311} facet growth leads to an overall lateral reduction of the (100) mesa top at an estimated rate of 2.2:1 [lateral reduction (x,y):epi thickness (z)]. The {311} facet grows approximately 3-4 times faster than the {111} facet, more quickly promoting the lateral reduction. With an appropriate Si buffer layer, the lateral dimension can be reduced beyond the original lithographic definition, which can be then used as a template for growth of SiGe heterostructures. Triple axis x-ray diffraction measurements of the selective epi determined that the crystalline quality is not compromised by the presence of facet growth nor subject to detectable additional strain relaxation mechanisms as a result of additional free surfaces for ≥ 1 μm structures. Also, from double axis x-ray measurements, no significant growth dependence as function of feature size was observed. The extent of reduction is determined by the oxide thickness. Lateral reduction continues until the epi thickness overcomes the oxide, at which point overgrowth occurs. For epitaxial overgrowth of SiGe, the {111} facet becomes dominant consuming the {311} facet. The results for lateral overgrowth of SiGe are consistent with overgrowth of Si.

311 facet first, 111 facet later.

2:30 PM, H4+

Complete Suppression of Oxidation Enhancement of Boron Diffusion Using Substitutional Carbon Incorporation: M. S. CARROLL[1]; C. L. Chang[1]; J. C. Sturm[1]; T. Buyuklimanli[2]; [1]Princeton University, Department of Electrical Engineering, Center for Photonics and Optoelectronic Materials, Princeton, NJ 08540 USA; [2]Evans East, Plainsboro, NJ 08536 USA

Boron diffusion and its enhancement via implant damage (transient enhanced diffusion, TED) and oxidation (oxidation enhanced diffusion, OED) are severe problems for the scaling of Si based devices. Recently, the suppression of boron diffusion and the reduction of its enhancement due to OED and TED mechanisms has been demonstrated through the incorporation of carbon in silicon[1,2]. In this paper we show for the first time the ability, through introduction of a thin SiGeC layer, to completely filter interstitials injected by an overlying oxidizing surface, which results in the complete elimination of OED for underlying boron. Further, we also quantify the ability of the SiCeC to reduce normal thermal diffusion and OED in Si layers lying above the SiGeC layer. The test structures were grown using rapid thermal chemical vapor deposition (RTCVD), between 600 and 750°C using methysilane as the carbon source. A double peaked boron profile with and without a SiGeC or SiGe layer placed between the peaks was used to test the effect of the layer on boron diffusivities at different locations (above and below) with respect to the SiGe/SiGeC layer. Both boron peaks were approximately 250A thick and had a boron concentration of 5*10¹⁹/cm³ centered 2000A and 3000A away from the surface respectively, while the 250A thick SiGeC layer was centered 2300A from the surface. As-grown samples were then cleaved and annealed in nitrogen and oxygen ambient atmospheres at 850°C for 30 minutes. Boron profiles were characterized using secondary ion mass spectroscopy (SIMS), and a commercially available process simulator (TSUPREM4 by TMA) was used to quantitatively compare boron profiles and obtain boron diffusivities. Silicon samples, oxidation at 850°C is observed to cause a 10 times enhancement of boron diffusivity, consistent with existing simulators. Unlike previous reports of partial OED suppressions, introduction of 0.5% substitutional carbon in SiGeC between the oxidizing surface and boron marker completely suppresses any oxidation enhanced diffusion, presumably by filtering out all interstitials injected at the surface by the oxidation process. Work is in progress to determine the critical density of susbtitutional carbon to suppress boron OED. A comparison of Si, SiGe, and SiGeC samples shows that substitutional carbon, not Ge, is critical for this result. Further, we report a boron diffusivity 33% of that in the annealed Si control sample layer -350A above the SiGeC layer (i.e. between the top surface and the SiGeC layer). This nonlocal suppression of boron diffusion, indicates that the SiGeC getters Si interstitials with an effective range of over ~350A in all cases including annealing in oxygen atmospheres. This work was supported by ONR (NO0014-96-1-0334), and AFOSR. References:1. L. D. Lanzerotti, et. al, Appl. Phys. Lett. vol 70, No 23, 9 June 972. Stolk, H. J. Gossmann, D. J. Eaglesham, J. M. Pate, Mat. Sci. & Eng. B36, 275-81, 96

N_{RT} ~ [illegible] , n_{10} ~ 5x10¹⁹

[illegible] gets limit in SiC ≈ SiGeC ~ 0.5%..

2:50 PM, H5+

Effect of Low Carbon Levels on Boron Diffusion and Strain Relaxation in $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ Alloys: ANDA C. MOCUTA[1]; Richard Strong[2]; David W Greve[1]; [1]Carnegie Mellon University, Department of Electrical and Computer Engineering, 5000 Forbes Ave. , Pittsburgh, PA 15213 USA; [2]Northrop Grumman, STC, 1350 Beulah Rd., Pittsburgh, PA 15235 USA

We report the growth of p-type $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ epitaxial layers using Ultra High Vacuum Chemical Vapor Deposition (UHV/CVD). This is a novel application of UHV/CVD, a batch process epitaxial growth technique used in the commercial manufacture of Si-based integrated circuits. Silane, germane, and methylsilane were used as the source gases for Si, Ge, and C respectively. Boron doping was achieved both by (1) in-situ doping using diborane; and (2) B-implantation followed by annealing. Both doped and undoped layers were annealed at temperatures of up to 900 °C and analyzed using SIMS and high-resolution X-ray diffraction. For small concentrations (0.25%), carbon incorporation is completely substitutional in both $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$. These low carbon levels produce a significant enhancement in the thermal stability of SiGe alloys. Upon annealing at 900 °C for 1 hour, no significant strain relaxation occurs in SiGeC single layers or multiple quantum well structures while in similar SiGe structures with comparable strain and thickness strain relaxation is observed. The addition of carbon also greatly reduces the diffusivity of boron, regardless of whether the boron is implanted or incorporated during growth. For a 900 °C, 30 min anneal boron diffusion has been effectively inhibited in $Si_{1-y}C_y$ and a reduction in diffusion coefficient by at least a factor of 10 could be calculated. Sheet resistances of $Si_{1-y}C_y$ films with [B] ~ 10¹⁹ cm⁻³ are unaffected by low carbon levels; I/V characteristics of pn junctions show no increase in recombination current with the addition of 0.25% carbon. Fabrication of SiGe heterojunction bipolar transistors or p-channel MOSFETs involves both ion implantation and high temperature annealing steps. These results demonstrate that incorporating small amounts of substitutional carbon into films grown by UHV/CVD can have beneficial effects in processing devices by allowing a higher thermal budget.

no SiGeC [illegible] 25% [illegible] SiGe | Si 15Ge | Si | Si | Si

Tc

3:10 PM Break

3:30 PM, H6

Effect of Growth Interruption on Si/SiGe Layers Using UHVCVD: JACK O. CHU[1]; Khaled Ismail[1]; Steve Koester[1]; [1]IBM T.J. Watson Research Center, Div 22/ Dept K4W, P.O. Box 218, MS 18-246, Yorktown Heights, NY 10598 USA

Si/SiGe modulation-doped layers have been harnessed to study the effect of growth interrupt on the epitaxial quality of layers grown by UHVCVD. Without any growth interruption, a mobility of about 1,900 cm²/Vs (55,000 cm²/Vs) is achieved at 300K (20K). The growth was interrupted at varying distance underneath the strain Si electron channel, while the wafers were pulled out to the load lock for 60 minutes. For an interrupt that is 200nm underneath the channel, there was no measurable effect on the mobility. However, interrupting the growth at 50nm, 10nm, and 0nm from the channel resulted in a mobility of 1,500, 1200, and 600 cm²/Vs at room temperature, and 43,000, 8100 and 450 cm²/Vs at 20K, respectively. The interrupt was associated with an oxygen spike in the SIMS profile amounting to a dose of 1 x 10¹³cm⁻². If, however, the wafers are cooled to 380C prior to growth interrupt while flowing SiH_4, the surface reamins hydrogen passivated, and the mobility increases from 600 cm²/Vs to 1630 cm²/Vs at 300K, and from 450 cm²/Vs to 25,300 cm²/Vs at 20K, for the case of interrupting the growth right underneath the channel. Thus the hydrogen passivation can be used as a valuable technique to interrupt the growth in case

[illegible]