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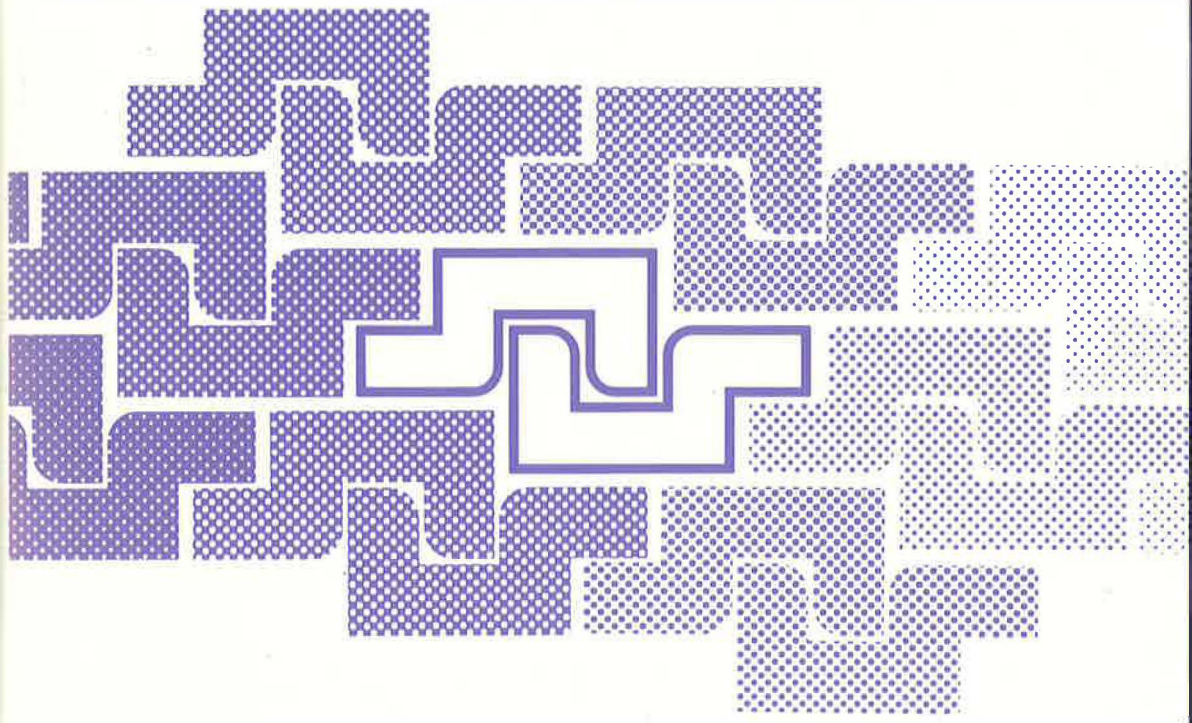

Physical and Technical Problems of SOI Structures and Devices

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SEMI-INSULATING OXYGEN-DOPED SILICON BY LOW TEMPERATURE CHEMICAL VAPOR DEPOSITION FOR SOI APPLICATIONS

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Abstract

In this paper the growth of crystalline silicon layers with large amounts of oxygen (~10^{20} cm^{-3}) by low temperature chemical vapor deposition is described. These layers have semi-insulating electrical properties with resistivities as large as 10^6 Ω-cm at room temperature and exhibit the classic characteristics of a space-charge limited current in an insulator with many deep traps. Single crystal SOI layers without oxygen were grown on top of the semi-insulating layers. P-channel MOSFET's fabricated in these films had characteristics above threshold similar to bulk control samples, although their subthreshold characteristics were degraded.

1. Introduction

The advantages of SOI, such as reduced substrate capacitances, reduced process complexity, and improved scaling and subthreshold slopes (Colinge effect) are well known. However, all of the conventional processes for the formation of

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SOI layers, such as SIMOX, ZMR, bond-and-etch, etc, suffer from one or more of several technological or economic problems. The primary economic problem is the time for processing (such as high oxygen doses or long laser scanning times), leading to high wafer costs. Besides defects, other key technical problems associated with the buried oxide and active silicon layer are the control, uniformity, and flexibility of choice of the film thicknesses. These problems will probably only become more significant as the wafer size increases.

One technical approach towards an SOI formation process which addresses the issues of large-area capability, low-cost, and good layer thickness control would be an all epitaxial process. First an epitaxial insulator on the silicon substrate would be grown, followed by the SOI layer. This approach has been limited by the availability of an epitaxial insulator lattice-matched to silicon. Considerable work in the past has been done using CaF_2 and related materials as insulators [1]. While considerable progress was made, this effort suffered from differing thermal expansion coefficients, facetting of the CaF_2 surface, and incompatibility of CaF_2 with conventional Si processing.

In this paper, we describe the growth, electrical properties, and SOI application of a new material, oxygen-doped crystalline silicon (Si:O) [2], as an epitaxial semi-insulator on (100) silicon substrates. The motivation for the work was the fact that O is known under certain conditions to introduce levels 0.4 eV and 0.6 eV above the valence band edge in silicon [3]. The incorporation of large amounts of oxygen into silicon might then lead to a pinning of the fermi level near midgap, leading to semi-insulating characteristics.

Previous attempts to incorporate large amounts of oxygen into silicon included Semi-Insulating POlycrystalline Silicon (SIPOS), which was formed by CVD and could contain up to several tens of percent of oxygen [4]. The application of these polycrystalline films was for surface passivation [5] and for a wide bandgap emitter in silicon-based heterojunction bipolar transistors [6]. OXygen-doped Silicon Epitaxial Films (OXSEF) have also been grown as a crystalline substitute for wide bandgap emitters [7]. These crystalline layers were grown by MBE between 300 and 700 ^{o}C, and surprisingly could contain on the order of 10% oxygen [8]. When heavily doped with arsenic, the layers were conducting.

2. Growth of Oxygen Doped Silicon (Si:O) by Chemical Vapor Deposition (CVD)

During conventional silicon epitaxy (e.g. > 900 ^{o}C), the presence of small

amounts of oxygen or water vapor (e.g. < 10 ppm) in the growth chamber has little effect on the quality of the layers. The oxygen concentration in the epitaxial layers in this case is typically below that of the maximum solid solubility (~2 x 10^{18} cm^{-3}). For higher amounts of contaminant in the source gases, first heavily defected layers (eg. with many stacking faults and a very hazy surface) are found and then polycrystalline layers result. Therefore we have focussed our work on low-temperature CVD (700-750 °C) with the hope that excessive SiO_2 precipitation and the defect formation which leads to polycrystalline growth could be surpressed. The layers were grown in a lamp-heated CVD chamber equipped with a load-lock and gas purifiers, so that the background oxygen and water concentrations were <100 ppb. The source gases were either silane or dichlorosilane in a hydrogen carrier at 6 torr. Oxygen was introduced by bleeding small controlled amounts of a dilute oxygen in argon mixture into the growth chamber. Oxygen was chosen instead of water vapor because water vapor was found to stick to the quartz chamber walls, and the water partial pressure could take days to decrease after the water vapor source was shut off. No such problem was observed using an oxygen source.

The material was initially characterized by infrared absorption (FTIR), X-ray diffraction (XRD), and SIMS. It was found that up to 10^{20} cm^{-3} of oxygen could be incorporated into the films while they still remained crystalline and without any evidence of haze on the sample surface. The amount of oxygen incorporated into the films was two orders of magnitude lower than that expected from sticking coefficeints determined in UHV experiments. This was attributed to the passivating effect of a hydrogen layer on the sample surface present during CVD, and also due to the presence of a boundary layer during CVD growth [9]. Fig. 1 shows a typical X-ray diffraction curve of a sample containing 5 x 10^{19} cm^{-3} of oxygen and a thickness of 5 microns. No polysilicon peaks are present and only strong single crystal peaks are seen. A typical FTIR spectrum of a similar sample with a slightly higher oxygen level (~10^{20} cm^{-3}) is shown in Fig. 2. A broad peak around 1010 cm^{-1} is observed, which is at an energy considerably lower than those normally observed for interstitial O in Si (1107 cm^{-1}) and for various forms of SiO_x precipitates (1100-1230 cm^{-1}). This spectrum looks very similar to that previously observed in OXSEF samples [8]. The exact microstructural configuration of the oxygen in our Si:O layers is not known at present.

3. Electrical Characterization and SOI Applications

To avoid complications with parallel conduction from the underlying substrate, the layers were evaluated mostly using vertical transport measurements. In some cases the layer directly on top of the Si:O was a metal contact, and in other

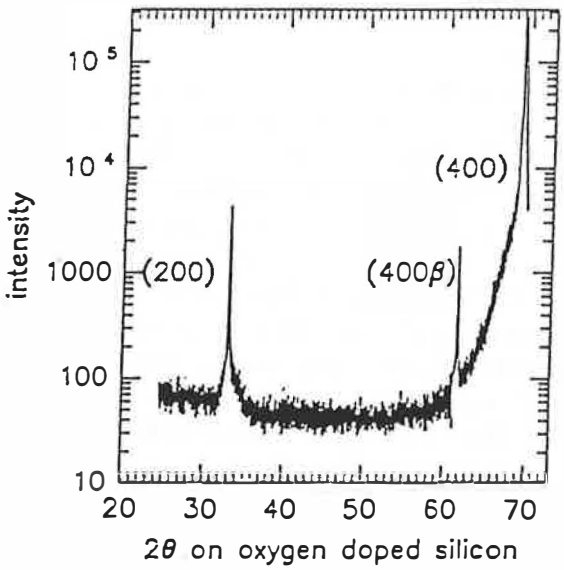

Fig. 1. X-ray diffraction (using Cu-K_α and Cu-K_β radiation) of a 5-μm thick Si:O film containing 5 x 10^{19} cm^{-3} of oxygen, showing no evidence of any polycrystalline silicon.

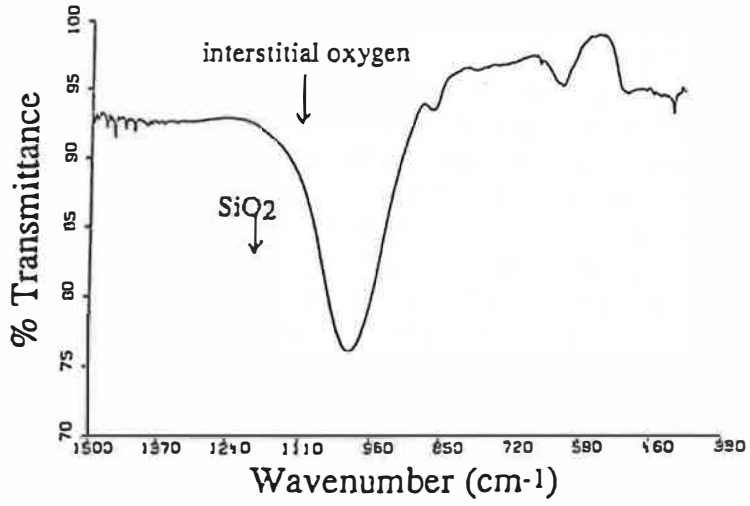

Fig. 2. FTIR transmission spectrum of a 5 μm thick Si:O layer containing ~10^{20} cm^{-3} of oxygen.

cases it was a crystalline silicon layer without oxygen grown on top of the Si:O. This was accomplished simply by turning off the oxygen flow, although in most cases the growth temperature was also then raised to 1000 °C to give a faster growth rate. These top Si layers were either doped p-type or n-type by introducing dopants during the epitaxial growth.

A typical I-V curve at room temperature from an aluminum Schottky barrier on undoped Si:O (thickness 10 microns) on an n-type substrate is shown in Fig. 3. The current in forward bias was limited by the resistance of the Si:O layer, from which the resistivity of the SiO layer was then extracted. These measurements were made as a function of temperature for layers containing total oxygen concentrations on the order of both 5 x 10^{19} cm^{-3} and 2 x 10^{20} cm^{-3} (Fig. 4). For both samples a resistivity of ~10^6 Ω-cm was found near room temperature, with the value for the sample with more O somewhat higher. Assuming mobilities near that of bulk Si, such a resistivity implies a fermi level pinned near midgap. Further evidence that the fermi level in the material was pinned near midgap is the activation energy of the resistivity which in both cases was 0.6 eV, approximately half of the bandgap of silicon. As the nature of the microstructure of the oxygen is not known, the exact mechanism which contributes to the fermi level pinning (surface states of oxide precipitates, levels due to isolated O atoms, etc) is also not known.

More complex are the I-V characteristics observed in p-Si/undoped Si:O/p-Si structures at higher electric fields. In materials with very low intrinsic carrier densities, such as insulators or semi-insulators, there are not sufficient carriers present in the material to conduct large amounts of current. At higher current levels, excess carriers which flow in from the contacts must be present, giving the material a net charge. This charge in the material causes the I-V characteristics to deviate from a simple ohmic relationship. In the simplest case (Fig. 5(a.)), the log I - log V characteristics have a slope of 1 at low currents where the background carrier density is sufficient to carry current, but a slope of 2 at higher currents where there is a large injected carrier density. If traps are present in the material, the situation can become more complex [10]. In this case, a jump in the log I - log V characteristics can be observed as the quasi-fermi level passes through the trap level, both because of changes in scattering and because all new injected carriers will then be available for conduction (Fig. 5 (b.)). Such characteristics are indeed observed from experimental structures (Fig. 6), confirming that deep levels are indeed present in the Si:O material. From a quantitative analysis of Fig. 6, a trap density on the order of 10^{19} cm^{-3} can be inferred [2]. This is consistent with high donor and acceptor doping experiments of Si:O in our lab, as at very high doping levels (e.g. concentrations of phosphorus or boron >> 10^{19} cm^{-3}), the Si:O films are no longer semi-insulating and conduct well. Hall measurements of doped layers yield a hole mobility which is somewhat lower

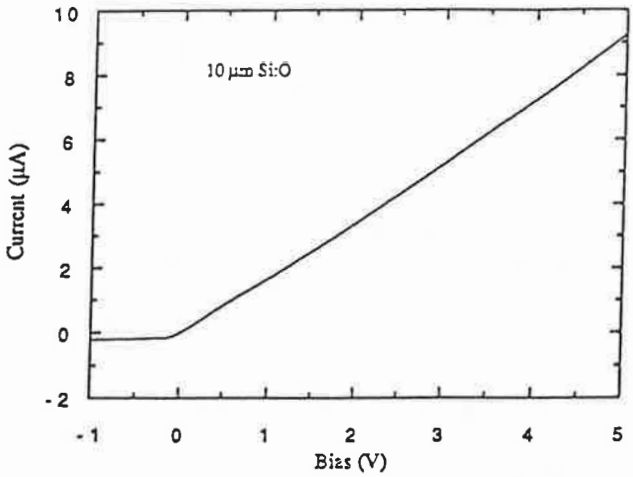

Fig. 3. Current-voltage characteristic of an Al/10-μm undoped Si:O/n-type Si Schottky barrier at room temperature.

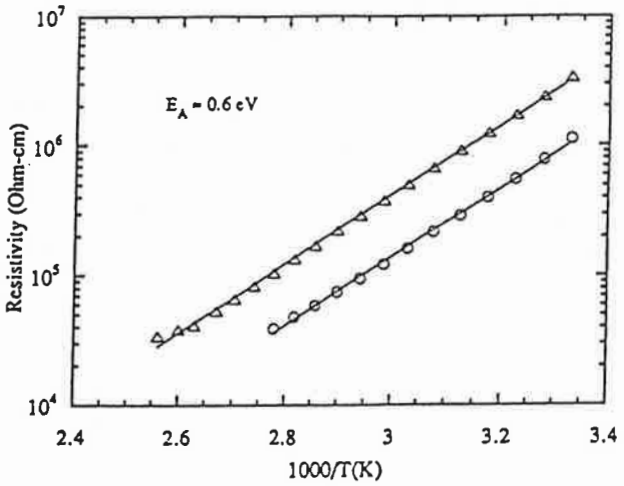

Fig. 4. Resistivity vs temperature of Si:O layers for fields less than 5 x 10^3 V/cm. Triangles indicate oxygen concentrations of ~2 x 10^{20} cm^{-3} and circles indicate oxygen concentrations of ~5 x 10^{19} cm^{-3}.

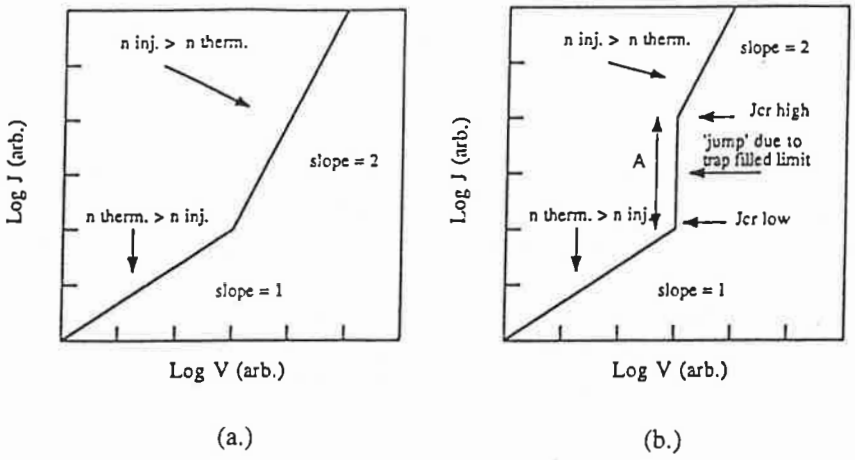

Fig. 5. Schematic log I - log V curves of space charge limited current in an insulator (a.) without traps and (b.) with traps.

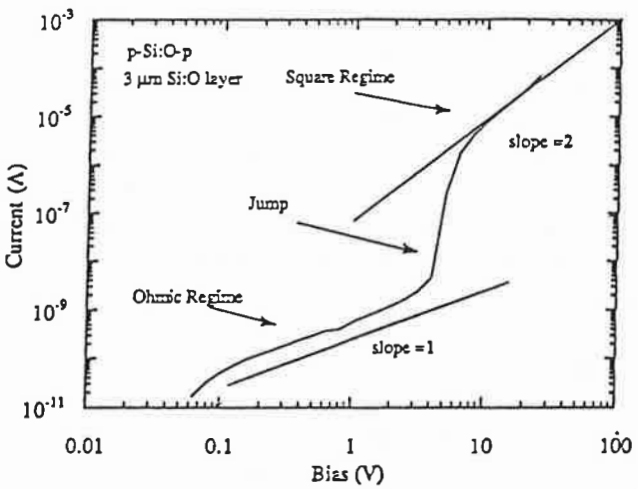

Fig. 6. Log I- log V characteristics of a p-Si/Si:O/p-Si structure. The Si:O thickness is 3 μm.

than bulk material. p-Si/undoped Si:O/n-Si structures in forward bias show a current-controlled hsyterisis (Fig. 7). This is also characteristic of a semi-insulating material with a high trap density [10].

The lifetime of the material was probed using an all optical pump and probe technique in a thick (10 μm) Si:O layer with approximately 10^{20} cm^{-3} oxygen [11]. First a pump pulse excites carriers in the Si:O layer, and their recombination is monitored through their effect on the reflectance of a second probe pulse, whose delay from the pump pulse can be adjusted. From the exponential decay of the reflected probe signal vs. delay, a lifetime of ~ 50 ps may be extracted (Fig. 8). Such a low lifetime is to be expected given the large number of traps in the material.

4. SOI FET's

SOI FET's were fabricated by growing ~0.6 um of crystalline Si n-type (~10^{16} cm^{-3}) without oxygen doping at 1000 °C on top of 1.5 um of Si:O. P-channel MOSFET's were then fabricated by a standard self-aligned process using simple mesa isolation for the SOI islands. The gate oxide was thermally grown to a thickness of ~40 nm. Typical SOI FET characteristics and those of simultaneously fabricated bulk control FET's are shown in Fig. 9. Well-behaved characteristics were obtained, with a slightly higher threshold voltage in the SOI case, possibly due to a lower doping in the control wafer. Long-channel devices showed similar mobilities for both the SOI and bulk devices. N-channel devices in the SOI films were also well behaved above threshold, but a processing failure in the control devices prevented any comparison with bulk devices.

The subthreshold characteristics of the PMOS devices are shown in Fig. 10. An unknown process problem caused fairly poor subthreshold slopes (~250 mV/decade) and high leakage current in the bulk devices. The subthreshold performance of the SOI devices was still worse, however (~1000 mV/decade). It is not known if this poor performance is due to defects in the SOI films (or at the top SiO_2 interface) itself, or is due to full depletion resulting from poor control of the intended doping of the SOI film during epitaxial growth. If full depletion occured, the many deep levels in the underlying Si:O layer would be expected to lead to a poor subthreshold slope.

5. Future Directions

Recent TEM results [12] have shown that the Si:O layers with oxygen con-

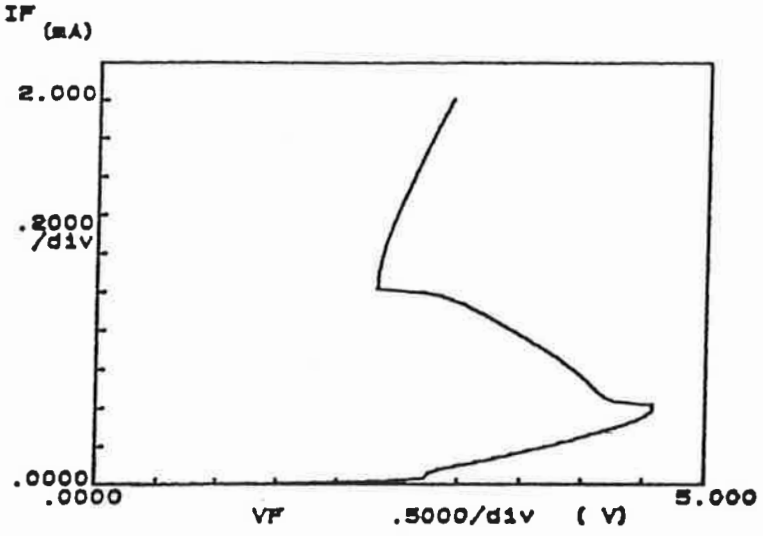

Fig. 7. Current-Voltage characteristics of a double-injector (p-Si/Si:O/n-Si) structure in forward bias.

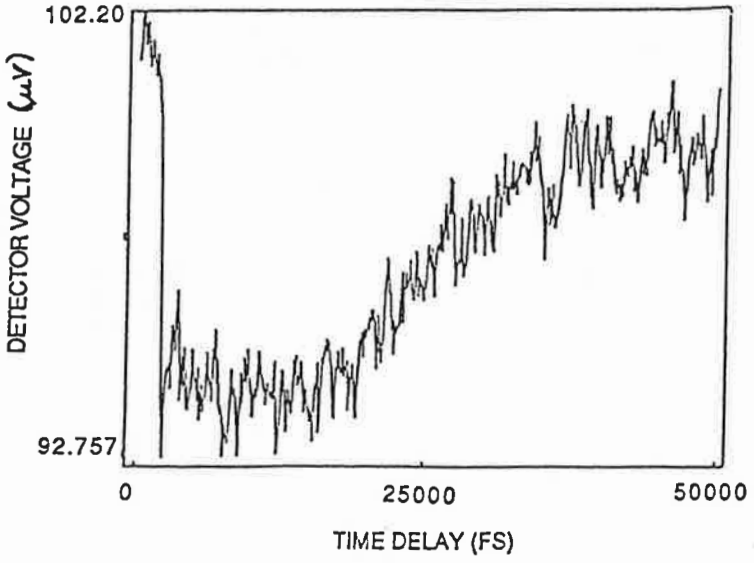

Fig. 8. Reflectance vs time of a 10 mm Si:O layer after excitation by a 20 ns laser pulse. A recombination lifetime of ~50 ps can be extracted.

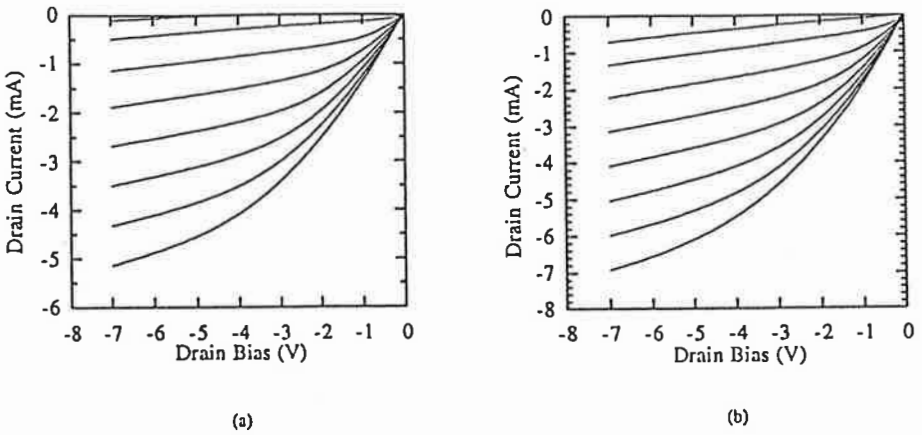

Fig. 9. I-V characteristics of (a.) SOI and (b.) control (bulk Si) FET's with W = 50 μm and L = 2 μm. The gate voltage is stepped from 0 V to -7 V in 1 V increments.

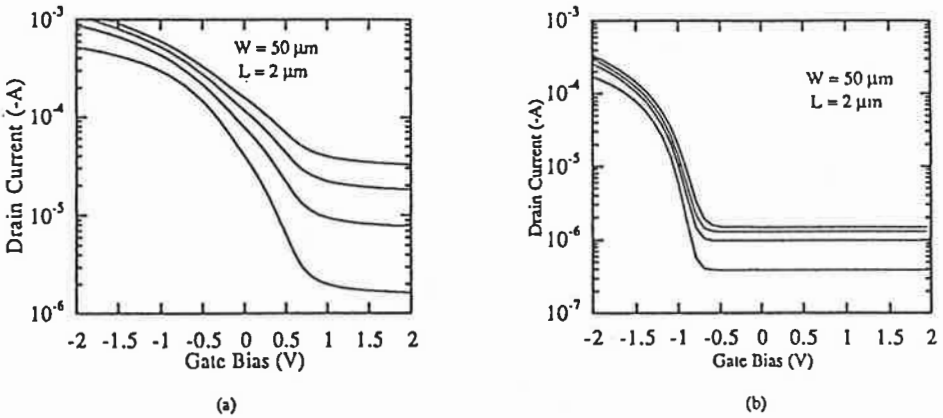

Fig. 10. Subthreshold characteristics of (a.) SOI and (b.) control MOSFET's. The drain voltages were -0.5, -1.0, -1.5, and -2.0 V.

centations on the order of 1 - 5 x 10^{19}cm^{-3} contain hairpin dislocations originating at the lower Si/Si:O interface, but with a density not exceeeding 10^7 cm^{-2}. SiO_x precipitates were also found at the lower Si/SSi:O interface (about 2-3 nm diameter), as were smaller precipitates uniformly throughout the film. For oxygen levels an order of magnitude higher, a high density of stacking faults (10^{11} cm^{-2}) and microtwins was seen in the Si:O as well as much larger precipitates (~ 15 nm) in the entire layer.. For the two cases of high and low oxygen concenration, defect densites (stacking faults and dislocations) in overlying SOI films without O were ~10^7 and 10^5 cm^{-2}, respectively. This indicates that still lower growth temperatures are required to surpress oxygen precipitation and related defects during the CVD process. It should be noted that due to unintentional contamination, SiGe layers grown by CVD on Si at ~640 °C with ~ 10^{20} cm^{-3} of oxygen have been reported [13]. Despite this high oxygen density, no defects or precipitates could be observed in these layers by TEM, or in overlying Si layers grown at higher temperature without O contamination . Although the films were conducting due to their high dopant concentration (~ 10^{19} cm^{-3} to ~ 10^{20} cm^{-3}), they demonstrate the advantages in crystal quality which can be obtained at lower growth temperatures when large amounts of oxygen are present.

6. Summary

Semi-insulating crystalline silicon layers with ~ 10^{20} cm^{-3} of oxygen can be grown by low temperature CVD. The layers have a resistivity of ~ 10^6 Ω-cm at electric fields below 10^4 V/cm, and exhibit the classic characteristics of space-charge limited current in an insulator with traps at higher current levels. Crystalline Si layers without oxygen can be grown on top of these semi-insulating layers. FET's in the SOI layers have good mobilities, but poor subthreshold slopes and high leakage levels. The key to improved material quality appears to be lowering the growth temperature of the Si:O layers.

7. References

1. T. Asano and H. Ishiwara, J. Appl. Phys. **55**, 3566 (1984).

2. P.V. Schwartz, C.W. Liu, and J.C. Sturm, Appl. Phys. Lett. **62,** 1102 (1993).

3. S.M. Sze, *Physics of Semiconductor Devices*, 2nd. ed. (Wiley, New York, 1981), p. 27.

4. H. Mochizuki, T. Aoki. H. Yamaoto, M. Okayama, and T. Ando, Suppl. Jpn. J. Appl. Phys. **15**, 41 (1976).

5. T. Matsushita, T. Aoki, T. Ohtsu, H. Yamoto, H. Yayashi, M..Okayama, and Y. Kawana, IEEE Trans. Electron Device **TED-23**, 826 (1976).

6. T. Matsushita, N. Oh-uchi, H. Hayashi, and H. Yamoto, Appl. Phys. Lett. **35**, 549 (1979).

7. M. Takahishi, M. Tabe, and Y. Sakakibara, IEEE Electron Device Lett., **EDL-8**, 475 (1987)

8. M. Tabe, M. Takahashi, and Y. Sakakibara, Jpn. J. Appl. Phys. **26**, 1830 (1987).

9. P.V. Schwartz and J.C. Sturm, J. Electrochem. Soc. **141**, 1284 (1994).

10. M.A. Lampert and P. Mark, *Current Injection in Solids* (Academic, New York, 1970).

11. P.V. Schwartz, C.W. Liu, J.C. S turm, T. Gong, and P.M. Fauchet, presented at the Elec. Mat. Conf., Cambridge, MA, USA (June, 1993).

12. Z. Liliental-Weber, P.V Schwartz, C.C. Wu, and J.C. Sturm, J. Vac. Sci. Tech. **B12**, 2511 (1994).

13. C.A. King, J.L. Hoyt., and J.F. Gibbons, IEEE Trans. Elec. Dev. **TED-36**, 2093 (1989).