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# A Three-Dimensional Merged Vertical Bipolar-MOS Device in Recrystallized Silicon

J.C. Sturm and J.F. Gibbons

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To date almost all work in laser-recrystallized films has concentrated on majority carrier devices. We have recently successfully fabricated vertical bipolar transistors in these films with a current gain of 100 [1], and have used this technology to develop a merged vertical bipolar-MOS device. The four-terminal device has the three terminals of a conventional bipolar transistor plus a fourth which serves to gate the collector current on or off.

The device was made in a 0.75 um p-type silicon film recrystallized with a shaped laser beam. An npn polysilicon emitter vertical bipolar transistor was then fabricated in the film in a fairly typical manner except that no collector buried layer or n-layer was provided. In order to achieve vertical bipolar transistor action, a collector layer is electrically created by biasing the substrate under the film to invert the p-type lower surface of the recrystallized film, leaving an effective base width of 0.2 um. Electrons flowing down across the base can then be collected into the inversion layer and flow to a collector contact on the side as in a conventional bipolar transistor. The collector is thus an MOS channel gated by the electrode under the film, and with a 5V swing on the bottom terminal an on/off current ratio of better than $10^5$ has been observed.

Despite a sub-grain boundary spacing of only a few microns, by minimizing the emitter implant anneal time and temperature, yield loss due to emitter-collector shorts from sub-grain boundary diffusion of the emitter dopant was avoided. Possible applications include logic and an analog multiplier.

1. J.C. Sturm and J.F. Gibbons, IEEE Elect. Dev. Lett., to be published.

—move E between B & C
- but keep lateral trans low

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ter-base and base-collector junctions were 1 and 4 $\mu$m, respectively, below the surface of the Si wafers. After fabrication of the bipolar transistors, the wafers were coated, using chemical-vapor deposition, with 2 $\mu$m of $SiO_2$, 1 $\mu$m of Si, and a cap of 2 $\mu$m of $SiO_2$ and 30 nm of sputtered $Si_3N_4$. The 1-$\mu$m-thick Si was converted by ZMR at speeds of 0.5 or 1 mm/s into a high-quality crystalline film in which high-quality MOSFET's were then fabricated using self-aligned implantation with poly-Si gates. In-plane distortion occurring as a result of ZMR ranged from 9 to 20 $\mu$m as measured between at the center and edge of a 3-in wafer.

The device characteristics of the bipolar transistors were measured before and after ZMR and MOSFET fabrication. Before ZMR, $h_{FE}$ was 20 to 30 and $|BV_{CEO}|$ had a value of 100 to 120 V for both n-p-n and p-n-p devices. Although ZMR brings the Si wafer to within a fraction of a degree of the melting point of Si, the n-p-n devices showed no measurable degradation. For ZMR at 1 mm/s the p-n-p devices showed an increase in leakage current, an increase in $h_{FE}$ to 100 and a reduction in $BV_{CEO}$ to about $-40$ V. These changes can be attributed to pipes that locally short the itter to the collector. We believe that the degradation can be reduced by increasing the ZMR rate, since the results for 1 mm/s were significantly better then those for 0.5 mm/s.

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**VB-2 A Three-Dimensional Merged Vertical Bipolar-MOS Device in Recrystallized Silicon**—J. C. Sturm and J. F. Gibbons, Stanford Electronics Laboratories, Stanford University, Stanford, CA 94305.

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The device was made in a 0.75-$\mu$m p-type silicon film recrystallized with a shaped laser beam. An n-p-n polysilicon emitter vertical bipolar transistor was then fabricated in the film in a fairly typical manner except that no collector buried layer or n-layer was provided. In order to achieve vertical bipolar transistor action, a collector layer is electrically created by biasing the substrate under the film to invert the p-type lower surface of the recrystallized film, leaving an effective base width of 0.2 $\mu$m. Electrons flowing down across the base can then be collected into the inversion layer and flow to a collector contact on the side as in a conventional bipolar transistor. The collector is thus an MOS channel gated by the electrode under the film, and with a 5-V swing on the bottom terminal and on/off current ratio of better than $10^5$ has been observed.

Despite a subgrain boundary spacing of only a few micrometers, by minimizing the emitter implant anneal time and temperature, yield loss due to emitter collector shorts from subgrain boundary diffusion of the emitter dopant was avoided. Possible applications include logic and an analog multiplier.

[1] J. C. Sturm and J. F. Gibbons, *IEEE Electron Device Lett.*, to be published.

**VB-3 Polycrystalline Silicon Devices for Large-Area NMOS and CMOS Logic Applications**—William G. Hawkins, Xerox Webster Research Center, Webster, NY.

A fabrication process for polycrystalline silicon (polysilicon) thin film transistors was tailored to provide a basis for NMOS or CMOS logic circuitry. Implementation of logic circuitry in polysilicon mandates ability to select and control threshold voltage, low leakage current in the off state, high mobility for good frequency performance, n- and p-channel devices or enhancement- and depletion-mode devices for CMOS and NMOS, respectively, and high subthreshold output current swing for fast switching. Fabrication processes for polysilicon devices reported to date suffer from low mobility and anomolous leakage as well as high threshold voltage.

Grain boundary scattering in polysilicon reduces device channel mobility approximately an order of magnitude below that of single-crystal material. Polysilicon devices fabricated in thick layers maximize channel mobility because grain enlargement caused by high-temperature annealing is limited in lateral extent to film thickness. Alternatively, thin channel layers achieve low off currents by full depletion of the deposited silicon channel layer. Reduction in mobility is the ramification of the thin fully depletable channel.

The present fabrication sequence has achieved the high mobility typically observed in thick film channels while retaining currents of less than 1pA/$\mu$m of channel width. The key process steps for simultaneous achievement of high mobility ($\mu_h = 35$, $\mu_e = 50$ $cm^2/V \cdot s$) and low leakage for both n- and p-channel devices are: i) the 150-nm-thick silicon channel layer was deposited as an amorphous silicon film by using a conventional low-pressure chemical-vapor deposition system at 575°C. ii) The deposited channel layer was oxidized at or above 1050°C but below 1100°C in dry oxygen. iii) Devices were immersed in a plasma of atomic hydrogen following device sintering at 400°C. Aluminum and $n^+$ polysilicon self-aligned gate technologies were investigated. Following contact sintering, but prior to hydrogenation, the aluminum gated devices show superior mobility but equivalent threshold voltages. Following brief hydrogenation, aluminum gated devices show mobility and threshold voltage improvement which saturates rapidly. More lengthy exposure of poly gated devices to the atomic hydrogen environment yields equivalent performance to aluminum gated devices. The self-aligned poly gate process is more desirable in logic applications since Miller capacitance is lowered.

The oxidation temperature also plays a major role in determining the channel mobility both n- and p-channel devices. Oxidation at a low temperature followed by inert nitrogen annealing at higher temperatures yields devices with low channel mobility compared to oxidation at the higher temperature. The sensitivity of mobility to furnace ambient as well as process temperature suggests that excess silicon self-interstitials play a role in mobility enhancement.

**VB-4 Comparison of Different Techniques for Passivation of Small-Grain Poly-Si MOSFET's**—M. Rodder* and S. Madan, Massachusetts Institute of Technology, Cambridge, MA 02139.

Hydrogen passivated small-grain poly-Si SOI MOSFET's are currently being investigated for SRAM and DRAM circuits. In this paper, we present a new technique based on the rapid thermal annealing (RTA) of hydrogen implanted device structures. Specifically, we compare the RTA *-I/IH* technique with (a) our earlier method of passivation (sintering of Al contacts in presence of encapsulating LPCVD $Si_3N_4$) and (b) hydrogen passivation from a plasma nitride source. We also report on the dependence of device characteristics on (a) annealing (and/or sintering) time and temperature, (b) different doposition conditions of the poly-Si, and (c) different encapsulation layers.

Self-aligned poly-Si gate MOSFET's with a *W/L* ratio of 256 $\mu$m/2 $\mu$m were fabricated in small-grain poly-Si of final thickness 150 nm. All gate dielectrics consist of 70 nm of $SiO_2$ and 55 nm of $Si_3N_4$. The top encapsulating layer was either 80 nm of LPCVD $Si_3N_4$ alone, 1100 nm of plasma deposited $Si_3N_4$ alone, a composite layer of 80 nm of LPCVD $Si_3N_4$ and 1100 nm of plasma $Si_3N_4$, or there was no encapsulating layer. For our method reported earlier, contact holes were opened after deposition of the LPCVD $Si_3N_4$ and the Al was patterened and sintered at various temperatures and times in $N_2$. Both time and temperature of the sintering step affect